Contribution ID: **112** Type: **Poster**

Upgrades to the CSC Cathode Strip Chamber Electronics for HL-LHC

Tuesday, 27 September 2016 17:54 (1 minute)

The luminosity, latency, and trigger rate foreseen at the High Luminosity LHC presents challenges to efficient readout of the Cathode strip chambers (CSCs) of the CMS end cap muon detector. Upgrades to the electronics are targeted for the inner rings of CSCs in each station, which have the highest flux of particles. The upgrades comprise digital cathode front end boards for nearly deadtimeless operation long latency capacity, new DAQ motherboards with higher-bandwidth links to accept the higher data rate, and a new Front End Driver system that can receive the higher input rates.

Summary

Cathode strip chambers (CSCs) are used to detect muons in the end cap region of the CMS detector. The chambers are arranged in rings in four planes on each end of the detector. The inner rings of CSCs in each station have the highest flux of particles and this presents challenges to efficient readout at the luminosity, latency, and trigger rate foreseen at the HL-LHC.

The existing front end electronics in Stations 2, 3, and 4 are based on switched capacitor arrays with limited buffering capability. Queuing models have shown that significant saturation of the buffers would occur for the luminosity, Level 1 trigger rates, and required Level 1 latency for running at the HL-LHC. In addition, the expected output rate of data is expected to exceed the 1 Gbps bandwidth of the optical links that carry data to the back end, resulting in loss of event synchronization.

The upgrade of the inner ring of CSCs addresses these problems by replacing some types of electronics boards in these rings with upgraded boards. In particular, the existing cathode front end boards on the inner rings of Stations 2, 3, and 4 will be replaced with new digital cathode front end boards. These boards follow the design of those installed in the inner ring of Station 1 in the recent long shutdown of the LHC. The boards use flash ADCs and digital pipelines in place of the switch capacitor arrays used previously. The digital pipeline results in nearly deadtimeless operation and the capability to accommodate long latency requirements without loss of data. Also, new DAQ motherboards will be designed with optical output links with higher bandwidth to accept the higher data rate. Finally, the FED system, which is the interface between the CSCs and the central DAQ of the CMS experiment, will be replaced with a system that can receive the higher input rates.

We present the measurements and calculations that predict the behavior of the CSC electronics under HL-LHC conditions. We describe the design of the electronics systems for the upgrade and show studies of expected performance.

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Session Classification: POSTER

Track Classification: Systems