

Design studies for the Phase II upgrade of the CMS Barrel Electromagnetic Calorimeter



- **Front-End (FE) : Data pipeline & transmission**
- Separate readout for data & trigger
- 40 MHz readout of 2448 TT, 100 kHz readout of 61200 channels (single crystal).

pre-amplifier (MGPA), 43 ns shaping time, 12 bit ADC



NEW AND				
	2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2	2020 2021 2022 2023 2024 2025 2026	2027 2028 2029 2030 2031 2032 2033 2034 2035 2036 20)37
	LHC		HL-LHC	•
	E = 7-14 TeV		E = 14 TeV	
	$L = 1 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ PU> ~ 40-60		L = $5 \cdot 10^{34} \text{ cm}^{-2} \text{s}^{-1}$ <pu> ~ 140</pu>	
	\geq 50 fb ⁻¹ per year 300-500 fb ⁻¹ total		250 fb ⁻¹ per year 3000 fb ⁻¹ total	

Target for CMS ECAL Phase II upgrade at HL-LHC : Maintain physics performance for $H \rightarrow \gamma \gamma$ at 5x higher luminosity and pile-up (PU), increased radiation levels and adjusting to the increased first level trigger rate of 750 kHz at 12.5 µs latency.

Upgrade strategy & implementation :

- ➢ PbWO₄ Crystals, APDs, mother boards, & overall mechanical structure will remain
- > Reduce temperature from 18° C to 8º C
- > VFE similar, but change shaping + digitization
- > FE card becomes pipeline, most processing off-detector
- > Same data stream for trigger & data > Full detector readout with upgraded links > Off-detector electronics upgraded to higher transfer rates & generation of trigger primitives



- > FE : Move L1A pipeline off-detector with arbitrary trigger latency
- Trigger primitive generation off detector single crystal granularity. See poster by Nabarun Dev.
- > Data links from detector to readout cards updated to versatile link w/ GigaBit Transceiver (GBT) \Rightarrow full granularity readout for the trigger
- > Potentially more advanced topological filtering of anomalous events
- \succ VFE : Re-designed ASICs to optimize shaping time & sampling \Rightarrow reduce impact of noise, out-of-time PU, spikes, precision timing.
- > Pulse shaper/preamplifier ASIC options : Trans Impedance Amplifiers (TIA) or iteration of current architecture (MGPA, CR-RC), optimized for 130 nm process, faster shaping & additional spike rejection logic. See poster by Sema Zahid.
- > ADC: Multi-channel ADC with ~12 bit resolution, sampling rate up to 160 MHz
- Prototype boards undergoing lab & test beam measurements, Simulation studies ongoing to optimize shaping time & sampling rate

Performance of the upgraded detector :



Noise reduction :

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amplitude

TWEPP 2016, Karlsruhe Institute of Technology

- > APD dark current increases with integrated lumi due to irradiation \rightarrow noise increase ×10 (~400 MeV/channel) after 3000 fb⁻¹.
- > Mitigate by operating EB colder: $18^{\circ} C \rightarrow 8^{\circ} C$, reduce noise by 35%
- Shortening the signal shaping time in VFE will also reduce noise





Spike rejection :

- > Anomalous signals (spikes) are energy deposits directly into APD bulk. Create fake EM-like pattern.
- Spike rejection currently rejected at L1 using coarse topological algorithm > Efficiency will degrade to unacceptable
- levels at HL-LHC due to noise & PU
- > Upgrade for better spike rejection using pulse shape & finer granularity L1



Precision timing @ 30 ps :

> Intrinsic timing resolution of PbWO₄+APD is < 30 ps, as measured at test beam. See poster by Vincenzo Ciriolo. > Use cases for precision timing : Vertex resolution for $H \rightarrow \gamma \gamma$, subtraction of neutral energy from PU that enters **EM clusters, identification of PU jets** > New system designed to approach 30 ps timing precision for high energy EM signals

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