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A Versatile Small Form Factor Twisted-Pair TFC FMC for mTCA AMCs

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In continuous readout systems of particle physics experiments, providing a common clock, time reference and the distribution of critical low latency messages to the processing and fronted layers of the readout is a crucial task. In the context of CBM, a versatile small form factor TFC interfacing FMC was developed, offering bidirectional twisted-pair (TP) links for communicating between TFC nodes and a versatile clocking including voltage controlled oscillators and the connection to the telecommunication clock lines of mTCA crates. Being designed for both TFC Master and Slaves, the card allows rapid system developments without additional Slave hardware circuits.

Summary

Timing and Fast Control (TFC) systems play an important role in the readout of particle detectors. They enable the deterministic recording of data at the frontend electronics (FE), which allows analyzing it in the latter processing layers as coherent data sets.
In the planned CBM readout, the FE in the irradiated area is connected through the radiation-hard GBTx ASICs to FPGA boards in the processing electronics room using optical fiber links. At the FPGA layer, data containers formed from the detector data are then transferred to the server farm through fiber-based 10 Gigabit links.
As a requirement of the self-triggered readout of the CBM system, the FE has to use a clock derived from the fiber link in order to guarantee a deterministic data recording. Thus, the TFC system is connected to the FPGA layer and provides a common reference clock for the fiber links' transceivers towards the FE.
For studying the feasibility of different approaches, a preliminary TFC Master interfacing board was developed as part of our previous work. Though it was sufficient for showing the transmission of TFC data, it lacked features being required from a flexible TFC interface.
For that reason, in this article a new twisted-pair TFC FMC is proposed for the CBM readout, which offers a small form factor allowing it to be mounted onto FPGA-based AMCs for microTCA crates. Besides that, the card is evaluated with a prototype system, demonstrating both its versatility and its applicability for a TFC system inside the processing electronics room.
On this FMC, bidirectional Multi-point Low Voltage Differential Signaling (MLVDS) ICs are connected to galvanically isolated TP lines through multi-port RJ45 connectors.
The four bidirectionally operated pairs of the TP cable are used for different purposes. Fast control messages are exchanged between Master and Slave through two data lines. For the timing functionality, one pair is used for distributing a reference clock from a dedicated IC and another line for the timing control link.
The clocking IC is connected to the bidirectional clock lines of the FMC connector dedicated to receiving and transmitting clock signals respectively. In conjunction with a suitable AMC like the AMC FMC Carrier Kintex (AFCK), clocks may be distributed between the boards inside a crate using the telecommunication clock lines. This allows composing advanced TFC topologies like a frequency-locked Multi-Master TFC crate.
Besides that, different VCXOs are provided on the PCB which can be adjusted from the FPGA side. Together with the bidirectional timing link this allows a precise timestamping approach similar to the one applied in White Rabbit systems.
Last but not least, the card can also be used at the TFC Slaves since one of its ports also offers the complete

functionality to lock a FPGA node to the TFC link.
In summary, the FMC card provides a versatile functionality which supports the rapid development and evaluation of a TP TFC system being integrated into an mTCA crate-based readout topology.

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