Tile Rear Extension Module for the Phase-I Upgrade of the ATLAS L1Calo PreProcessor System

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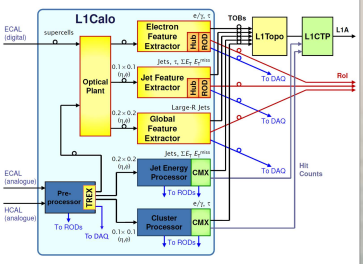
The ATLAS Level-1 Calorimeter Trigger (L1Calo)

- Hardware-based, pipelined system to identify high-p_T objects based on coarse-granularity analogue input from the ATLAS Liquid Argon (LAr) and Tile Calorimeters.
- Consists of three main subsystems:
  - **PreProcessor** (PPr)**:** receives, digitises and processes the analogue signals and transmits digital data, representing the transverse energy deposits (E_T) for the identified bunch-crossing (BC), to the subsequent processors.
  - **Cluster Processor** (CP)**:** identifies isolated clusters of electrons, photons, taus or hadrons.
  - **Jet/Energy-sum Processor** (JEP): identifies jets and computes the total and missing transverse energy.
- Transmits the results to the **Central Trigger Processor** (L1CTP) in approximately 2μs after the pp collision has occurred.

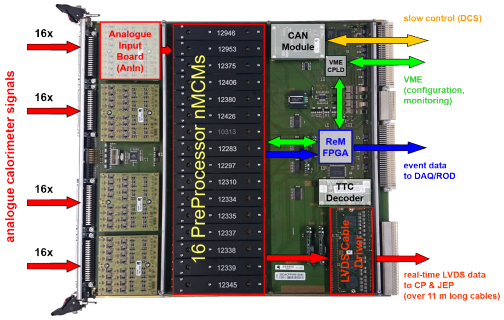


The L1Calo Phase-I Upgrade

- Additional finer-granularity digital input from LAr Calorimeter.
- New subsystems to process the digital input and to maintain the trigger performance at high LHC luminosity:
  - **Electron Feature Extractor** (eFEX): provides similar functionality to CP, but refined.
  - **Jet Feature Extractor** (jFEX)**:** provides similar functionality to JEP, but refined.
  - **Global Feature Extractor** (gFEX): identifies large jets.
- New module, **Tile Rear Extension** (TREX), in the PreProcessor to provide the Tile digitised results to the FEX processors as well as to CP and JEP.
- The part of PreProcessor that processes analogue signals from LAr, and the CP and JEP subsystems will be decommissioned after the performance of the FEX processors has been validated.
- Remaining PreProcessor will be replaced in Phase-II upgrade by a Tile digital pre-processing system.

The PreProcessor System

- Highly-parallel system with fast trigger-specific algorithms implemented in Field Programmable Gate Array (FPGA) based devices, to process **7168 analogue signals** from the entire ATLAS Calorimetry.
- Highly-modular system, consisting of **124** hardware-identical **PreProcessor Modules** (PPMs) organised into **8 VME crates**. The PPMs in two crates process analogue signals from the Tile Calorimeter, while the others process signals from the LAr Calorimeter.

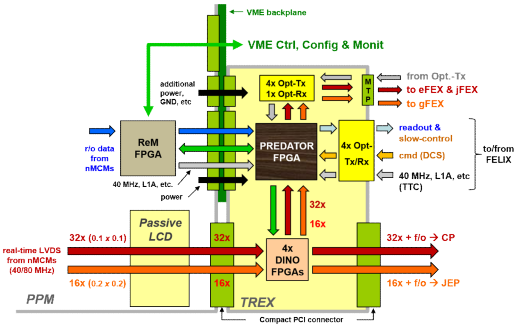


The PreProcessor Module

- Processes 64 analogue signals describing 0.1 x 0.1 ($\Delta\eta$ x $\Delta\varphi$) E_T deposits in calorimeters. The input signals arrive in differential form through the front-panel, while the digital energy results are sent as Low-Voltage Differential Signaling (LVDS) signals via parallel pair cables connected to the rear side.
- Is a 9U VME slave module, hosting:
  - **4 Analogue Input Boards** (AnIn) to convert the differential signal to single-ended and to map the input signals into the digitisation window.
  - **16 Multi-Chip Modules** (nMCMs), each of which processes 4 analogue calorimeter signals:
    - Digitisation with 10-bit resolution and sampling frequency of 40.08 MHz
    - Nanosecond phase-adjustment of digitisation strobes.
    - Coarse synchronisation of pulses originating from the same collision.
    - Dynamic, BC-wise pile-up suppression.
    - Identification of the E_T deposits per trigger channel and of the corresponding BC in time (FIR Filter and PeakFinder for pulses in linear range, dedicated algorithms for saturated pulses).
    - Separate noise suppression, pedestal subtraction and fine-calibration of the extracted E_T values for each destination processor (CP, JEP).
    - Re-ordering of the trigger cells to better utilise the bandwidth to the CP system (BC multiplexing).
    - Pre-summing of the four calibrated E_T values into a 0.2 x 0.2 jet element for the JEP system.
    - Pipelined event data readout for monitoring purposes.
    - Rate-metering and histogramming for trigger-independent monitoring purposes.
    - Transmission of digital energy results to CP and JEP as LVDS signals at a rate of 480 Mb/s.
  - **1 Readout Merger** (ReM) FPGA to configure, control and monitor the module over the VMEbus, and to transmit the event data to the ATLAS DAQ system via a rear-mounted G-Link Transmitter Module.
  - **1 TTC Decoder** card as interface to the ATLAS Timing, Trigger and Control system.
  - **1 CanBus** interface to send slow-control data to the ATLAS Detector Control System (DCS).
  - **1 LVDS Cable Driver** (LCD) card to transmit the digital energy results over up to 15m long cables to CP and JEP.

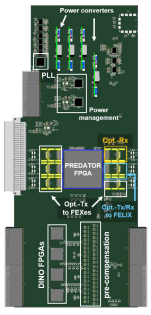
The Tile Rear Extension Module (TREX)

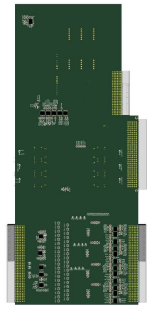
- **Rear transition module** in the two PreProcessor crates that process analogue signals from the Tile Calorimeter.
- Acts as a **physical extension of the PPM** in the corresponding crate slot, to:
  - Transmit the pre-processing digital results via optical links to the new FEX processors at 11.2 Gb/s (L1Calo baseline rate).
  - Maintain the legacy trigger path by sending the same digital results via parallel pair cables to the CP and JEP processors.
  - Collect and format the PPM event data and local slow-control data.
  - Interface via multi-Gb/s optical links to Front-End Link Exchange (FELIX) devices to transmit event data to DAQ and slow-control data to DCS, and to receive TTC information and DCS specific commands.
- Can handle double data rate input from the PPM (960 Mb/s). This mode will be enabled with an upgrade of the LCD card (passive LCD) and only after the CP and JEP have been decommissioned.
- Is connected to the VME crate controller via the ReM FPGA on the PPM for configuration, control and monitoring purposes.



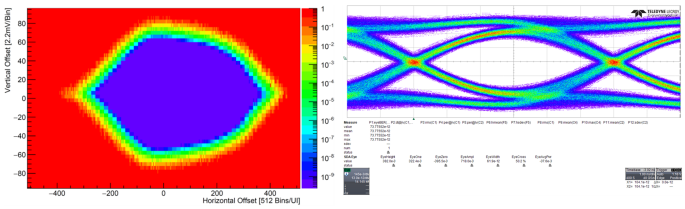
The TREX Prototype Module

- 18-layer, 150 mm x 366 mm PCB, hosting:
  - **4 Xilinx Artix-7 FPGAs** (XC7A35T-2CSG324C), called 'LVDS **D**ata **I**n-**O**ut' (DINO), to produce copies of the pre-processing results for the CP, JEP and FEX processors.
  - **pre-compensation circuit** to drive the signal copies for CP and JEP over long parallel pair cables.
  - **1 Xilinx Kintex UltraScale FPGA** (XCKU115-FLVF1924C), called '**Pr**eProcessor **Da**ta Collec**tor**' (PREDATOR), with 64 GTH Gigabit transceivers that support data rates up to 16.3 Gb/s. The PREDATOR FPGA performs most of the tasks assigned to the module:
    - Receive, format and transmit copies of the pre-processing results via 48 links to the FEX processors.
    - Receive and analyse pre-processing results via 12 links in loopback mode for diagnostic purposes.
    - Collect, format and transmit the PPM event data to DAQ and the local slow-control data to DCS via one link.
    - Receive and decode TTC information and DCS commands via one link.
    - Playback facility to test and debug all the high-speed interfaces.
    - Build local monitoring and status information and deliver it to VME.
  - **Four 12-channel Samtec FireFly optical transmitters** (ECUO-T12-14-030-0-1-1-2-01; 14 Gbps/channel) to send the pre-processing results to the FEX processors.
  - **One 12-channel Samtec FireFly optical receiver** (ECUO-R12-14-030-0-1-1-2-01; 14 Gbps/channel) to test the transmission over optical links in loopback mode for diagnostic purposes. The receiver will be removed in the next hardware iterations.
  - **One 4-channel Samtec FireFly Duplex Transceiver** (ECUO-B04-14-030-0-1-1-2-01; 14 Gbps/channel) to implement the bi-directional communication with the FELIX devices.
  - **One 10-channel PLL chip** (Si5345) to generate low-jitter clock pulses for the multi-Gb/s transmission and to supply the TREX and the PPM with 40.08 MHz based clock pulses in the absence of the TTC system in the laboratory environment.





- High-speed transmission tested with Kintex UltraScale based (XCKU040) development board:
  - optical transmission up to 10 Gb/s (using SFP+ optical transceivers)
  - electrical transmission up to 12.8 Gb/s (loopback mode on PCB)
  - **BER smaller than 10^{-13}** (using Xilinx integrated statistical eye tools and oscilloscope)



- First TREX prototype board is currently being manufactured.
- Intensive and thorough testing will be carried out at CERN, together with the FEX processors and the FELIX devices, in December 2016 and January 2017.
- Final design review is planned for spring 2017.
- Production readiness review and mass production expected in 2018.