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Tile Rear Extension Module for the Phase-I Upgrade of the ATLAS L1Calo PreProcessor System

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After the Phase-I ATLAS upgrade the Tile calorimeter will have to provide its data via fast optical links to the new Feature Extractor (FEX) modules of the L1Calo trigger system. In order to provide the FEXes with digitised Tile data, new Tile Rear Extension (TREX) modules need to be developed and installed in the existing L1Calo PreProcessor system. The TREX modules are highly complex PCBs, with state-of-the-art FPGAs and high-speed optical transmitters working at rates up to 14 Gbps. The prototype design of TREX and first corresponding test results will be presented.

Summary

The ATLAS Level-1 Calorimeter Trigger (L1Calo) is a hardware-based, pipelined system designed to identify high-pT objects based on coarse-granularity analogue input from the ATLAS Liquid Argon (LAr) and Tile Calorimeters. The L1Calo consists of three subsystems: the PreProcessor, to digitise the input signals and to extract a bunch-crossing-aligned transverse energy value from each pulse, and two object finding processors, the Cluster Processor and the Jet/Energy-sum Processor, which use as input the pre-processing results.

In the Phase-I upgrade, L1Calo will be extended with three subsystems to maintain the trigger performance at high LHC luminosity: the electromagnetic Feature Extractor (eFEX), the jet Feature Extractor (jFEX) and the global Feature Extractor (gFEX). The input to the FEXes is entirely digital. The LAr will directly provide the FEXes with digital trigger data via optical fibres. The Tile will continue to send analogue signals to the PreProcessor, which will then have to transmit the digital results to the FEXes.

The PreProcessor is a highly modular system consisting of 124 hardware-identical PreProcessor Modules (PPMs) organised into eight VME crates. The modules in two crates process analogue signals from the Tile, while the others process signals from the LAr. The PPMs receive the analogue signals through the front-panel and transmit the digital results via LVDS cables connected to the rear side.

In order to transfer the pre-processed Tile information to FEXes, Tile Rear Extension (TREX) modules will be developed and installed in the two crates processing Tile signals. Each TREX will act as a physical extension of the PPM in the corresponding crate slot, to transmit the real-time pre-processing results to the FEXes at a maximum rate of 11.2 Gbps via up to 48 high-speed optical links. Additionally, the TREX will have the tasks to provide a copy of the real-time data to the legacy L1Calo processors via 73 LVDS links, and to gather, format and transfer the PPM event data to the ATLAS DAQ system via additional optical links. For configuration, control, and monitoring purposes, the TREX will be connected to the computing infrastructure of the experiment via the PPM and the existing VME interface, while its operating conditions will be continuously monitored ßby the ATLAS Detector Control System.

The TREX will be based on the most recent PCB design technologies, FPGA devices and high-speed optical transmitters. The main challenge of the design will be to integrate a high density of components while maintaining the signal integrity required to achieve a bit error rate lower than 10ˆ(-14). In this contribution, the functionality and development of the board as well as initial test results will be presented.

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