A High Bandwidth and versatile Advanced Mezzanine Card

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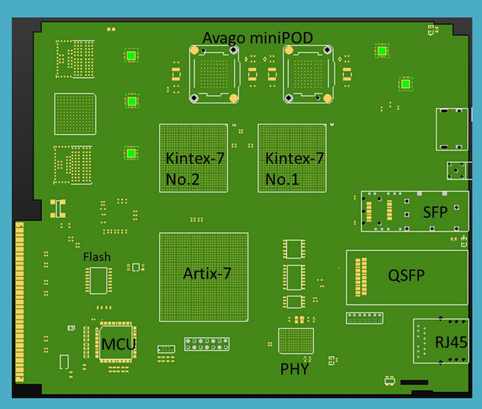
Motivation:

Nowadays, the trigger and data acquisition (TDAQ) system of many particle physics experiments always require larger data throughput, larger number of high speed I/Os and much more sophisticated trigger algorithms with longer latency. The micro-TCA and the ATCA standards, with their FPGA-based boards, respond to those requirements. Besides, Maintenance of the electronics may become an issue and it is therefore of interest to limit the use of many different custom-made electronics boards.

So it is significant to develop a high bandwidth and versatile board. On TWEPP 2015, we presented an AMC.0 based Trigger Receiver Board (TRB)[1,2]. This year we are developing a new TRB version with higher bandwidth on both front panel and backplane.



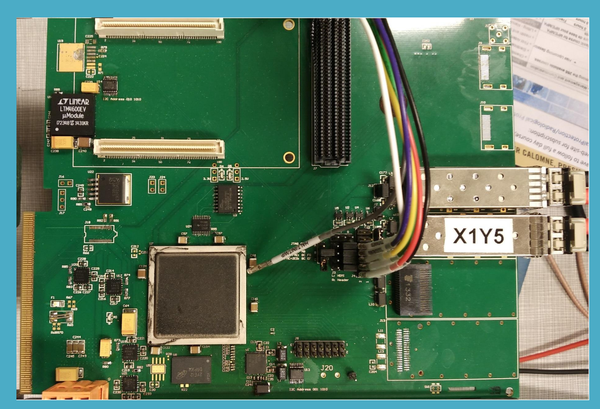
An external PHY chip is added to implement IPbus protocol [3] together with Artix-7.

TRB_v1:

- FPGAs: Artix-7 takes care of the board control, backplane connection and the optical links through SFP and QSFP. 2 Kintex-7s handle the optical links through Avago miniPOD and data processing.
- MMC: implemented on board with MCU, ATmega128.
- Optical links: 12 links through Avago miniPOD with line rate up to 10Gbps, 5 links through SFP and QSFP with line rate up to 6.6Gbps. 17 links in total.

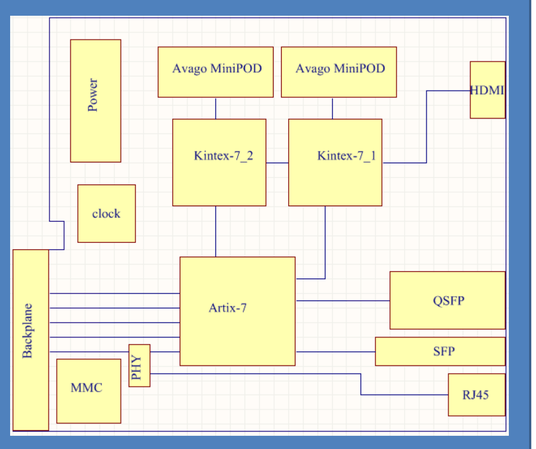
TRB_v0:

- FPGA: Artix-7 controls whole board, the front panel optical links and the backplane connection.
- MMC: implemented on mezzanine. The connector is compliant with CERN_MMC
- Optical links: 10 links through SFP and QSFP, each could run at 6.6Gbps.



Architecture

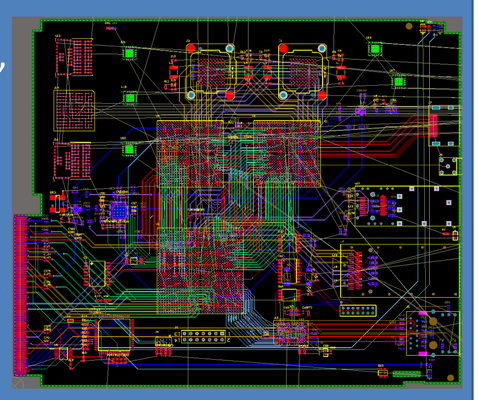
- FPGAs: Artix-7 uses XC7A200T-FFG1156 and Kintex-7s use XC7K160T-FFG676. The data from front panel goes into the Kintex-7s. After processing, it is sent to the Artix-7 through the interconnect between FPGAs.
- The backplane: high speed backplane connection is handled by Artix-7. GbE, PCIe and other user defined protocols can be used.



- Clock distribution: the CDCE62005 generates clean and accurate clock for FPGA, can ensure deterministic phase difference between input and output. System clock comes from an on-board 40MHz oscillator while a 125MHz oscillator generates the GbE clock.
- Optical links: Avago miniPOD is a 12 in 1 high speed transceiver, could run at 10Gbps. These 12 links are connected to Kintex-7 GTXs. 1 SFP and 1 QSFP are connected to Artix-7 GTPs. The maximum line rate of these 7 links is 6.6Gbps.
- The PHY chip: 88E1111. The GbE is implemented by Artix-7 + PHY. In stand alone mode, the RJ45 connector is used. While working in uTCA crate, the PHY can be configured to serial mode and connected to the backplane. This solution could also save 1 GTP.
- MMC: the MMC is integrated on board and uses exactly same devices with CERN_MMC so we could use the existing firmware and save time on MMC developments.

Interconnection

- 59 LVDS pairs and 1 GTX between Artix-7 and Kintex-7_1.
- 51 LVDS pairs and 1 GTX between Artix-7 and Kintex-7_2.
- 23 LVDS pairs and 1 GTX between Kintex-7_1 and Kintex-7_2.
- The HDMI is connected to Kintex-7_1.
- Backplane connection:
  - -Port 0 with the PHY chip, using GbE protocol.
  - -Port 1 with GTP to Artix-7, using GbE protocol when working with redundant MCH or as DAQ data path when working with the CMS AMC13 [4].
  - -Port 3 with LVDS to Artix-7, used as TTC path when working with AMC13.
  - -Port 4-7 & 8-11 with GTPs to Artix-7, using PCIe protocol or user defined protocols.



This AMC has high speed links to both MCH and redundant MCH in common option region and fat-pipes region. The LVDS links can run at about 800 Mbps, the GTP and GTX links can run at line rate up to 6.6 Gbps and 10Gbps respectively. This makes our board compatible with most microTCA crates (we are using a Vadatech VT892 crate, dual star topology).

Challenges

- Power distribution for 3 FPGAs: use separate power modules and power planes for large current parts.
- 10Gbps differential pairs' routing: make the lines short and keep the lines away from noisy devices.
- Hundreds of wires routing within 10 layers PCB stack.

Next steps

This board is currently under design and routing is almost complete. Special care will be put on the IPbus communication as we had problems with TRB_v0 (hardware bug). Since we gained experience with the IPbus firmware on a KC705 developing kit using the external PHY chip. Besides, we will try to implement GBT with all 17 optical links. The 12 links with 10Gbps line rate also have potential for future upgrade.

References:

1. J.Dong, *A High Bandwidth and versatile Advanced MC Board,* JINST proceeding, 26 February 2016.
2. PICMG AMC.0 R2.0, *Advanced Mezzanine Card Base Specification*, November 15 (2006).
3. IPbus firmware wiki page, https://svnweb.cern.ch/trac/cactus/wiki/IPbusFirmware.
4. E. Halzen et al., *The AMC13XG: a new generation clock/timing/DAQ module for CMS MicroTCA,* 2013 JINST 8 C12036