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A High Bandwidth and Versatile Advanced MC Board, TRB_v1

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We developed a new AMC board based on AMC.0, named as Trigger Receiver Board (TRB). TRB is a high bandwidth data-stream processor, using a Xilinx Artix-7 and 2 Kintex-7 FPGA. The Artix-7 takes care of the backplane connection while the Kintex-7s handle the front panel optical links. There are 17 optical links on the front panel, making a total bandwidth up to 150Gbps both in and out. On the backplane side, we implemented 2 Gigabit Ethernet and 8 multi-gigabit transceiver links connected to MCH and redundant MCH.

Summary

Nowadays many particle and nuclear physics experiments are planning to use the micro-TCA or the ATCA standards for their Trigger and Data Acquisition (TDAQ) system. In most of these experiments the first stages of the TDAQ system are based on FPGA-based hardware architecture to select events of interest and suppress background to an acceptable level for the DAQ system. Future projects or experiment upgrades always require larger data throughput, larger number of high speed (optical) Input/Output and much more sophisticated trigger algorithms with longer latency. The micro-TCA and the ATCA standards, with their FPGA-based boards, respond to those requirements. These experiments are also built to run over many years, even up to a couple of decades. Maintenance of the electronics may become an issue and it is therefore of interest to limit the use of many different custom-made electronics boards. Since a couple of years, several evaluation platforms or "generic"micro-TCA boards (AMC) have been introduced.

Last year we made a poster, introduced the prototype version, based on AMC.0 named as Trigger Receiver Board (TRB) version 0. In this contribution we will present the formal version TRB_v1. Compared to TRB_v0, TRB_v1 significantly increased the bandwidth and data processing ability.

TRB_v1 has 17 optical links on the front panel (1 pair Avago miniPOD, 1 QSFP and 1 SFP) which can receive data from front-end electronics system with bandwidth up to 150 Gbps. There are 2 gigabit Ethernet links and 8 multi-gigabit transceiver links communicating with the MCH and redundant MCH through backplane, building up the DAQ and slow control path.

Among the 3 FPGAs, there are hundreds high speed LVDS signals connected. The 2 Kintex-7s receive data and compress it, then send to the Artix-7. The high level algorithm running on Artix-7 will process the data and send to DAQ though the backplane.

In this contribution we will report the first performance results obtained with this new version and possible applications in particle physics experiments.

Primary author: DONG, Jianmeng (Universite Libre de Bruxelles (BE))

Co-authors: Prof. ROBERT, Frédéric (Université libre de Bruxelles); DE LENTDECKER, Gilles (Universite Libre de Bruxelles (BE)); YANG, Yifan (IIHE)

Presenter: YANG, Yifan (IIHE)

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