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A Prototype for an Artificial Retina Processor Aimed at Reconstructing Tracks at the LHC Crossing Rate

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We present the results for the prototype of a processor capable of reconstructing events in a silicon strip tracker at about 1 MHz rate with sub-microsecond latency. The processor is based on an advanced pattern-recognition algorithm, called "artificial retina", inspired to the vision system of the mammals. We design and implement this processor on a DAQ board designed to run at 1 MHz event rate. This is the first step towards a real-time track reconstruction system working at the nominal collision rate of LHC.

Summary

The goal of the "INFN-RETINA"R&D project is to develop and implement a parallel computational methodology that allows to reconstruct events with an extremely high number (>100) of charged-particle tracks in pixel and silicon strip detectors at 40 MHz, thus matching the requirements for processing LHC events in real time.

Our approach relies on a massively parallel pattern-recognition algorithm, dubbed "artificial retina", inspired by studies of the processing of visual images by the brain as it happens in nature. The artificial retina algorithm is based on two main concepts. First, for each track pattern we compute a quantity R that measures how any combination of entered hits matches the pattern itself. Second, the hit sequence delivered to a pattern is an appropriate subset of all the events hits, reducing the data bandwidth involved in the process. Preliminary studies on simulation already showed that high-quality tracking in large detectors is possible with sub-microsecond latencies when this algorithm is implemented in modern, high-speed, high-bandwidth FPGA devices, opening a possibility of making track reconstruction happen transparently as part of the detector readout.

As first step, we design a sizable prototype of a tracking processor using a 6-layer silicon detector as model. The detailed geometry and charged-particle hits of this detector are used to assess the processor performances. The algorithm simulation shows that tracks can be reconstructed in this detector using with a track-parameter matrix with only 3,000 patterns.

In order to demonstrate that a track-processing system based on the retina algorithm is feasible, we build the designed prototype, fitting the whole system on 8 currently-used readout boards, each equipped with 4 Altera Stratix III FPGA's. Four boards, corresponding to 16 FPGA's, are used to implement the delivering of proper hit sequences to the next step, receiving as input data separately from each readout module of the detector. All the chips in each board are interconnected between them in a full-mesh configuration, in order to be able to deliver sequences containing hits from all the layers. The other 4 boards are used to implement the computation of R for 3,000 patterns. Each chip contains a pattern sub-matrix, where a search for local maxima is performed for each event.

All the processing steps were implemented successfully on the FPGA's at the nominal clock frequency of the board (160 MHz). We test the whole processing chain providing hit sequences as input, and correct parameters for reconstructed tracks were received on the output. Assuming hit sequences from real events that include background and noise, data can be processed at a 1.8-MHz event rate, using boards that had originally been designed for a 1-MHz readout-only functionality.

Finally, we report on the scalability prospects of this track processor to larger detector systems and to higher event rates.

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