A Neural Network on FPGAs for the z-Vertex Track Trigger in Belle II

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1. Belle II CDC z-Vertex Trigger

Goal for Belle II: Rejection of events originating outside of z=0 at the 1st level

Requirements
- Rejection of data to be made within 500 ns
- Spatial resolution of the z-Vertex to be within 2 cm

Approach
- Prediction of an event’s z-Vertex using data from the CDC as input
- Decision made on FPGAs close to the readout

2. Neural Network for Trigger

- Neural networks used to predict z-Vertex of an event
- Even with background the achieved resolution is within the desired range
- Feed-Forward Multi Layer Perceptrons used for prediction
- Trained with rprop algorithm from FANN

3. Basic Setup

- Missing Hits
  - Networks perform worse in case CDC SuperLayers do not record a Hit
  - Specialized networks trained for compensating missing hits in stereo layers

- Sectorization
  - Number of inputs for whole CDC not feasible for one network
  - Sectorization of CDC for reduction of number of inputs
  - Different MLPs for each sector

4. Input Calculation for MLP

One Hit for each of the 9 SuperLayers of the CDC is selected and processed

3 Inputs are calculated for each Hit
- Crossing Angle of 2D-Track
- Drift Time of segment hit
- Delta ID: Distance between wire of the hit and 2D-Track

5. Hardware Architecture of z-Vertex Trigger

Pipelined architecture for processing of CDC data and prediction of z-Vertex

Architecture consists of three major parts
- Input handling capturing data from CDC trigger system
- Preprocessing calculating the MLP inputs
- Neural network calculating the prediction of the z-Vertex

6. Latency and Resource Consumption

Implementation of z-Vertex Trigger on UT3 using a Virtex 6 HX565T

<table>
<thead>
<tr>
<th>Metric</th>
<th>Slices</th>
<th>DSPs</th>
<th>BRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Utilization</td>
<td>48%</td>
<td>90%</td>
<td>57%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module</th>
<th>Frequency</th>
<th>Latency in cycles</th>
<th>Latency in ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>MLP</td>
<td>205.4 MHz</td>
<td>10</td>
<td>50</td>
</tr>
<tr>
<td>Preprocessing</td>
<td>232 MHz</td>
<td>10</td>
<td>50</td>
</tr>
<tr>
<td>Total</td>
<td>200 MHz</td>
<td>20 Cycles</td>
<td>100 ns</td>
</tr>
</tbody>
</table>

7. Summary and Outlook

- Prediction of z-Vertex on FPGAs using neural networks
- Current Implementation of the z-Vertex Trigger meets latency, resource and resolution requirements
- Upgrade possibilities using 3D-Finder as Preprocessing
- Integration into full CDC trigger system