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A Neural Network on FPGAs for the z-Vertex Track Trigger in Belle II

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Background originating from events outside of the interaction point is going to play a major role in the upcoming Belle II experiment. In order to reduce this background a track trigger based on the reconstruction of an event's z position is employed on FPGAs. This paper presents the architecture and implementation of neural networks and supporting preprocessing that is going to be used at the upcoming cosmic ray test of Belle II. Using hit information from simulations figures of merit like latency, accuracy and resource demand are presented.

Summary

The upgraded SuperKEKB collider is designed to achieve a luminosity of $\mathcal{L} = 8 \times 10^{35} cm^{-2} s^{-1}$. This will lead to more machine background at the upcoming Belle II experiment, located at SuperKEKB, in comparison to its predecessor. Hereby background originating from events outside the interaction point is a major concern.

To reduce this background a track trigger based on neural networks is implemented on FPGAs. These networks are reconstructing the z (longitudinal) position of the event vertex, which is then used for background reduction. It uses the hit information from the Central Drift Chamber (CDC) of Belle II to estimate the z-vertex without explicit track reconstruction. Additional preprocessing is based on the track information provided by the standard CDC trigger.

An implementation of neural networks has to stay within the constraints of the Trigger. The reconstruction has to be completed within $1 \mu s$, meanwhile it has to be ensured that the limited resources available on the used FPGA are not exceeded. Additionally a sufficient resolution for the vertex reconstruction has to be achieved on the FPGA. The effects of using fixpoint calculation have to be carefully considered for this.

This paper presents the architecture and implementation of neural networks that are designed to be used in the upcoming cosmic ray test of Belle II. They're supplemented by custom preprocessing algorithms, transforming input data from the central drift chamber of Belle II into a suitable representation.

The presented architecture encompasses two layers of neurons totaling 83 neurons that are executed in parallel. Since the input data arrival frequency is much slower than the achievable clock frequency for the network, processing of the inputs is pipelined and time multiplexed for each neuron. This allows staying within the available resources of the FPGA, especially multipliers, while still achieving the demanded latency. Bit widths used for the data within the network are selected to achieve the best trade-off between accuracy of the implementation's calculation and resource consumption.

Evaluation of the presented architecture for neural networks is conducted by using hit information from the CDC derived from simulations. Figures of merit like latency, accuracy and resource demand are presented using this data.

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