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FPGA Based Algorithms for the New Trigger System for the Phase 2 Upgrade of the CMS Drift Tubes Detector

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The Phase 2 upgrade of the CMS Drift Tubes detector aims at moving all the readout and trigger electronics from the inner detector to outside the cavern. Trigger algorithms need to be redesigned to handle direct timing information and remove present bottlenecks of resolution and deadtime, approaching to present high level trigger performance. In the present contribution we describe the work that has been performed to emulate the firmware that process 1 ns TDC hits from one DT chamber with the combinatorial problematic of the arrival time uncertainty in a detector with up to 400 ns of drift time.

Summary

A fundamental task of the CMS (Compact Muon Solenoid) detector is its ability to trigger on and reconstruct muon tracks at high luminosities. This task is performed by various detectors, among them, the DT (Drift Tube) chambers, and maintaining this capability is fundamental during the HL-LHC (High Luminosity LHC) era.

DT Chambers are made of three super layers each consisting of four layers of rectangular drift tube cells, staggered half-width. When a charged particle crosses one cell, it ionizes the gas and the electrons drift at constant velocity to the anode wire. Accordingly, there is a linear relation between the time measurement of the incoming signals (hit) and the muon track position. Due to the particular cell's arrangement it's possible to use that time from, at least, 3 cells to apply a mean-timer algorithm to calculate track angle and chamber crossing point and the LHC beam bunch-crossing to which muon hits belong to.

DT electronics will be redesigned due to radiation and maintenance constrains. The new electronics will substitute present on detector electronics with a simplified system in charge of hit time measurement and optical transmission. All the trigger algorithms will be implemented in the FPGA-based back end electronics, which will produce trigger primitives. This new system will allow to improve the hit resolution used in the DT trigger and reduce the single hit dead-time.

In this contribution we present the hardware oriented software algorithm that has been developed in C++ to validate the implementation of the mean-timer paradigm based on the foreseen architecture of the future electronics. The algorithm developed is capable of building muon trajectories and reject background signals producing trigger primitives with bunch crossing identification. Moreover, it also gives a quality level to each accepted track.

In order to be easily translated into a firmware code, its internal architecture is distributed in a parallel way, using software-processing threads, imitating the intrinsic FPGA parallel behaviour. Syntactically complex expressions difficult to be converted into VHDL code have also been avoided. To simulate variations in the arrival time of incoming DT hits, C++ classes working as FIFOs, ring buffers, etc, ⋯have been implemented.

The algorithm needs to reproduce the expected system hardware and thus it is responsible of unmixing groups of hits received from each optical link and rearrange them into candidate packages. This unmixing and mixing procedure is one of the main challenges of the proposed architecture, because it can easily grow into a exponential combinatorial explosion. It is important to note that the maximum cell drift time is 400 ns and the bunch crossing separation is 25 ns, so hits need to be stored for a significant amount of time and combined with a possible large number of signals which are received for the duration of the drift time.

The algorithm has been validated with muon candidates, demonstrating good agreement with the generated data, being able to reconstruct bunch crossing, angle and position with good precision.

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