Contribution ID: **159**   Type: **Poster**

Performance and Advantages of a Soft-Core Based Parallel Architecture for Energy Peak Detection in the Calorimeter Level 0 Trigger for the NA62 Experiment at CERN

Tuesday 27 September 2016 18:18 (1 minute)

The NA62 experiment at CERN SPS has began its data-taking. Its main topic is to reduce uncertainties in the branching ratio of the ultra-rare decay $K^+ \rightarrow \pi^+ \ \nu \ \bar{\nu}$. In this context rejecting the background is a crucial topic. The Cal-l0 trigger get energy deposit from the calorimeters to suppress decays with π^0 and muons in the final state. In this work we present the performance of a soft-core based parallel architecture build on FPGAs for the energy peak reconstruction as an alternative to an implementation completely founded on VHDL language.

Summary

The NA62 experiment at CERN has began this year the data-taking phase scheduled until the next accelerator's second long shutdown in 2018 . The experiment was designed to check the validity of the Standard Model in the region of most suppresed processes involving flavour-changing neutral currents (FCNCs). In particular its main topic is to improve the precision in measuring the branching ration of the ultra-rare decay $K^+ \rightarrow \pi^+ \ \nu \ \bar{\nu}$ using a detectors ensemble to identify and tracks the particles. Among the others detectors involved, several electromagnetic calorimeters are used to suppress the background related to decay $K^+ \rightarrow \pi^+\pi^0$ while the background with muons in the final state is suppressed by a set of 3 hadronic calorimeters . This work focuses on the calorimenters level 0 trigger (Cal-l0) that works on three electromagnetic calorimeters (the Liquid Kripton (LKr), the Small Angle (SAC) and the Intermediate Ring (IRC)), and two hadronic calorimeters (MUV1 and MUV2). The Cal-l0 is a sequence of three connected layers. The first layer, made of 29 electronic boards, collects the data coming from the calorimeters and detects the energy peak underlying parametrized constrains. Most of the first layer, 28 boards each one corresponding to a vertical slice of the Lkr calorimeter, sends detected peaks to the second layer. It is made of 7 boards, each one merges information coming from 4 Lkr slices and send the aggregated information to the last level. The third layer aggregates all the information received from the second layer and from the IRC, SAC, MUV1, MUV2 board and sends it to the central level 0 trigger processor. In particular we preset the performances of the peak detection implemented in the firmware using only the VHDL language, as it is now, compared to those one of a parallel architecture of soft-core processor implemented on FPGAs. This solution adds flexibility and simplify the algorithm implementation because of the use of C language to program the soft-core processors and takes advantage of digital signal processing (DSP) blocks available on last generation FPGAs.

Primary authors: FUCCI, Adolfo (Universita e INFN Roma Tor Vergata (IT)); SALAMON, Andrea (Universita e INFN Roma Tor Vergata (IT)); Prof. SARGENI, Fausto (Università e INFN Roma Tor Vergata (IT)); FEDERICI, Luca (Universita e INFN Roma Tor Vergata (IT)); DE SIMONE, Nico (Universita e INFN Roma Tor Vergata (IT)); Prof. BONAIUTO, Vincenzo (Universita e INFN Roma Tor Vergata (IT))

Presenter: FEDERICI, Luca (Universita e INFN Roma Tor Vergata (IT))

Session Classification: POSTER

Track Classification: Trigger