Development of Network Interface Cards for TRIDAQ Systems with the NaNet Framework

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Abstract
NaNet is a framework for the development of FPGA-based PCI Express (PCIe) Network Interface Cards (NICs) with real-time data transport architecture that can be effectively employed in TRIDAQ systems. Key features of the architecture are the flexibility in the configuration of the number and kind of the I/O channels, the hardware offloading of the network protocols stack, the stream processing and the zero-copy RDMA (for both CPU and GPU) capabilities. Three NIC designs have been developed with the NaNet framework for the CERN NA62 L0 trigger and for the KM3NeT-IT underwater neutrino telescope DAQ system.

NaNet Design

- **I/O Interface**
  - Multiple link
  - Multiple network protocols
    - Ethernet: 1Gbe, 10Gbe
    - Custom APE/Link (24g sp, SFP+, XGMII link)
- **Router**
  - Dynamically interconnects I/O and NIC ports
  - Network Interface
    - Manages packets TX/RX from and to CPU/GPU memory
    - TLB & Nios II Microcontroller
    - Virtual memory management
- **PCIe X8 Gen2 Core**
  - CPU: 2.8 GHz/Read ~ 2.5 Gb/s Write
  - GPU: 2.5 Gb/s Read & Write
  - Finalizing PCIe X8 Gen3 Core
- **GPUDirect** P2P/RDMA
  - GPUDirect allows direct data exchange on the PCIe bus with no CPU involvement (zero copy)
  - -> Latency reduction for small messages

NaNet Software

- Host
  - User Space Application
  - User space Library (Open/Close, CLOP management, …)
- Linux Kernel Device Driver
- NaNet Device
  - Nios II Microcontroller: single-process software (bare metal) performing system configuration & initialization tasks

Case Study: NA62 RICH Detector

Ring-imaging Cerenkov detector
- Pion-Muon discrimination
- 70 ps time resolution
- 10 MHz event rate
- 20 photons detected on average per single event (hits from photo-detectors)
- 40 Byte per event

- 4 TEL2 for RICH detector
  - 8x1GbE links for data/o
  - 4xXGe trigger primitives
  - 4xXGe GPU trigger
  - Events rate: 10 MHz
  - L0 trigger rate: 1 MHz
  - Max Latency: 1 ms

NaNet-10 (four 10GbE SFP+ Ports)

- ALTERA Stratix V Terasic DES-5NET dev board
- 4 SFP+ ports (Link speed up to 10 Gb/s)
- PCIe X8 Gen2/3
- GPUDirect P2P/RDMA capability
- UDP offload support
- Real-time decommressing and event merging capability
- Planned 40GbE development

Results

- Ring reconstruction on GPU
  - XY plane divided into a grid
  - An histogram is created with distances from these points and hits on the physics event
  - Rings are identified looking at distance bins whose contents exceed a threshold value

Synthetic tests

- Test bed:
  - Supercmos X909-30-888 HF Intel C602/Intel Xeon E5-2650 2.6 GHz DDR3 8 Gb nVIDIA K20X
  - 1Gbe NIC – switch → NaNet10 for latency measurements
  - 10Gbe NIC – NaNet10 for bandwidth

**Preliminary results**

- Supercom X909-30-888 HF Intel C602
  - Intel Xeon E5-2662 2.0 GHz 32 GB DDR3 nVIDIA K20X
  - ~25% target beam intensity (910^10 Pps)
  - 1/16 downsampling factor
  - 8 CLOP each 32 kB
  - Timeout on data collection prior to ring reconstruction: 350 μs

**NA62 2016 Run**

- Experimental results
  - Supercom X909-30-888 HF Intel C602
  - Intel Xeon E5-2662 2.0 GHz 32 GB DDR3 nVIDIA K20X
  - ~25% target beam intensity (910^10 Pps)
  - 1/16 downsampling factor
  - 8 CLOP each 32 kB
  - Timeout on data collection prior to ring reconstruction: 350 μs

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- NaNet coordinators: Alessandro Lonardo (alessandro.lonardo@roma1.infn.it)

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