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Readout and Trigger for the AFP Detector at ATLAS Experiment

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AFP, the ATLAS Forward Proton consists of silicon detectors at 205 m and 217 m on each side of ATLAS. In 2016 two detectors in one side were installed. The FEI4 chips are read at 160 Mbps over the optical fibers. The DAQ system uses a FPGA board with Artix chip and a mezzanine card with RCE data processing module based on a Zynq chip with ARM processor running Linux.
In this contribution we give an overview of the AFP detector with the commissioning steps taken to integrate with the ATLAS TDAQ. Furthermore first performance results are presented.

Summary

The ATLAS Forward Proton detector aims to measure the transfer momentum and energy loss of very forward protons colliding in the ATLAS interaction point. For this purpose, the detector consists of two Roman Pots per ATLAS side at 205m and 217m from
the IP, each of them containing a 3D silicon tracker and a time-of-flight
detector in the far stations.

A first stage of installation took place during the LHC shutdown
of 2015-2016. In that period, the two Roman Pot stations on one side
were installed, together with a silicon tracker in each station
(AFP0+2) in February 2016. Functional TDAQ integration with the ALTAS
experiment was achieved in May of the same year, during LHC's luminosity
ramp-up. During 40h of common run with ATLAS AFP TDAQ collected more than
20pb-1 when detectors were inserted at 20 sigma from the beams. At
the same time, the detector commissioning took place. The
installation of the full AFP detector is planned to be completed during
the next shutdown (2016-2017).

The silicon detectors are bump-bonded to the FE-I4 readout chip, which is
read-out with a FPGA board based on a Xilinx Artix chip, HSIO-2, and a
mezzanine card that plugs into this board. The mezzanine card contains a
RCE data processing module based on a Xilinx Zynq chip.
The software for calibration and monitoring of the AFP detectors runs on the ARM processor of the Zynq under ArchLinux. The RCE communicates with the ATLAS Run Control software. Commands are transmitted from RCE to an optoboard over 200m of optical cable and then sent to each module via 8m of electrical twisted pair cable.

The trigger signal is obtained with the HitOr signal from each of the FE-
I4 modules, which consist in a logical OR of the signals of all the
columns in the detector. The length of the HitOr signal depends on the
deposited charge in the silicon and the tuning parameters, and can span
over several bunch crossings. Those signals are then sent to the Local
Trigger Board (LTB) mounted at the station with the Hitbus chip. The
Hitbus chip has 3 input channels for selectable trigger logic. The best
three detectors of each station were chosen to contribute to the trigger.

A majority vote logic was selected to reduce the time walk while minimising noise. The output of the Hitbus chip is a CMOS signal, which is then sent to a CMOS/NIM driver installed on the LTB and then sent over 260m of air-core coaxial cable to the Central Trigger Processor rack located underground. The signals from two stations enter discriminator, where the length is shortened down to 23ns. The 23ns NIM trigger signal is then fed into the ATLAS LV1 standard trigger system at the longest acceptable latency for configuration used in the high luminosity runs. Copies of the discriminated signals are also sent to the AFP local trigger electronics and used in standalone calibration runs.

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