Contribution ID: **135** Type: **Poster**

Study of Hardware Implementation of Fast Tracking Algorithms

Tuesday, 27 September 2016 18:25 (1 minute)

Real-time track reconstruction at high event rates is a major challenge for future experiments in high energy physics. To perform pattern-recognition and/or track fitting, artificial retina or Hough transformation have been introduced in the field which have to be implemented in the FPGA firmware.
In this contribution, we will report on a possible FPGA hardware implementation of retina algorithm based on the Floating-Point Operator IP. Detailed measurements with the algorithm are investigated. Retina performances and capabilities of the FPGA are discussed along with perspectives for further optimizations and for future applications.

Summary

The artificial retina tracking algorithm based on the vision mechanism in mammals, is a possible solution for fast, massively parallel, track reconstruction. The vision mechanism is able to process the huge amount of data collected from the environment, using neurons to recognize specific patterns in the acquired images. Similarly, this retina algorithm can recognize specific track characteristics from a multilayer detector data flow, comparing the detector hits with stored patterns (discrete parameter space), processing exponential function, performing weighed sum of the “distance” of the track from the patterns (engine) and identify local maxima response among different patterns. Our approach follows the current trends of industry using high-speed, high-bandwidth FPGA devices. Fast tracking algorithm in a realistic FPGA architecture poses two technical challenges: (1) LUTs are able to be used for the calculation of the distance and the exponential function. This kind of efficient implementation costs lower latency, more logic resources and limitation of data precision. (2) It is very convenient to use Floating–Point Operator IP for exponential function in real time track finding. The IP core provides arithmetic operators that can be targeted to any of the latest Xilinx FPGA. We developed retina algorithm based on the Floating–Point Operator IP with AXI4-stream interface. In order to test the implementation of the algorithm, a series of detailed measurements were taken. We also compared pure logic implementation with the use of DSP blocks. In both schemes, the measurements were performed with a mass of engines computing in parallel. Then we compared the total latency and resources of retina in various system clocks. Moreover retina was also tested on different hardware platforms including Arduino and Kintex-7. We focus the study on the possibility of retina algorithm implementation and optimization between latency and resources. From above, retina is based on a massively parallel calculation and suitable for implementation in FPGAs with a pipelined architecture. The algorithm is very flexible in terms of calculation process and latency so that better performance can be achieved. These results are encouraging and represent a first step towards the development of a fast efficient track-fitting system for applications in future experiments at high luminosity. However in real experiments, the geometry of the detector and the topology of the events may be quite complicated. And in some cases the Hough transformation seems more adequate. This aspect will also be discussed.

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Session Classification: POSTER

Track Classification: Trigger