Rad-hard DCDC converters for HL-LHC experiment's tracker modules power distribution

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TWEPP, 30 September 2016

The rad-hard DC/DC converters ASICs for LHC experiments upgrade

5-12 V to 0.6-5 V
Iout ≤ 4 A

FEAST2

ASICs and modules in production

30,000 ASICs and 20,000 modules are being provided to the experiments

upFEAST

"upgraded FEAST": increased displacement damage tolerance for tracker applications

A fully functional prototype is already existing

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2-2.5 V to 0.6-1.5 V
Iout ≤ 3 A

DCDC2S

First prototype almost ready for testing

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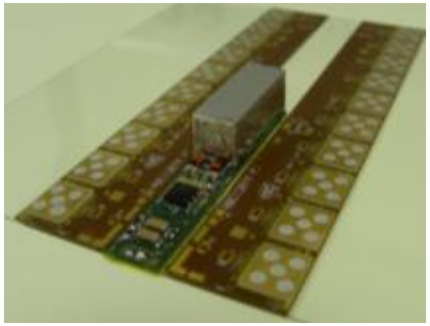
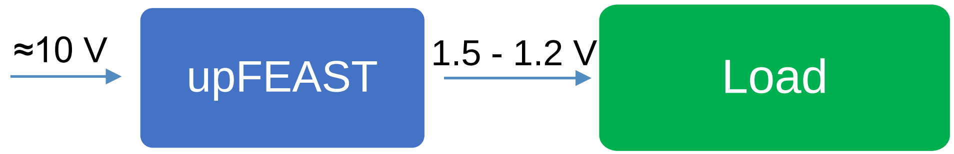
DCDC2S

First prototype almost ready for testing

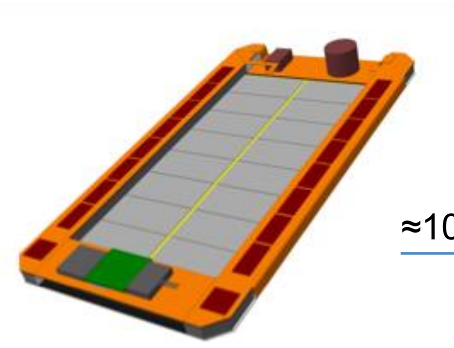
Efficient power distribution and material budget minimization in HL-LHC trackers require new DC/DC converters. Custom integration needed!

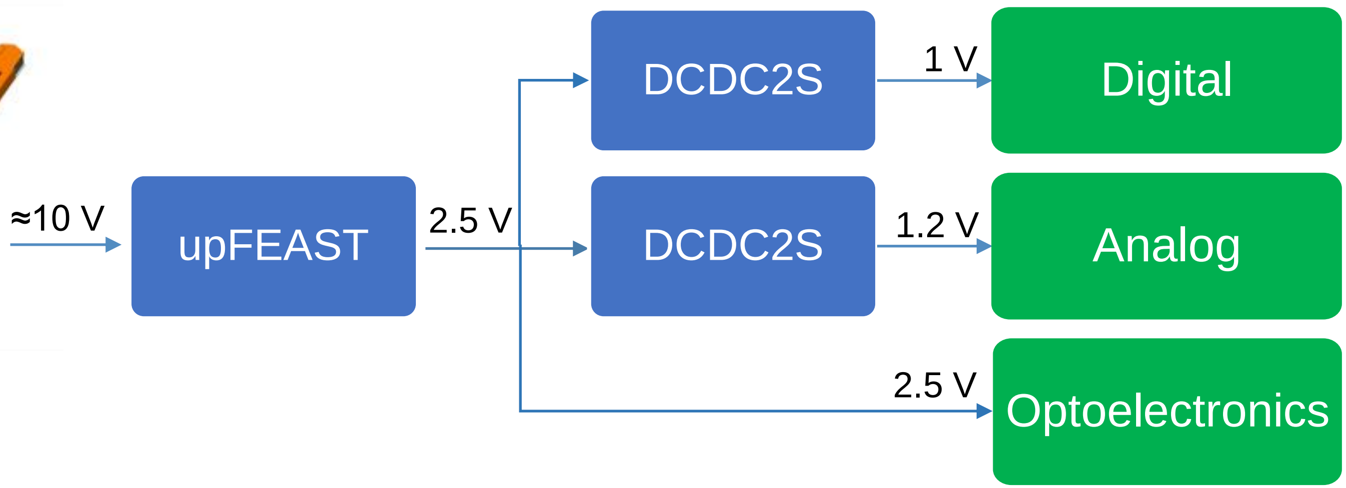
ATLAS ITK





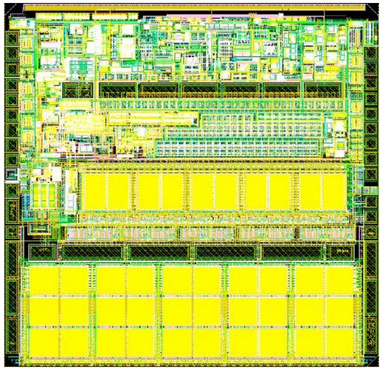
CMS PS Module





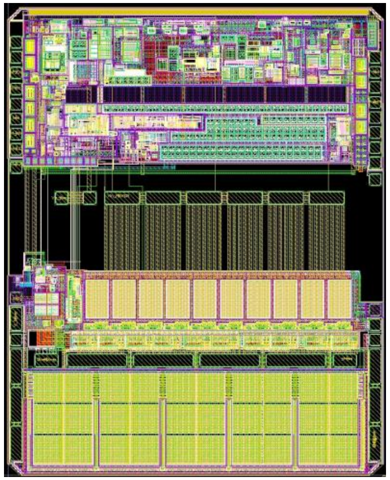
upFEAST is the result of the migration of FEAST2 design into a 'sister' technology (0.35 μm) that can stand much higher fluence

FEAST2

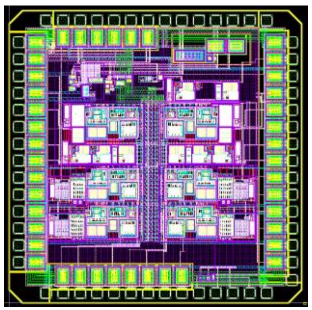


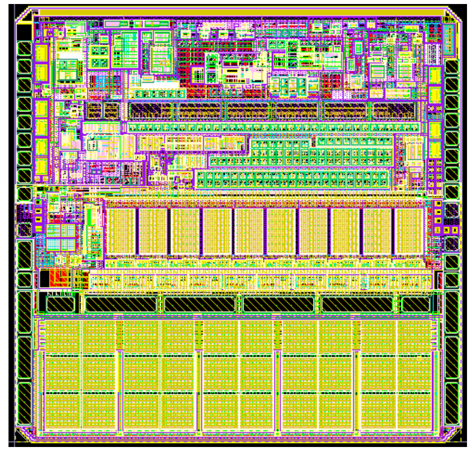
Displacement damage tolerance
$< 5 \cdot 10^{14}$ n/cm^2

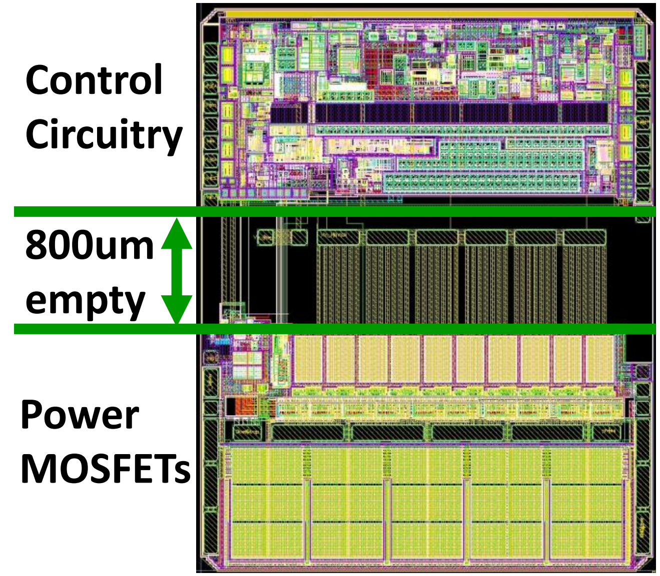
upFEAST



Displacement damage tolerance
$> 5 \cdot 10^{15}$ n/cm^2







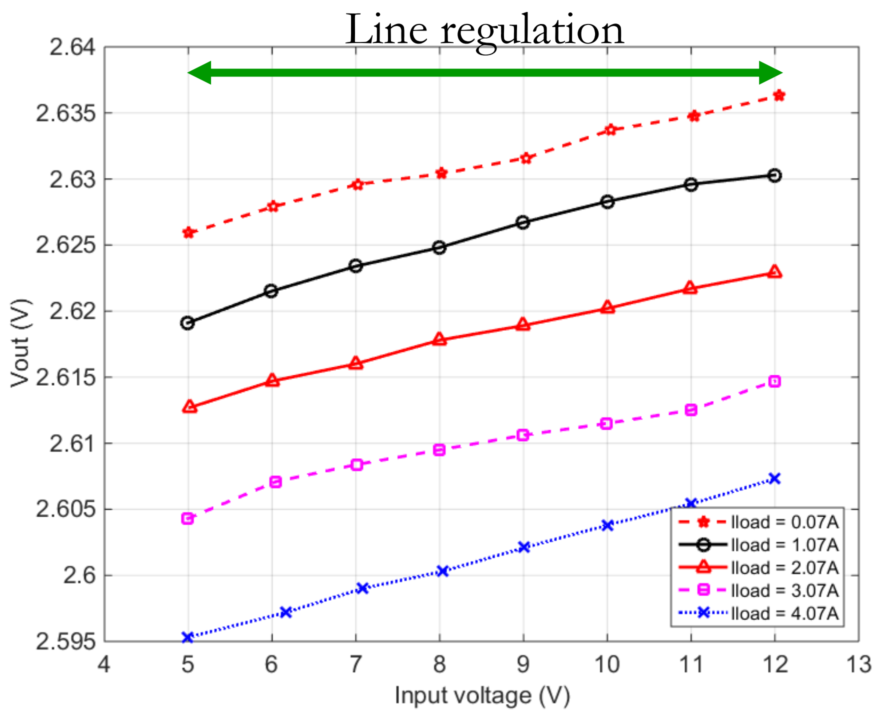
Test chip with the critical blocks for DD hardness (bandgap, linear regulator)

DD: $5 \cdot 10^{15}$ n/cm^2

upFEAST:
Substrate noise issues
(different buried layers compared to the previous technology)

upFEAST2:
800 μm introduced between power transistors and control + backthinning for lower substrate noise coupling

upFEAST2
pre-irradiation behavior



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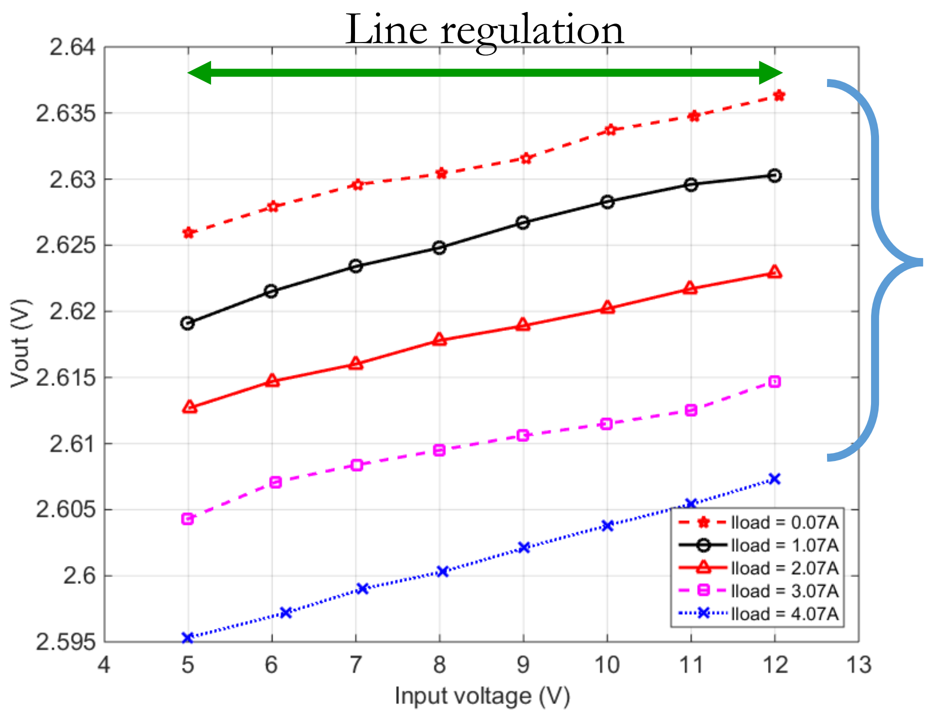
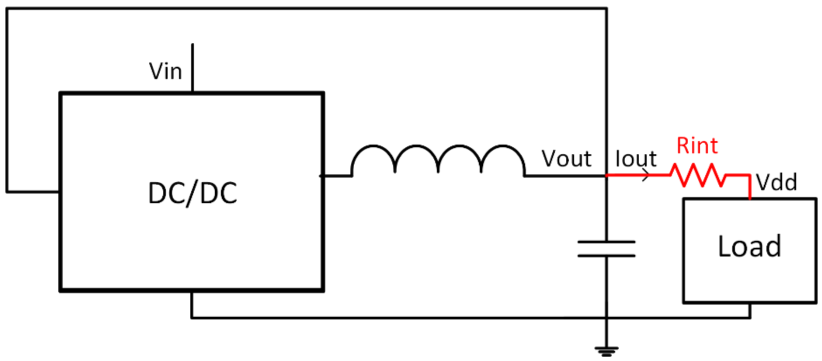
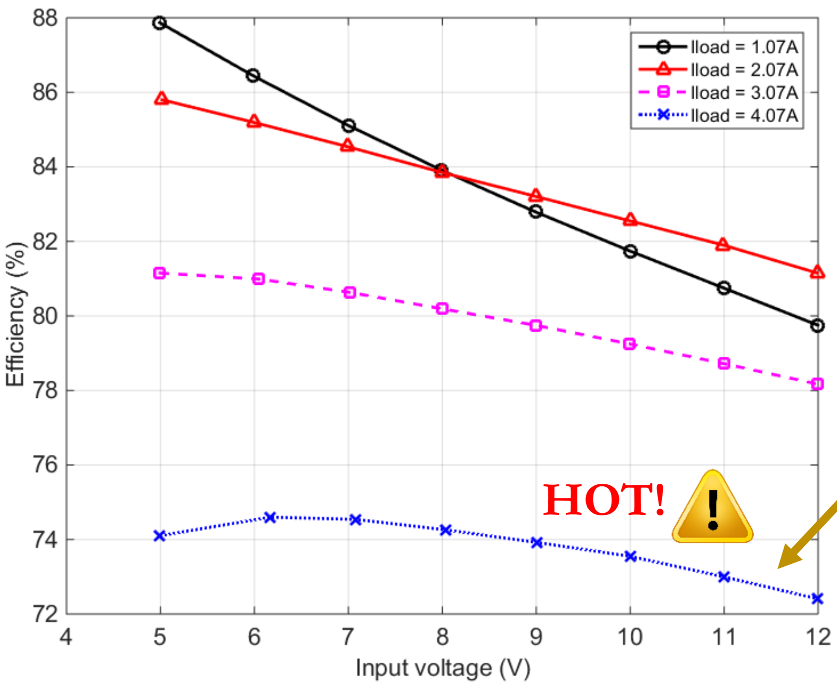


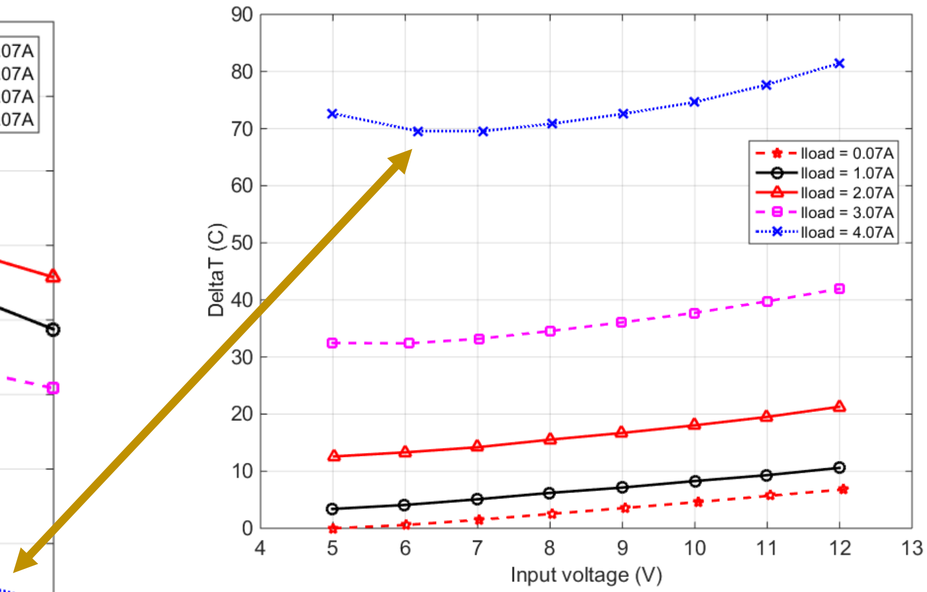


The interconnections are critical to minimize $\frac{dVdd}{dIout}$

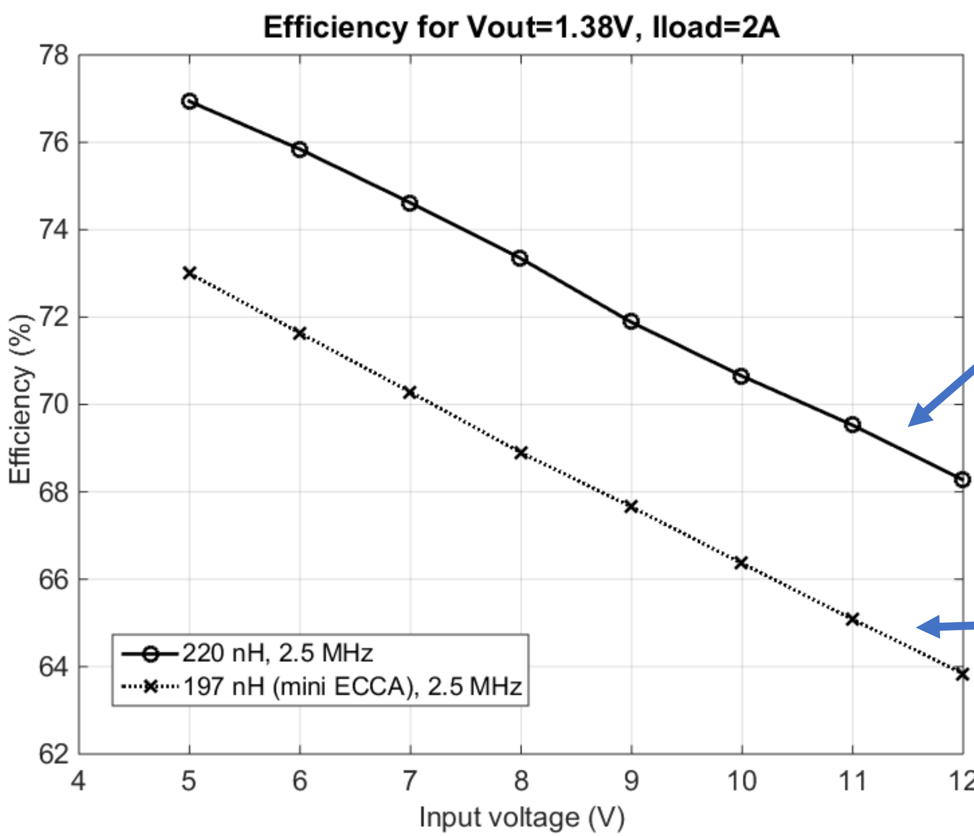
upFEAST2
pre-irradiation behavior: Efficiency

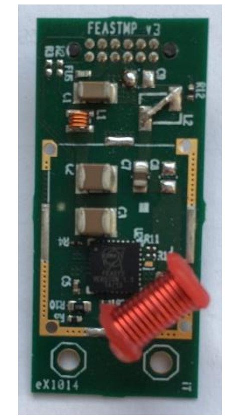
Efficiency for Vout=2.6V





The details of the integration (choice of the inductance and of the switching frequency) will determine the efficiency



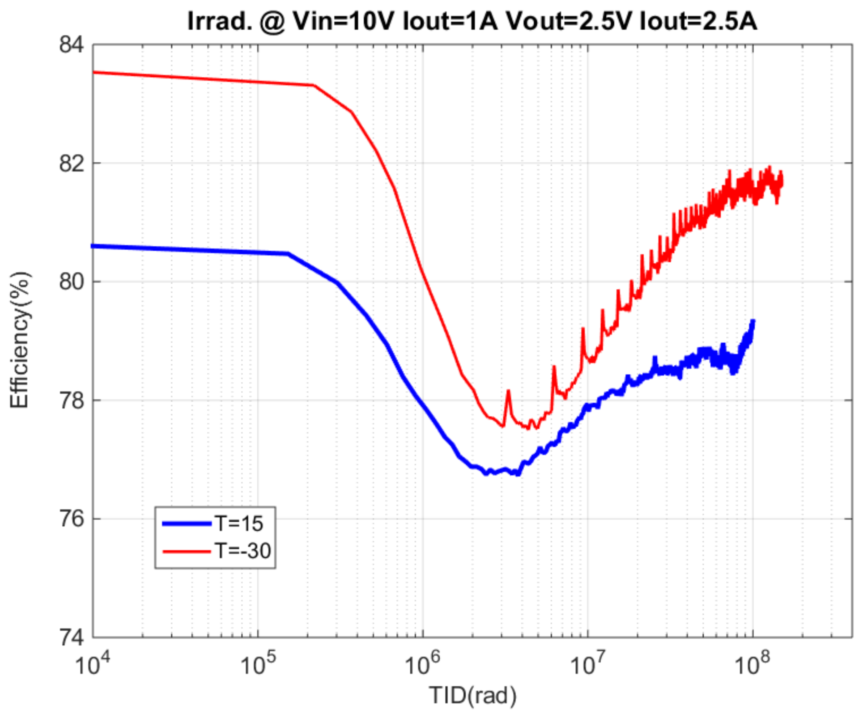


L = 220 nH

Cu volume > 50 mm^3

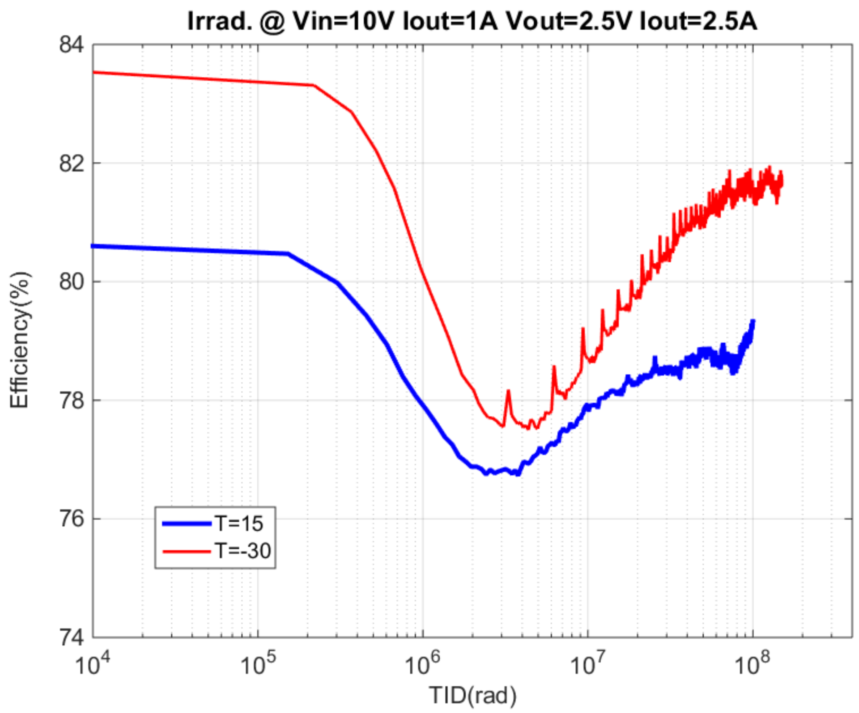
L = 197 nH

Cu equivalent volume: 7.1 mm^3



Efficiency with TID is degraded mainly because of the leakage current in power NMOS, which is independent from the load

Lower degradation at **higher power, lower dose rate, higher temperature**



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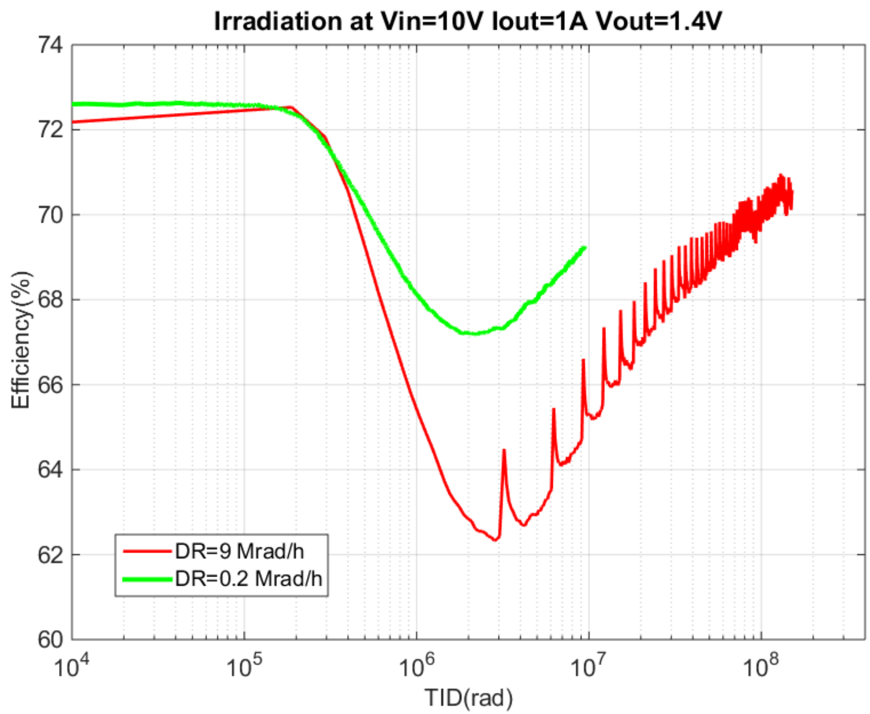
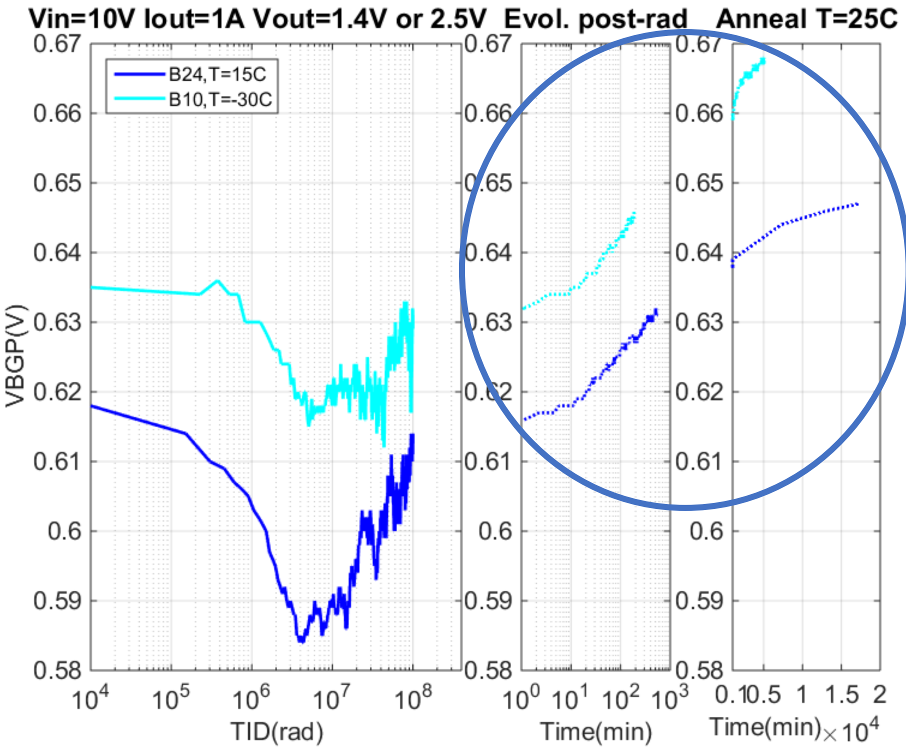
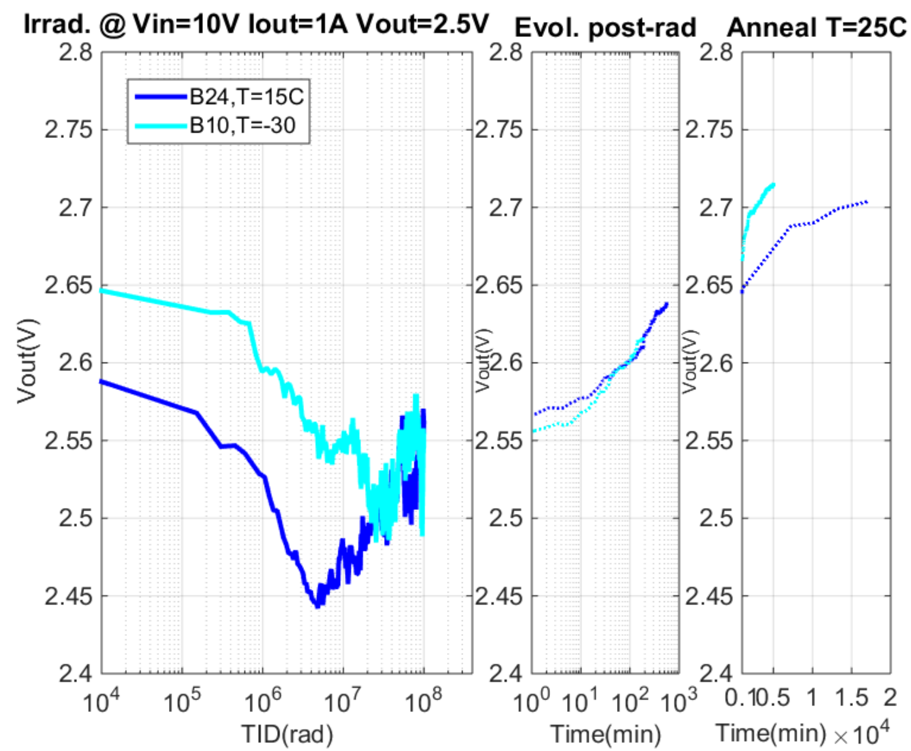




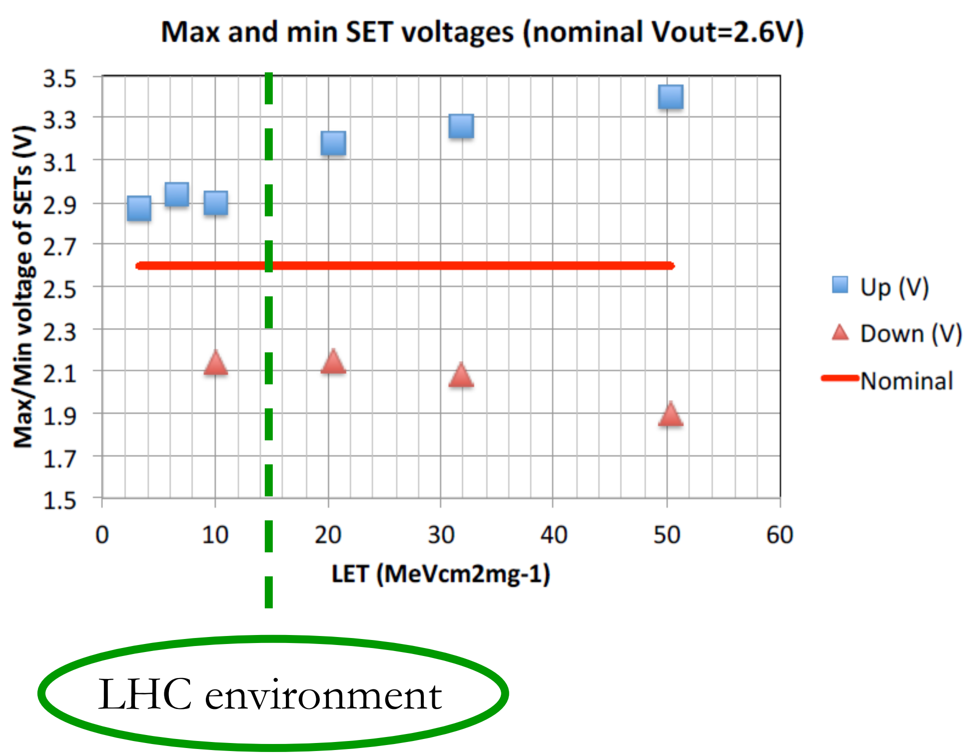
The reference voltage increases beyond its pre-rad value during annealing…

… and so does the output!

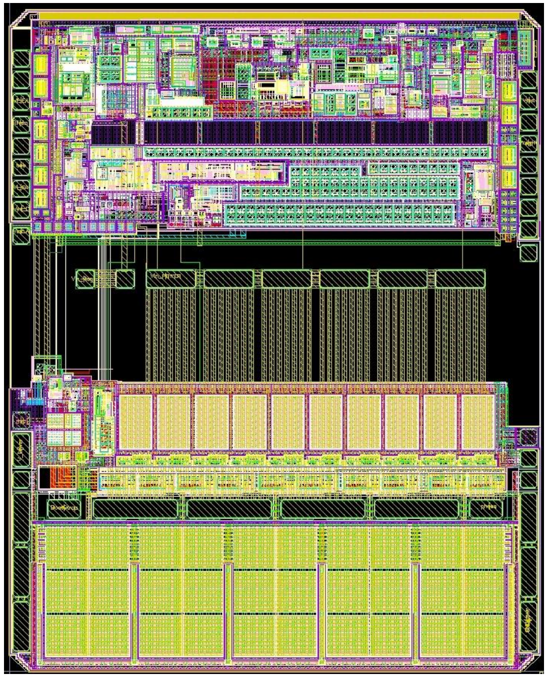


SEE tests using heavy ions (CRC facility in Leuvain-la-Neuve) up to a LET of $50\,\frac{MeVcm^2}{mg}$ have evidenced no reset or destructive event

Only transients at the output ($\approx 10\ \mu s$) have been recorded



Final considerations on upFEAST2



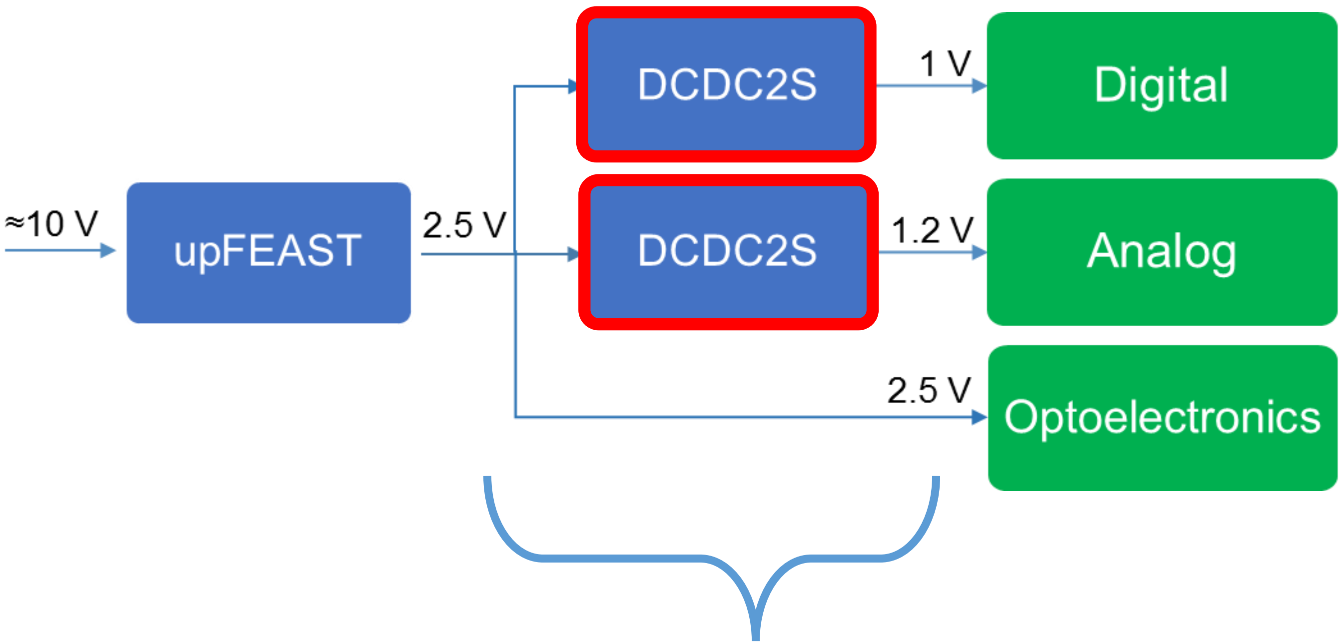
A fully functional prototype has been designed, showing satisfactory TID and SEE tolerance

Displacement damage tests are ongoing

Minor issues are currently being faced for the next, and hopefully final, iteration

Still, the details of the integration in the modules are not known: possibly, some customizations will be needed

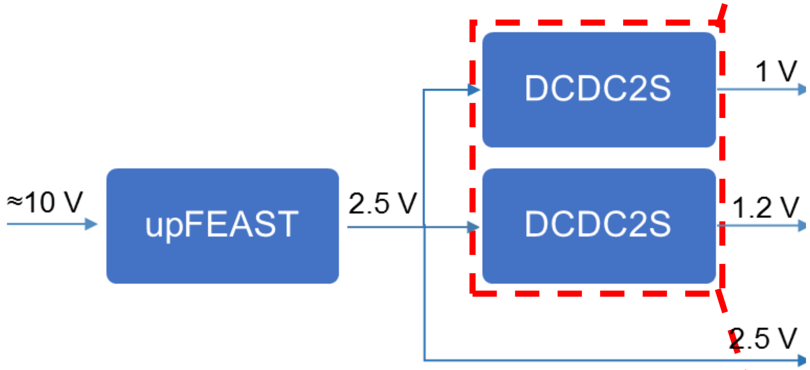
Power distribution scheme in CMS PS module



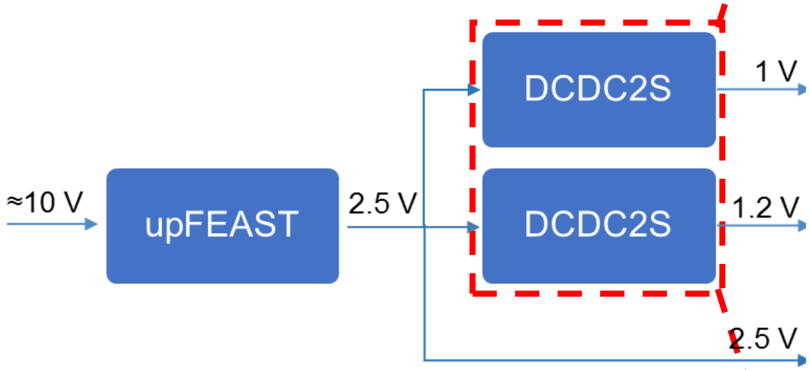
2^{nd} stage conversion

Novel design

(130 nm technology)



Input voltage	2.0 V ÷ 2.5 V
Output voltage	0.6 V ÷ 1.5 V
Output current	≤ 3 A
Switching frequency	≥ 4 MHz
Inductor value	< 150 nH
External components	Only C_{in}, C_{out}, L
Assembly	C4 bump bonding
Radiation Tolerance	
Total Ionizing Dose	< 150 Mrad
Displacement Damage	> $4 \cdot 10^{15}$ n/cm^2
SEEs: absence of destructive events and output power interruptions	> 40 MeV·cm^2/mg



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DCDC2S: what the technology offers

Accessibility,
MPWs available

Fast turnaround time

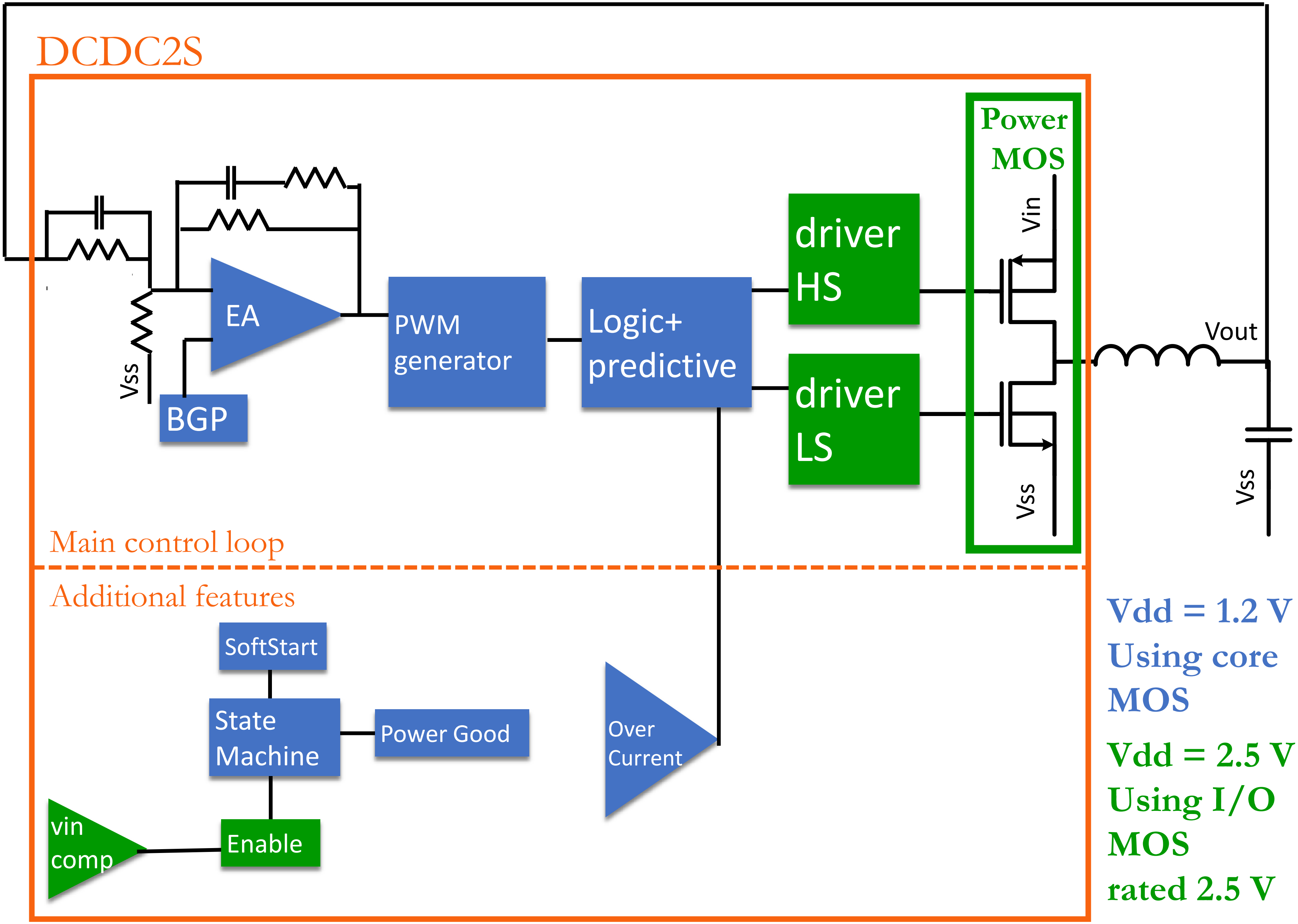
Bump bonding

130 nm CMOS

eFUSEs available

I/O transistors rated 2.5 V or 3.3 V

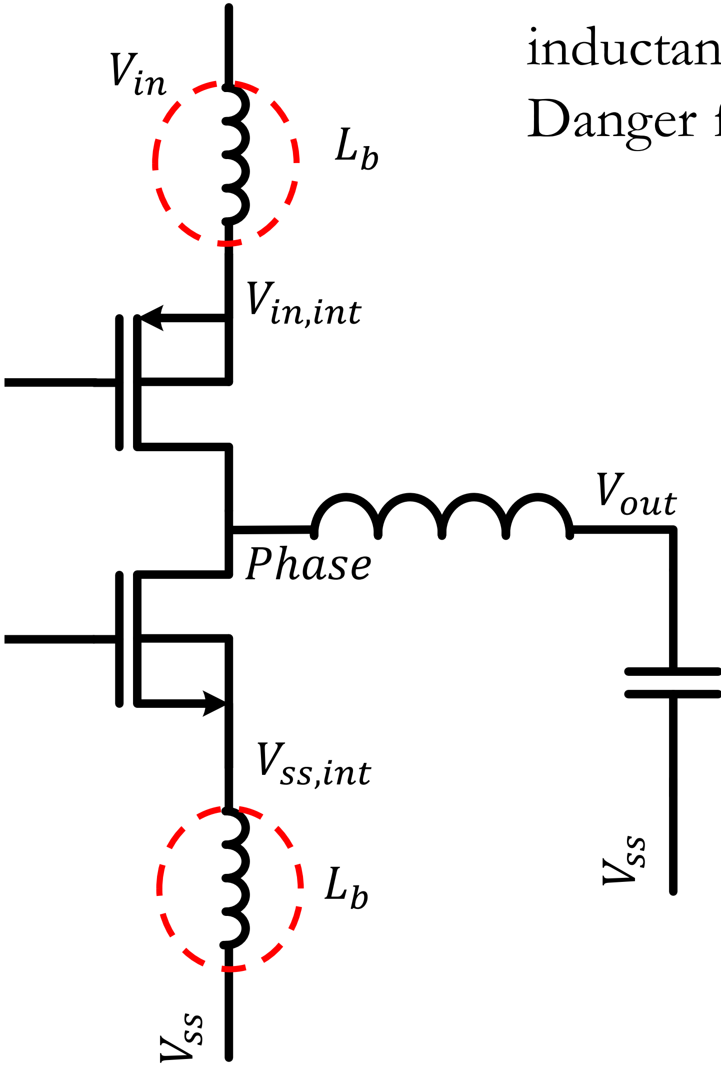
Improved radiation hardness (core devices in the control circuitry)



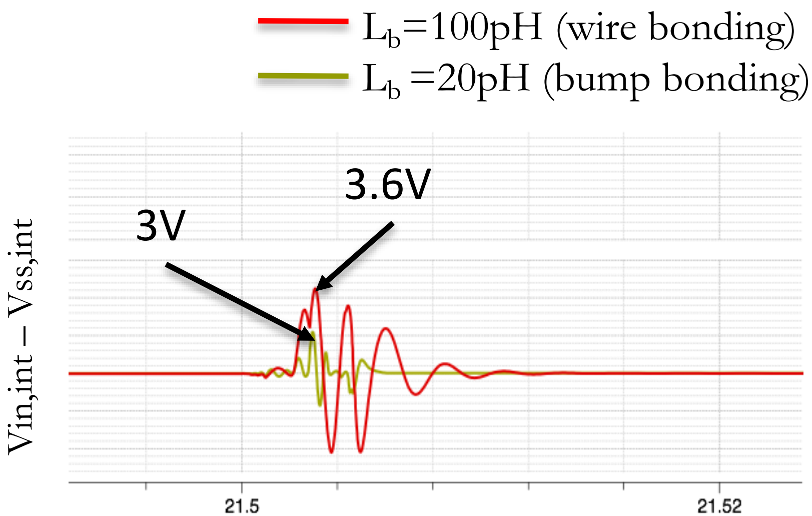
Vdd = 1.2 V
Using core MOS

Vdd = 2.5 V
Using I/O MOS
rated 2.5 V

The large $\frac{dI_{L_b}}{dt}$ in the bonding parasitic inductances cause spikes in $(V_{in,int} - V_{ss,int})$. Danger for I/O transistors rated 2.5 V!



$$V_{L_b} = L_b \frac{dI_{L_b}}{dt}$$



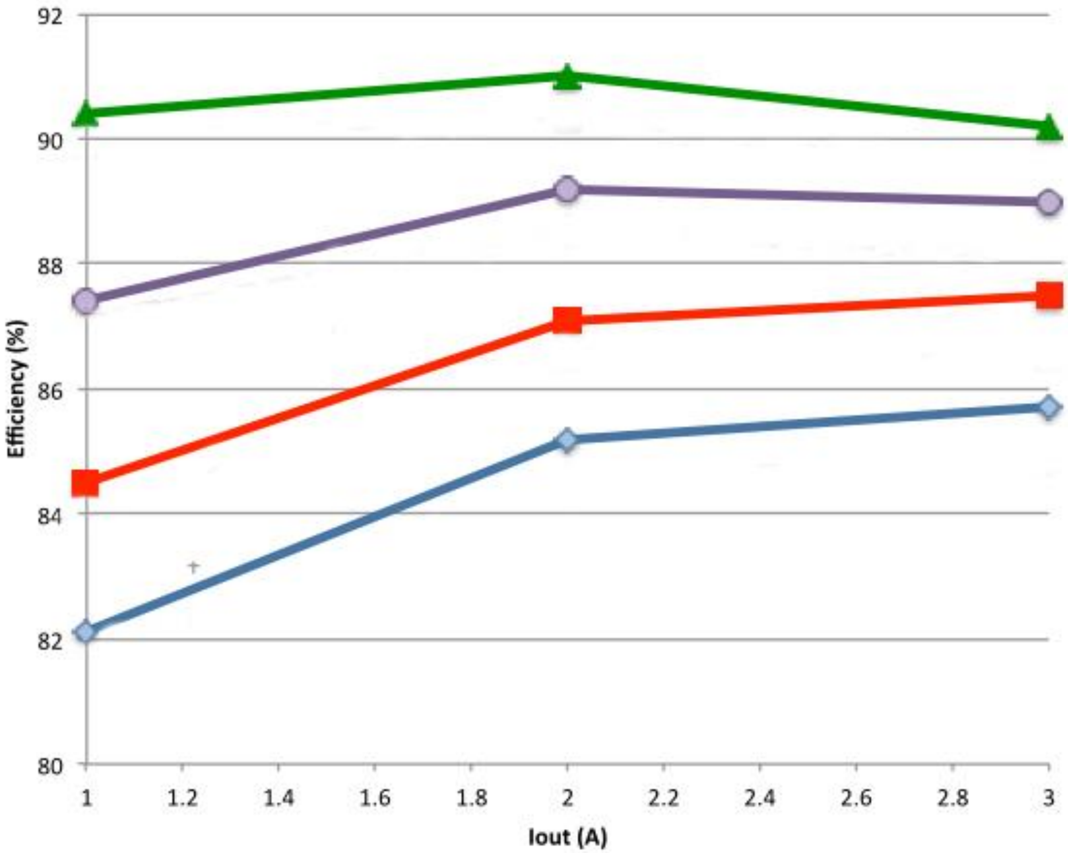
$$V_{L_b} = L_b \frac{dI_{L_b}}{dt}$$

Bump bonding needed to reduce the parasitic inductances

Slow rise and fall time for the power MOS Vgs

Penalty in efficiency

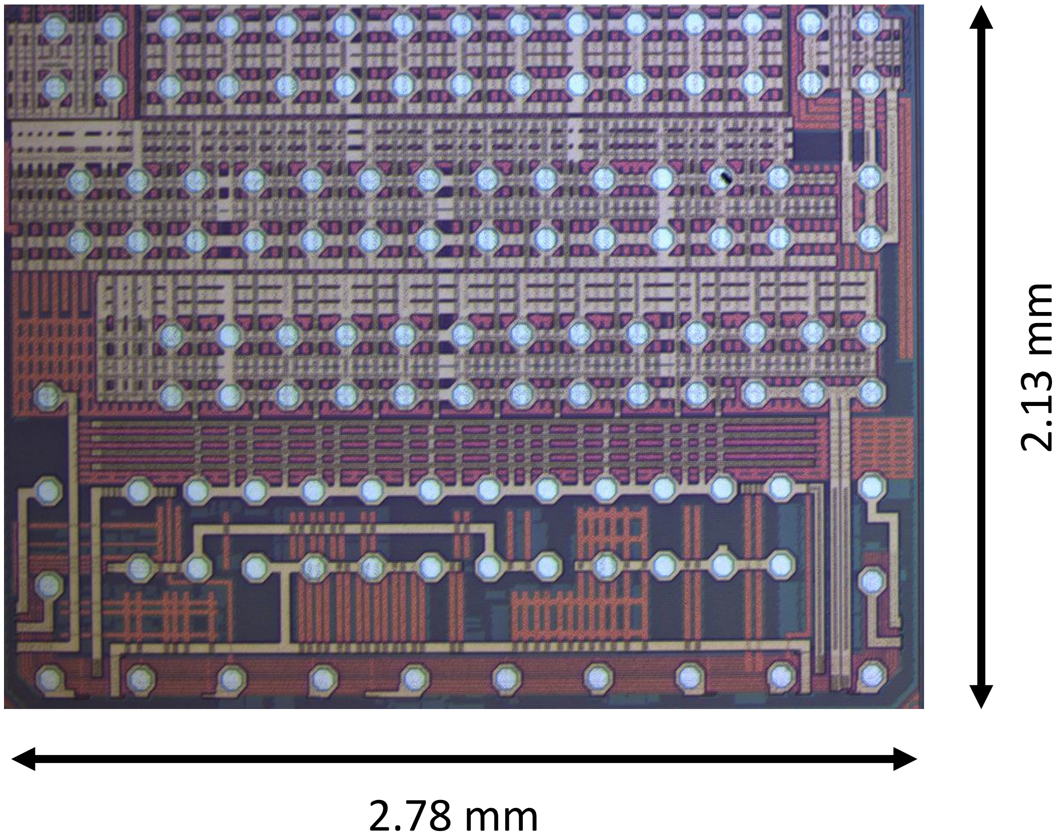
Efficiency simulations: DCDC2S using 2.5 V-rated MOSFETs



	Switching frequency (MHz)	L (nH)	DC Res (mΩ)
	4	100	21
	6	68	8.2
	8	47	5.6
	10	39	5

The inductance values are taken from the Coilcraft midi series (http://www.coilcraft.com/midi.cfm).

Just an example, since the inductor shape should be toroidal.

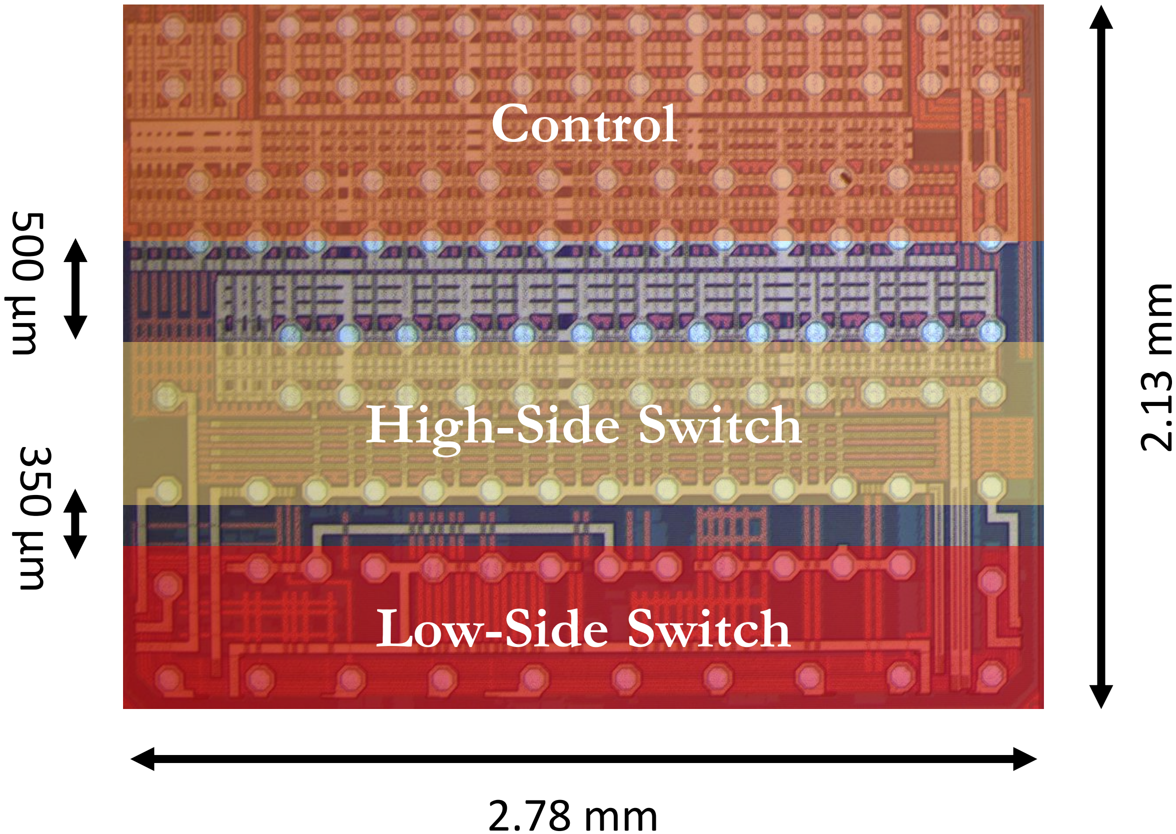


First prototype featuring I/O transistors rated 2.5 V

Submitted in May, 2016 (special thanks to VeloPix)

ASIC received and bumps deposited
Assembly is ongoing

A collaboration with EPFL is ongoing to investigate the optimum floorplan for minimum substrate noise



First prototype featuring I/O transistors rated 2.5 V

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ASIC received and bumps deposited

Assembly is ongoing

A collaboration with EPFL is ongoing to investigate the optimum floorplan for minimum substrate noise

New prototype in development using I/O transistors rated 3.3 V

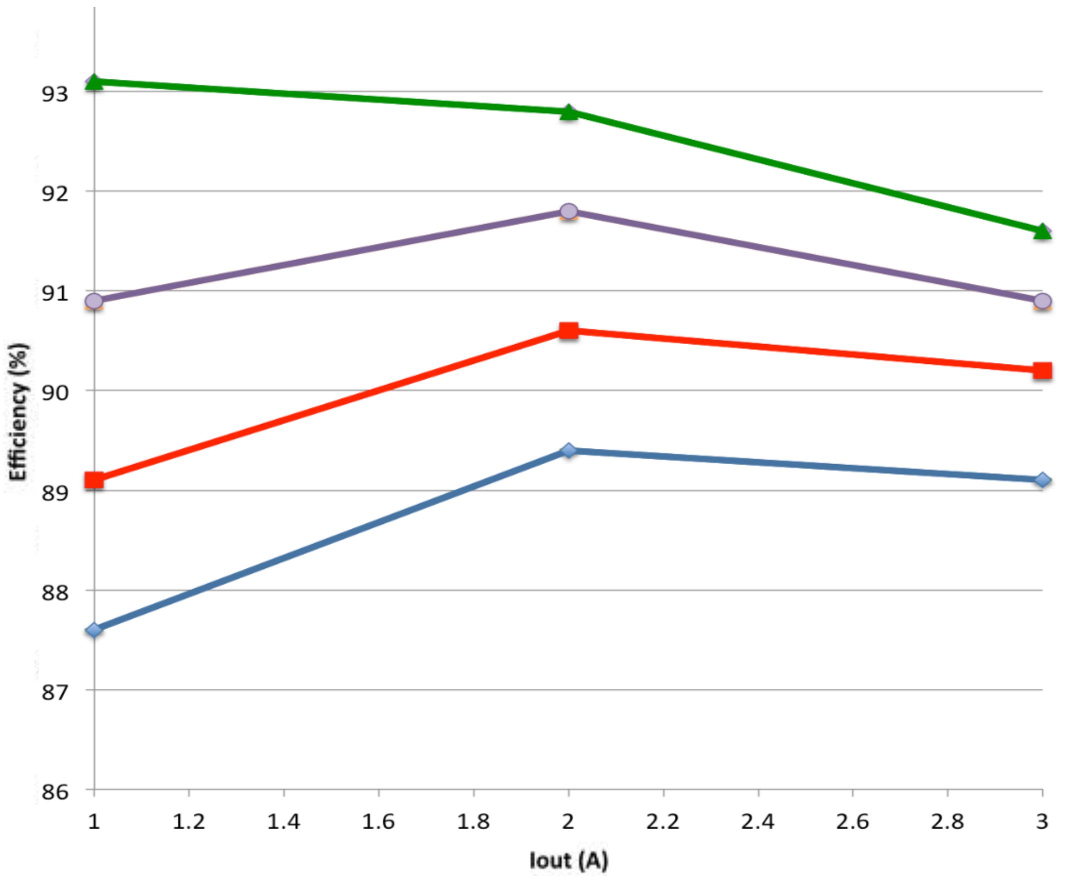
✓

- Larger input voltage range for the converter
- Tolerance to spikes on Vin
- Faster turning on and off of the power transistors possible: improved efficiency

✗

- Increased Ron
- Radiation tolerance?

Efficiency simulations: DCDC2S using 3.3 V-rated MOSFETs

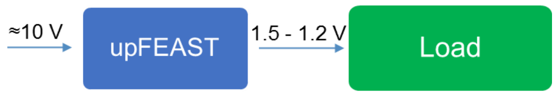


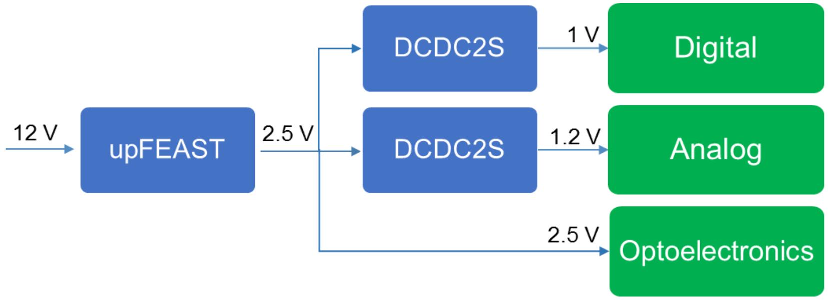
	Switching frequency (MHz)	L (nH)	DC Res (mΩ)
(green)	4	100	21
(purple)	6	68	8.2
(red)	8	47	5.6
(blue)	10	39	5

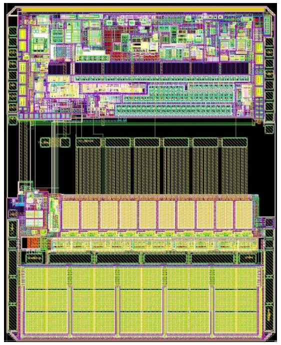
Improved efficiency compared to the previous prototype

Summary

New highly radiation-tolerant DC/DC converters are being designed for an efficient power distribution in HL-LHC experiments

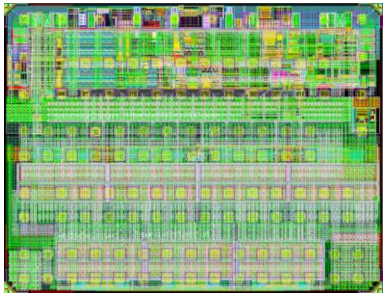






A functional and sufficiently rad-hard prototype of the **upFEAST** family is already existing

Some minor issues are being addressed in the next iteration



The first prototype of **DCDC2S** should be ready for testing at the end of October, 2016

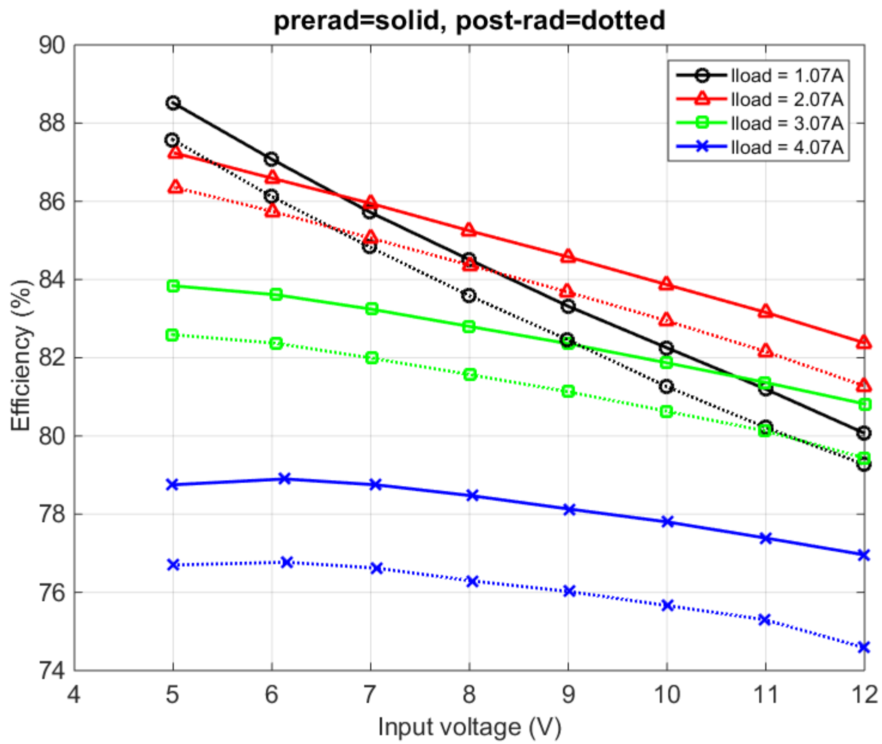
A new prototype is being designed using 3.3 V–rated I/O transistors for more flexibility in input voltage range and tolerance to spikes in Vin

Backup

upFEAST is the result of the migration of FEAST2 design into a 'sister' technology (0.35 μm) that can stand much higher fluence

Input voltage	5 V ÷ 12 V
Output voltage	0.6 V ÷ 5 V
Output current	≤ 4 A
Maximum output power	10 W
Inductor value	0.15 – 1.5 μH
Programmable switching frequency	1 – 3 MHz
Radiation Tolerance	
Total Ionizing Dose	> 700 Mrad
Displacement Damage	$> 5 \cdot 10^{15}$ n/cm^2
SEEs: absence of destructive events and output power interruptions	> 65 MeV·cm^2/mg

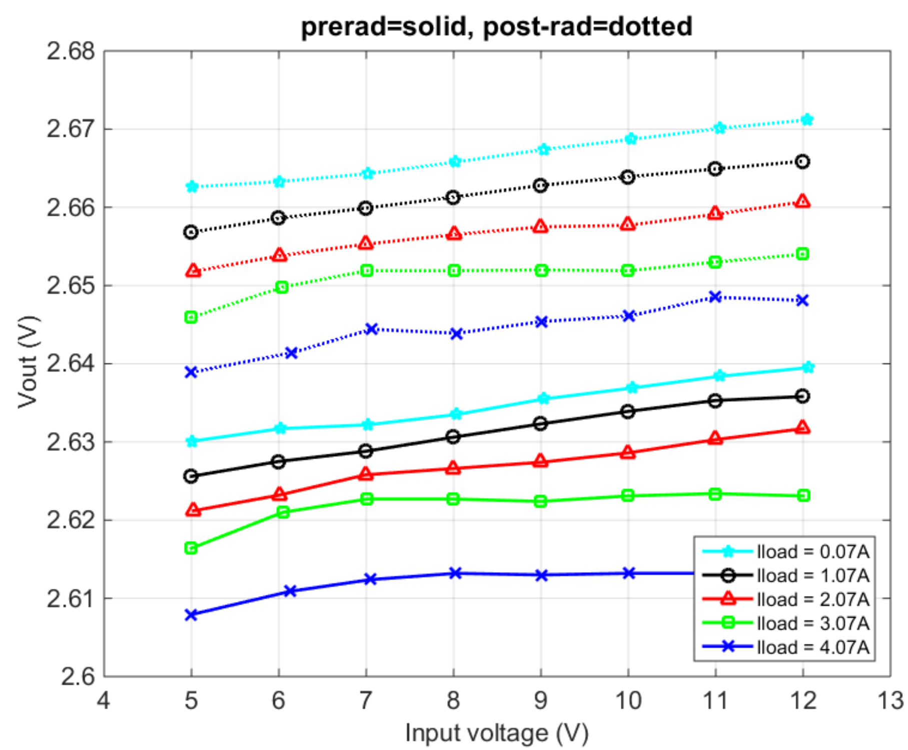
Major improvement compared to FEAST2 (10x)

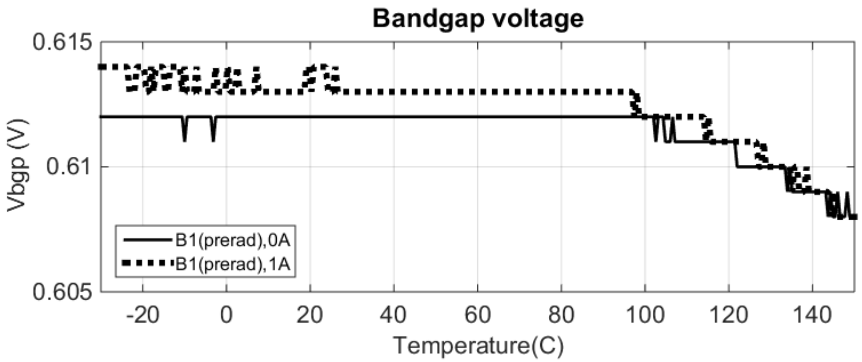


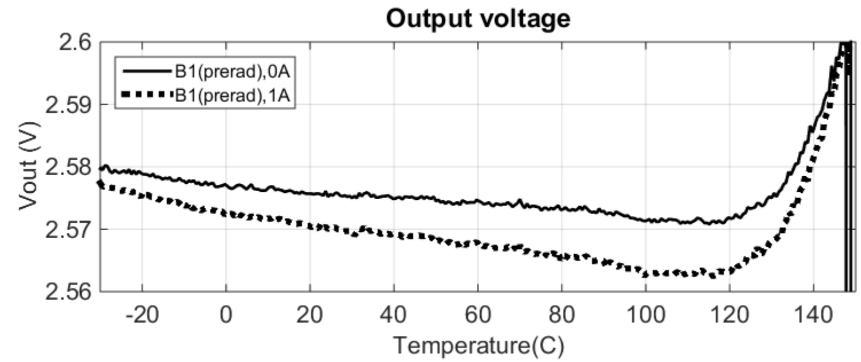
Pre-rad

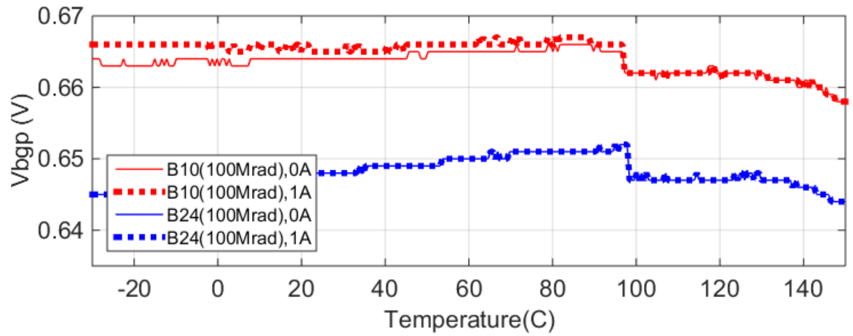
vs.

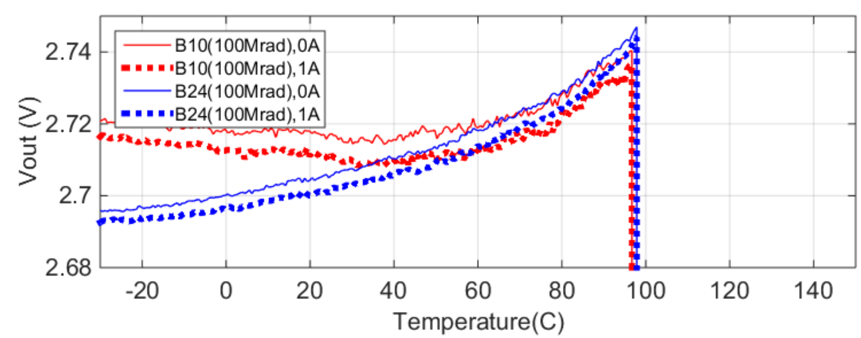
100 Mrad

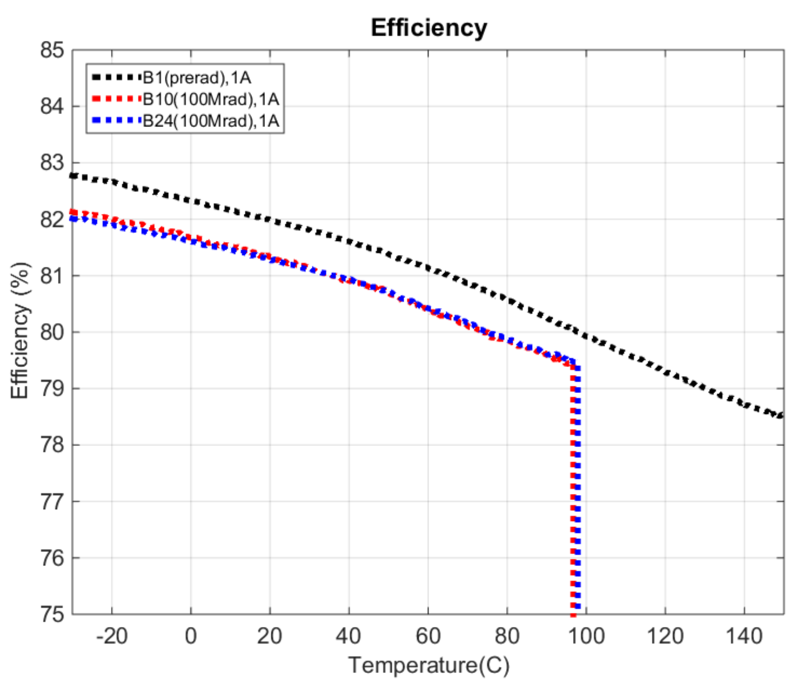




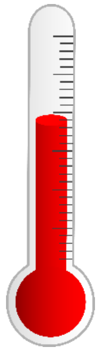


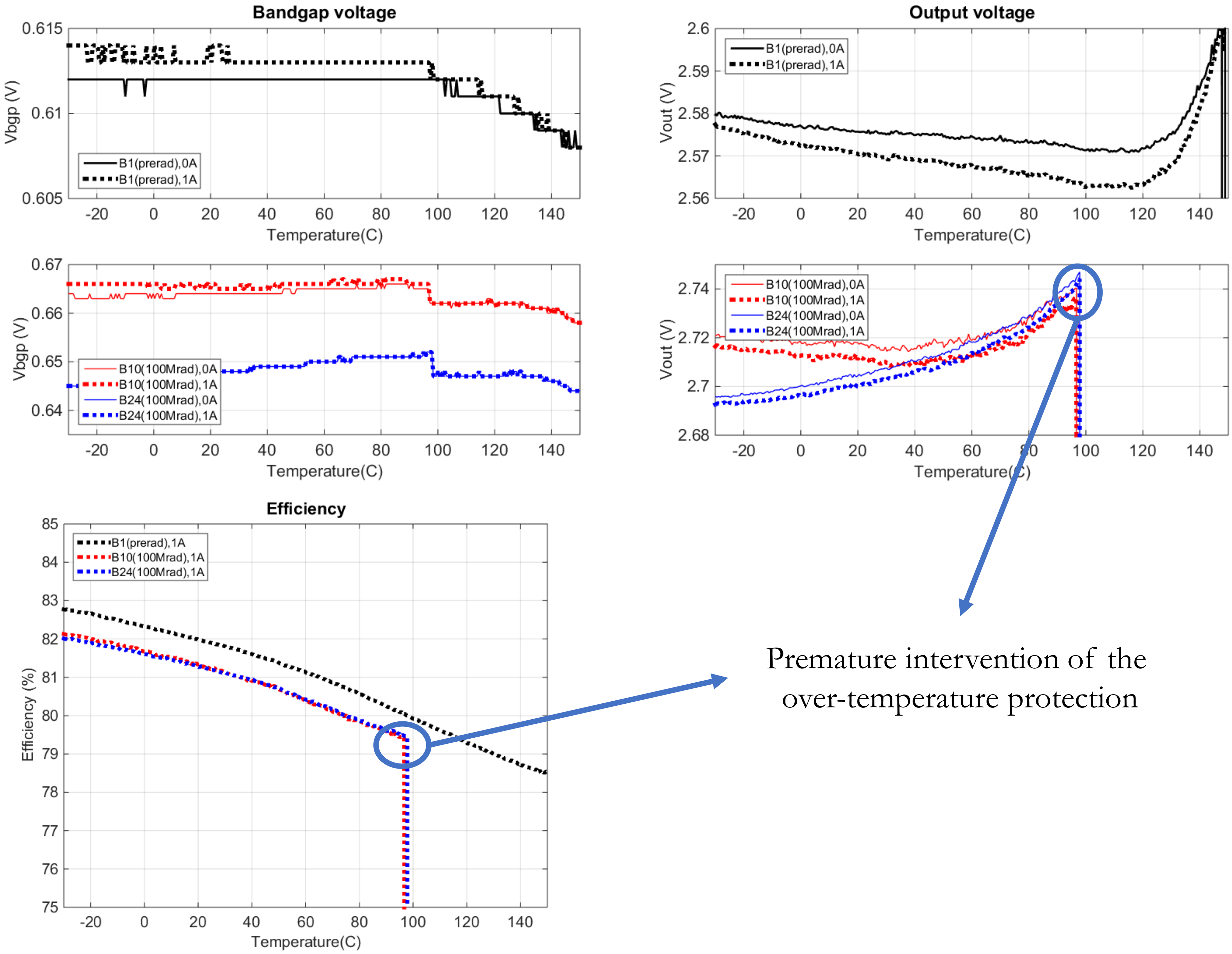






Behavior in Temperature





Bandgap voltage
Vbgp (V)
Temperature(C)
B1(prerad),0A
B1(prerad),1A
Output voltage
Vout (V)
Temperature(C)
B1(prerad),0A
B1(prerad),1A
Vbgp (V)
Temperature(C)
B10(100Mrad),0A
B10(100Mrad),1A
B24(100Mrad),0A
B24(100Mrad),1A
Vout (V)
Temperature(C)
B10(100Mrad),0A
B10(100Mrad),1A
B24(100Mrad),0A
B24(100Mrad),1A
Efficiency
Efficiency (%)
Temperature(C)
B1(prerad),1A
B10(100Mrad),1A
B24(100Mrad),1A
Premature intervention of the over-temperature protection

Monitoring the on-chip temperature…