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Rad-hard DCDC converters for HL-LHC experiment's tracker modules power distribution

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In the context of investigating a more efficient rad-hard power distribution scheme for HL-LHC trackers modules based on switching DC/DC converters, we developed two new prototypes, upFEAST2 and DCDC2S. The combination of upFEAST2 and two DCDC2S can provide the three required voltages (2.5V for the optoelectronics, 1V for digital and 1.2V for analog circuitry).

DCDC2S and upFEAST2 are manufactured with commercial 0.13 μ m and 0.35 μ m high voltage CMOS technology respectively. Design techniques, functional and radiation tests of the prototypes will be discussed.

Summary

The present design of pixel and strip modules for HL-LHC experiment trackers foresees a complex integration of different ASICs that requires several power domains: 2.5V for the optoelectronic drivers, 1.2V for the analog and 1V for the digital circuitry.

A very attractive power distribution scheme based on rad-hard DC-DC converters foresees different conversion stages to obtain the required voltages. The first conversion stage is represented by a new ASIC called upFEAST2 capable of converting 10-12V to 2.5V. The second stage is based on two ASICs called DCDC2S, able to convert 2.5V to 1V and 1.2V respectively.

upFEAST2 is a modified version of the production ready FEAST2 ASIC, integrated in a similar 0.35 μ m high voltage technology in order to enhance its radiation tolerance (in particular the displacement damage limit up to at least 5e15 n/cm²). upFEAST2 has been sent to production in March 2016 and it will be available for test starting from June 2016.

DCDC2S is a completely new ASIC that has been designed in a commercial 0.13 μ m technology. It makes use of IO transistors rated 2.5V for the power part and 1.2V core transistors for the control circuitry. DCDC2S is a fully integrated buck converter (except to input and output capacitor and inductor). It includes overcurrent and input under-voltage protections.

The power transistors are two IO MOS with a width of 320 μ m and 240 μ m for the high and low side respectively. The error amplifier has a bandwidth of 40MHz and a Slew Rate of 10V/ μ s.

The internal oscillator is programmable from 1MHz to 10MHz with an external resistor. The voltage reference is internal and it provides 0.3V with an error of 1% over 100 $^{\circ}$ C and 400Mrad. The dead time delay between the ON-states of high and low side power transistors is managed with the so-called "predictive logic". This logic reduces this delay as much as possible in order to increase the converter's efficiency.

A soft-start procedure is embedded to avoid too large inrush current at the start-up of the converter.

DCDC2S will be submitted in April 2016 and it will be available for test in July 2016.

Functional and radiation tests of upFEAST2 and DCDC2S will be presented at TWEPP.

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