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The VeloPix ASIC

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The LHCb upgrade, scheduled for LHC Run-3, will enable the experiment to be read out at 40 MHz in trigger-less mode, with full event selection being performed offline. The Vertex Locator (VELO) will be upgraded to a pixel device with a new dedicated ASIC, the VeloPix, a 130 nm technology chip with data driven and zero suppressed readout. The sensors are positione at just 5.1 mm from the LHC beams and the hottest ASICs will experience rates of more than 900 Mhits/s. The recently submitted ASIC will be presented along with the first test results.

Summary

The LHCb upgrade, scheduled for LHC Run-3, will transform the experiment to a trigger-less system reading out the full detector at 40 MHz event rate. The Vertex Locator (VELO) will be a hybrid pixel system, featuring silicon pixel sensors with $55 \times 55 \mu$m pitch, read out by the VeloPix ASIC. The sensors and ASICs will approach the interaction point to within 5.1 mm and be exposed to a radiation dose of up to 370 MRad or 8×10^{15} 1 MeV $n_{eq} \ cm^{-2}$. The hottest ASICs must sustain pixel hit rates of more than 900 Mhits/s and produce an output data rate of over 15 Gbit/s, adding up to 1.6 Tbit/s of data for the whole VELO.

This paper will present the VeloPix ASIC which has been developed for the readout of the upgraded VELO. This ASIC derives from the Medipix/Timepix family and has many features in common with the Timepix3, however the VeloPix is further optimised for speed and radiation hardness. Each ASIC reads out an array of 256 x 256 pixels with $55 \times 55 \mu$m square pitch. The ASICs are flip chipped in groups of three to the silicon sensors, and a total of 624 ASICs are needed for the full VELO readout. In order to ensure the cooling of the ASICs within the LHC secondary vacuum the power consumption is limited to <3 W per ASIC; however the achieved performance is expected to significantly improve on this. The ASIC is designed in a 130 nm CMOS technology.

The ASIC readout is data driven and zero suppressed, and the implementation of the super pixel concept (4x2 pixel grouping) further optimises the bandwidth and available space. The timewalk is minimised (at 1000 e-threshold) to reduce the number of out-of-time hits in the 25 ns LHC datataking conditions. Because of the severe radiation environment the ASIC is equipped with SEU protection and is designed to cope with sensor leakage currents. In order to meet the huge data output rate requirement while keeping the power consumption within the budget a dedicated 5.12 Gbit/s output serialiser, the GWT (Gigabit Wireline Transmitter), has been developed. The ASIC has been submitted in April and we expect to show the very first performance results.

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