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TOFFEE: a fully custom amplifier-comparator chip for timing applications with silicon detectors.

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In this contribution we present the design of a 8-channel amplifier-comparator chip specifically optimized to match the signals produced by Ultra-Fast Silicon Detectors (UFSD). The time resolution of the TOFFEE –UFSD system is expected to be around 30 ps. The chip is designed in UMC 110nm CMOS technology, it has a 2x2 mm area and it requires 40 mW per channel. It features LVDS outputs and the signal dynamic range matches the requirements of the HPTDC system.

Summary

The next generation of high-energy experiments will require the capability of taking data at unprecedented intensities, with hundreds of overlapping events. To face this challenge, we need the possibility to distinguish events separated by a few tens of picoseconds. For this reason, segmented silicon sensors with internal gain are being developed (the so called Ultra-Fast Silicon Detectors) so that they will provide the traditional silicon sensor benefits (segmentations, low leakage current, low noise, low capacitance) together with a much larger signal.

We have developed a fully custom ASIC to take advantage of this enhanced signal, optimizing the input stage of the chip to the signal shape of UFSD. The chip provides 8 independent amplifier-comparator channels, each with a comparator threshold controlled via an external voltage level. Each channel comprises a trans-impedance amplifier followed by a discriminator, a stretcher and LVDS driver. The CSA amplifier is implemented with a cascode with split current sources for best noise performances. The discriminator gives an output step between 2 and 14 ns, however to be compatible with the HPTDC input logic (minimum signal length ˜ 12 ns), the signal is lengthened by 10 ns. The chip uses two power values, 1.2 Volt for the analog part, and 2.5 Volt for the LVDS driver, with a total power consumption of 400 mW.

For a 6 pF input load, the gain value is around 7-10 mV/fC with a slope of 30-50 mV/ns and a r.m.s noise of 800 uV providing a SNR of ˜ 75. For a much larger input capacitance of 60 pF the SNR drops to 14, with a slope of ˜ 20 mV/ns and a r.m.s. noise of 1.4 mV. The rise time of the chip has been tailored to be equal to the collection time of a 50-micron thick UFSD sensor, around 1.8 ns, in order to optimize SNR.

The optimization of the chip design has been done using as inputs simulated signals from UFSD 50-micron thick sensors with a gain of 10, generated with the program Weightfield2. For a 6 pF input load, the combination of the TOFFEE chip coupled to 50-micron thick UFSD sensors with gain of 10 provides a r.m.s. time resolution between 25 –35 ps.
The chip has been submitted in early May, and will be tested in the summer 2016.

The performance of the UFSD-TOFFEE system have been tailored to the need of the CT-PPS detector of the CMS collaboration. First beam test results should be available during the 3rd quarter of 2016, with installation during the winter shutdown 2016-2017.

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