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The CMS Level-1 Calorimeter Trigger for LHC Run II

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Results from the completed Phase 1 Upgrade of the CMS Level-1 Calorimeter Trigger are presented. The upgrade was completed in two stages, with the first running in 2015 for pp and Heavy Ions and the final stage for 2016 data-taking. The hardware uses Xilinx Virtex-7 690 FPGAs and 10 Gbps optical links and operates in microTCA chassis. Stages of the upgrade were commissioned in parallel with the previous trigger. Innovations were evaluated, such as embedded linux on trigger processing boards and simultaneous eye-scans on data links. The final stage architecture is time-multiplexed.

Summary

The LHC has resumed operations since the spring of 2015. During Run II, the instantaneous luminosity is expecting to exceed the design parameters of the machine. To maintain acceptance for proton and heavy ion collision events of interest without exceeding the 100 kHz limit, the CMS Level-1 (L1) trigger has been being upgraded. The L1 calorimeter trigger, which finds electrons, photons, tau leptons, jet candidates and computes energy sums, has been upgraded in two stages. In these intense conditions, both stages have implemented pile-up mitigation techniques in order to reach acceptable performance. Modern technologies offer an effective solution to achieve these goals. The upgraded system makes use of new Xilinx Virtex-7 based AMC cards form the microTCA technology.

The final stage of the upgraded architecture implements an innovative approach called the Time-Multiplexed-Trigger (TMT). Higher granularity inputs, algorithms operating on a wider field of view allow for improved position and energy resolution of regional and global quantities. Calorimeter trigger primitive data is transmitted on 1,152 optical links running at either 4.8 Gbps or 6.4 Gbps. This is pre-processed at Layer-1 before being time multiplexed to Layer-2 where each node processes data from the entire calorimeter. Optical interconnects are via 10 Gbps optical links, which allow easy reconfiguration or expansion as required. This has been made substantially easier with the early adoption of Molex Flexplane technology. Data is then de-multiplexed before sequential transmission to the Global Trigger.

Calorimeter Trigger Processor, Virtex-7 (CTP7) AMC cards serve as the Layer-1 pre-processors, and MP7s serve as the Layer-2 Master Processor nodes. This approach is designed to allow for a high processing clock speed of 240 MHz and thus efficient use of logic resources. The fully pipelined firmware approach of the TMT provides an efficient way to localize the processing, reduce the size and number of fan-outs, minimize routing delays and eliminates register duplication. All calorimeter object algorithms are placed and routed into a single board using a precise FPGA floorplanning. The High Level Trigger model inspired the design of the upgraded Level-1 system.

The talk will cover the technological aspects of the Run II calorimeter trigger system emphasizing the many challenges of its implementation and commissioning over the past year. Results of its performance during the first 2016 collisions of the LHC will be presented and used to illustrate the experience learnt in terms of commissioning this complex electronics systems which relies on the deployment of high-speed optical links and large FPGA processing. The AMC boards designed for this project are aiming towards a standardization of the data processing required for the future LHC electronics systems.

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