

ATLAS FAST TRACKER AND TRACKING AT HIGH LUMINOSITY LHC

TWEPP, 2016

Nikolina Ilic on behalf of the ATLAS collaboration

Stanford University

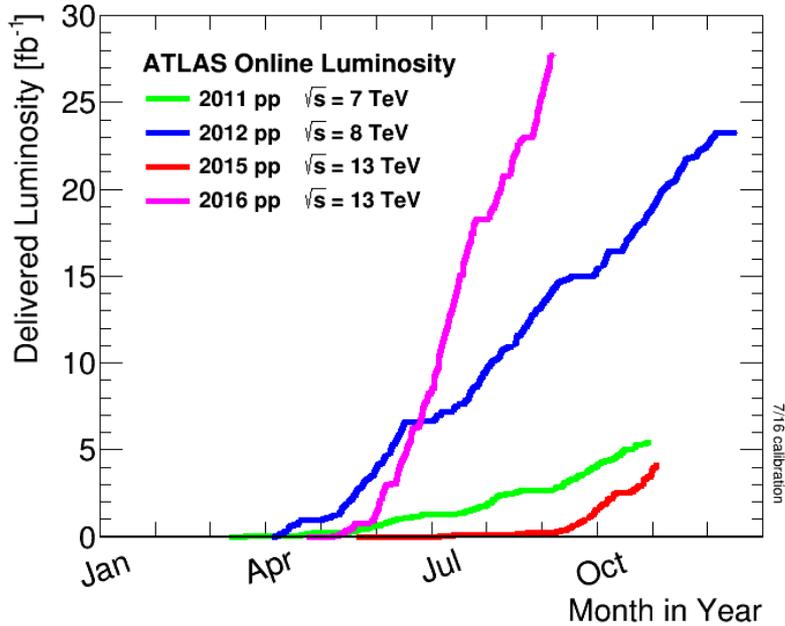
Sept. 30, 2016

- FTK Introduction
 - What is the ATLAS Fast Tracker (FTK)?
 - Why is the FTK useful?
 - How does the FTK work?
- FTK Hardware Components
- FTK Expected Performance
- FTK Commissioning Status
- FTK Plans

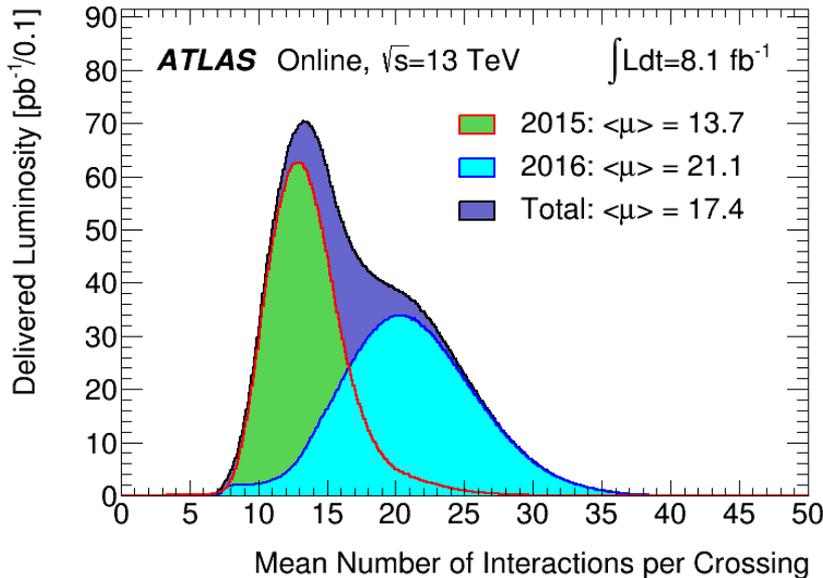
- Tracking at High Luminosity LHC

INTRODUCTION

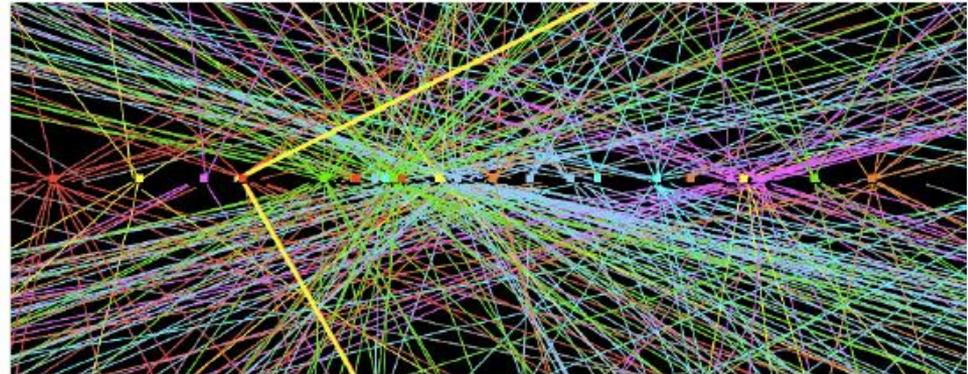
Introduction



- LHC running well, gathering a lot of data at high instantaneous luminosity
 $\sim O(10^{34} \text{ cm}^{-2} \text{ s}^{-1})$
- Peak mean number of interactions per bunch crossing (pileup) increased to 40 in 2016

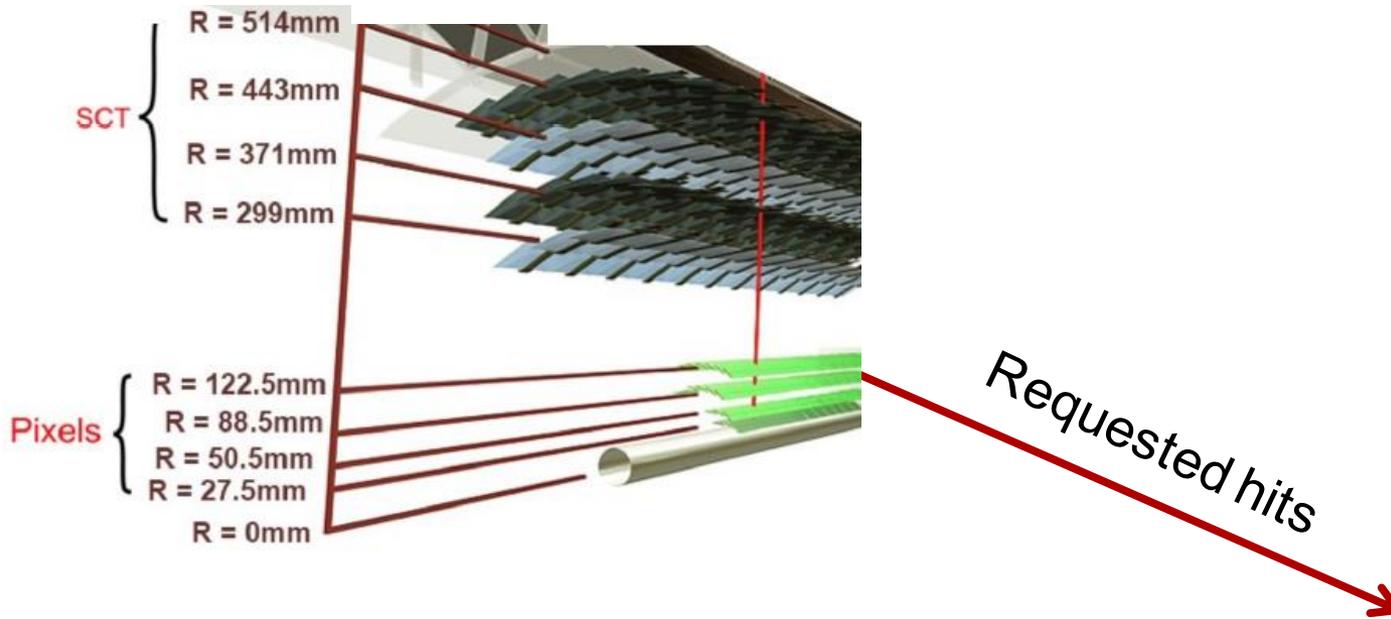


$Z \rightarrow \mu\mu$ event (25 reconstructed vertices)



What is the FTK?

ATLAS's innermost detector has
12 layers: 4 Pixel Detector, 8
Semiconductor Tracker (SCT)



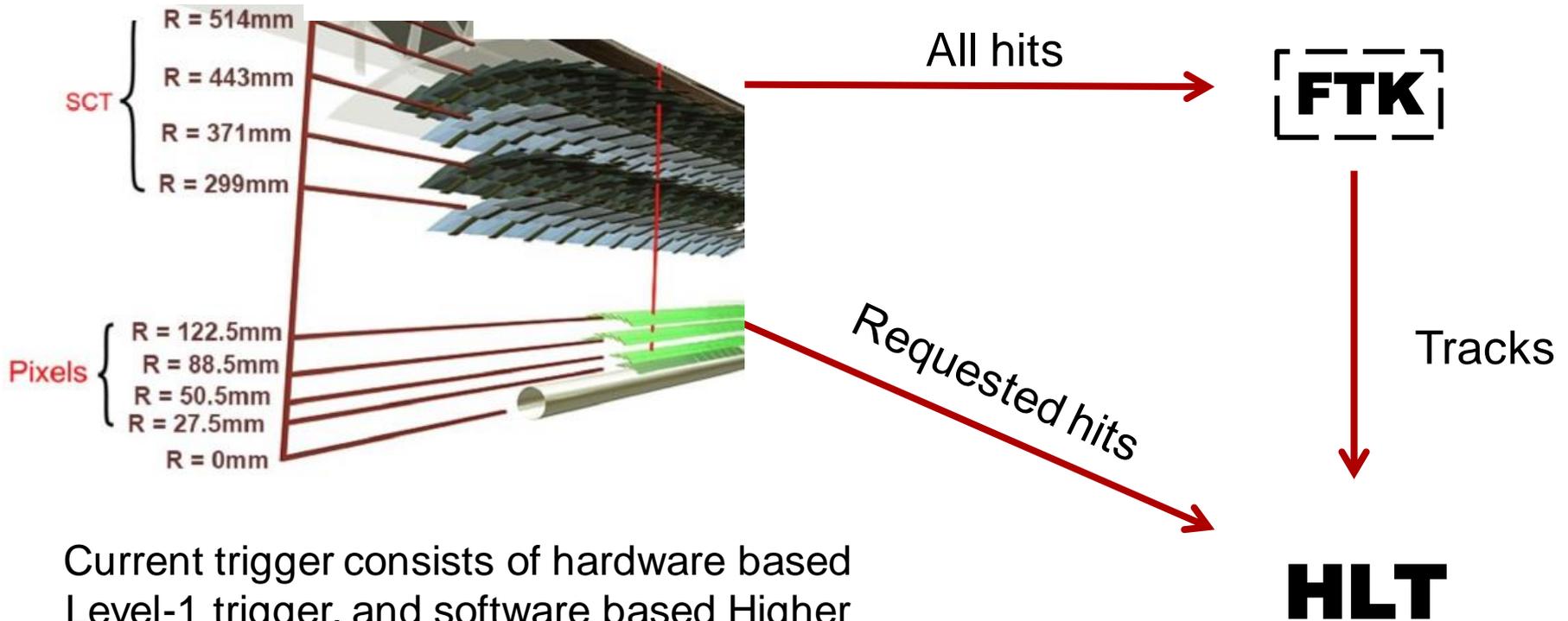
Current trigger consists of hardware based Level-1 trigger, and software based Higher Level Trigger (HLT). HLT utilizes tracking information in small regions of the detector for a subset of events

HLT

What is the FTK?

ATLAS's innermost detector has 12 layers: 4 Pixel Detector, 8 Semiconductor Tracker (SCT)

ATLAS Fast Tracker (FTK) will reconstruct tracks from all hits and provide them to HLT

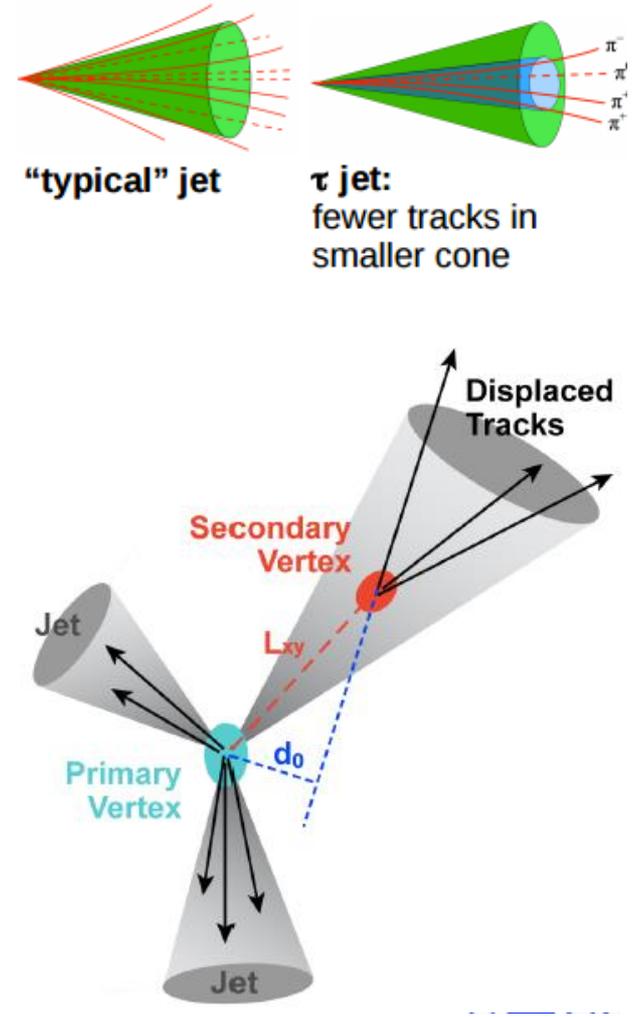


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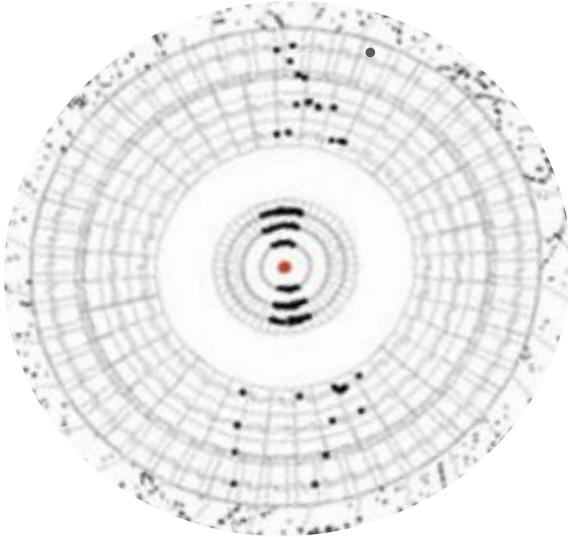
Why is FTK useful?

A few examples

- Measure Higgs Properties! (ex: are fermionic-couplings SM-like?)
 - Final states with b-quarks and τ - leptons important but have very large backgrounds from light quark and gluon jets
 - FTK can identify b-quarks by finding displaced vertex
 - FTK can identify τ leptons by providing tracks in jet cones
- SUSY sparticles can decay to medium energy b and τ which are difficult to trigger without FTK
- Exotic and other physics searches
 - track based Missing Transverse Energy (MET) is less sensitive to pileup than calorimeter based MET

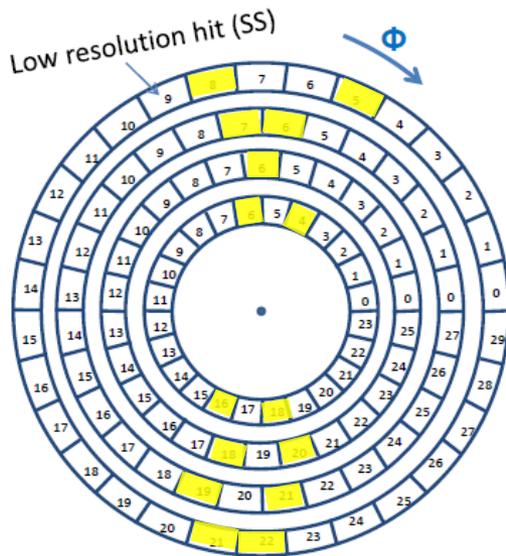


How does FTK work?



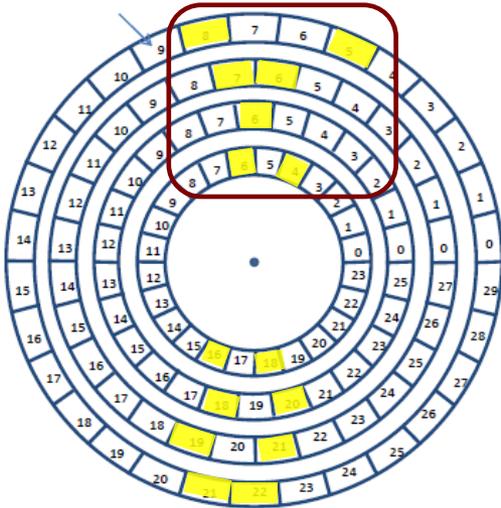
Cluster Pix/SCT
hits to reduce data

How does FTK work?

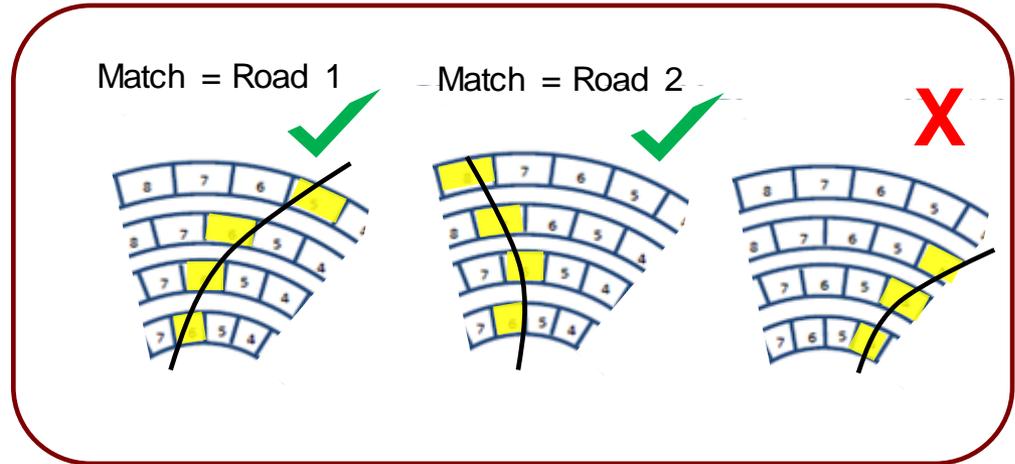


Identify hits by coarser grained Pix/SCT segments called super strips (SS)

How does FTK work?

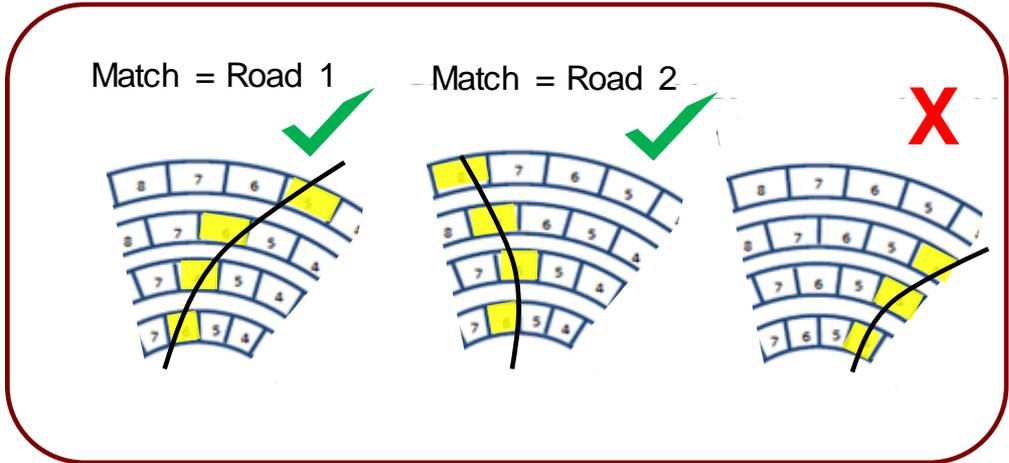
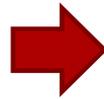
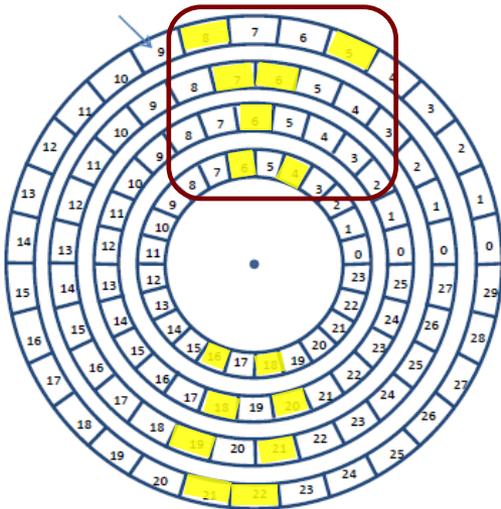


Identify hits by coarser grained Pix/SCT segments called super strips (SS)



Find pre-stored MC track patterns that match the super strips in 8 layers. Matches are called Roads

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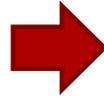
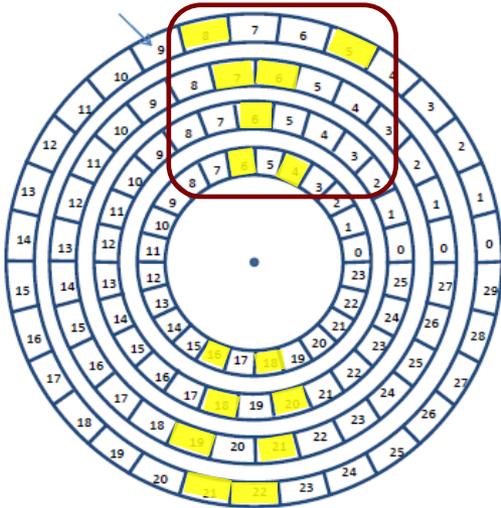
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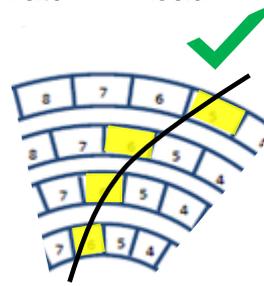


Retrieve fine resolution hits for all roads

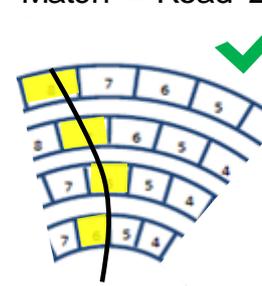
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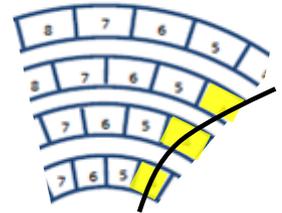
Match = Road 1



Match = Road 2

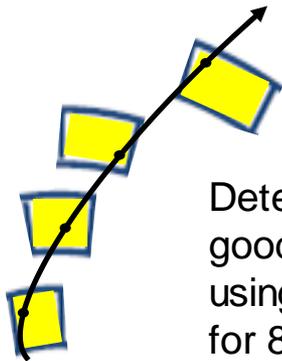


X



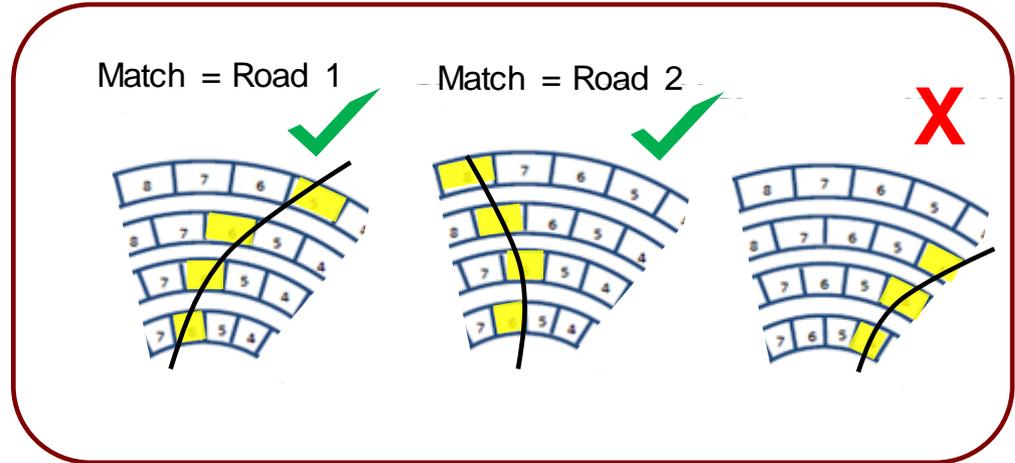
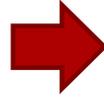
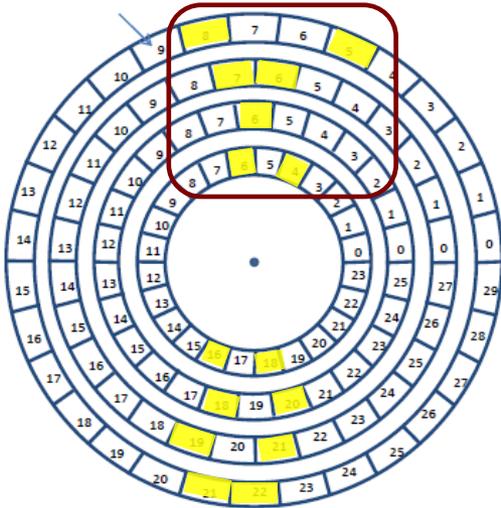
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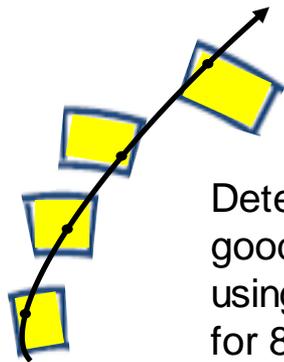
Determine goodness of fit using χ^2 test for 8 layers

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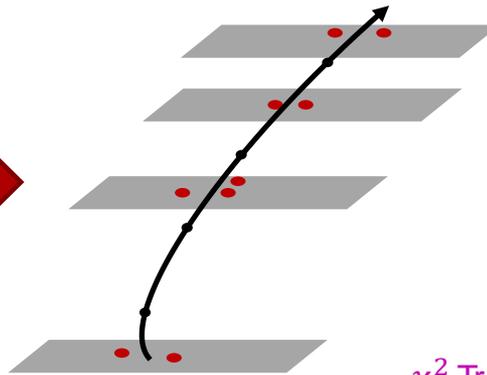
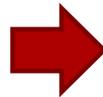


Identify hits by coarser grained Pix/SCT segments called super strips (SS)

Find pre-stored MC track patterns that match the super strips in 8 layers. Matches are called Roads



Determine goodness of fit using χ^2 test for 8 layers



Extrapolate 8 layer tracks to additional 4. Perform 12 layer track fit

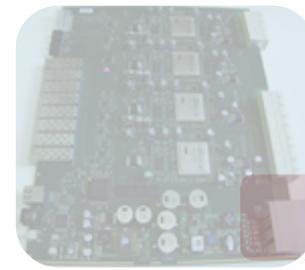
$$p_i = \sum_j C_{ij} \cdot x_j + q_i$$

χ^2 Track parameters, Hit position, Constants

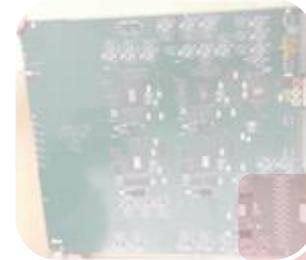
Hardware Components

Input Mezzanine

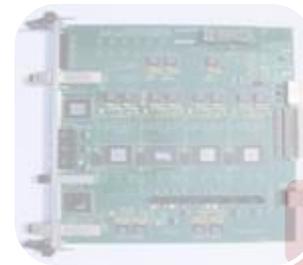
- Input Mezzanine (IM) receives the SCT/Pixel detector hits and clusters them at 100 kHz input event rate
- Calculates cluster centroid, cluster shape/size and Time Over Threshold value that contains charge information
- 128 IMs on 32 Data Formatter boards
- Uses Spartan-6 and Artix-7 FPGAs



Send to HLT



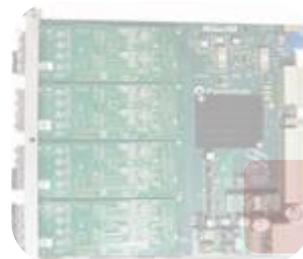
Fit 12 layer tracks



Fit 8 layer tracks



Match hits to pre-defined track patterns

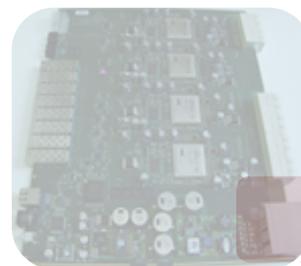


Sort hits into 64 regions

Cluster hits

Data Formatter

- Data Formatter (DF) sorts clustered hits into 64 eta-phi regions for parallel processing
- Distributes hits to regions using ATCA full-mess backplane and inter-shelf fibers
- Using custom microcontroller (LAPP IPMC) for powering/sensor control, and remote FPGA programming
- 32 boards in 4 ATCA shelves
- Uses Virtex-7 FPGA



Send to HLT



Fit 12 layer tracks



Fit 8 layer tracks



Match hits to pre-defined track patterns



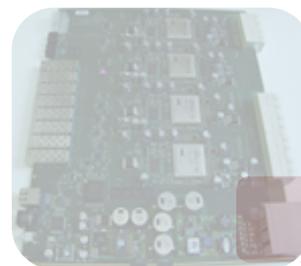
Cluster hits



Sort hits into 64 regions

Associative Memory

- Associative Memory Boards (AMB) match coarse grained hits (super strips) to pre-defined Monte Carlo track patterns in 8 layers
- 1 billion patterns stored in HEP-specific Content Addressable Memory (CAM) on AM Chip 06 which performs 10^{14} word comparisons per second
- Allows for patterns with widths that vary layer by layer (using ternary CAM cells)
- 16 chips per Local AMB (LAMB) \rightarrow 4 LAMBs per AMB \rightarrow 128 AMBs in VME crates



Send to HLT



Fit 12 layer tracks



Fit 8 layer tracks



See talk by L.Valentino



Match hits to pre-defined track patterns



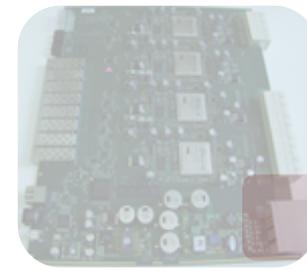
Cluster hits



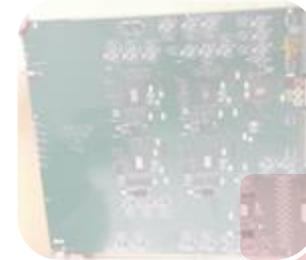
Sort hits into 64 regions

Auxiliary Card

- Auxiliary (AUX) Card receives matched track candidates (roads) from AMB, retrieves corresponding full resolution hits, does track fit in 8 layers
- Cuts on χ^2 to reduce data to next board
- Accounts for tracks that do not have hits in every layer, and if fit quality is poor, allows hits to be dropped
- Duplicate tracks removed
- 128 boards in VME crates
- Uses Arria-5 FPGAs



Send to HLT



Fit 12 layer tracks



Fit 8 layer tracks



Match hits to pre-defined track patterns

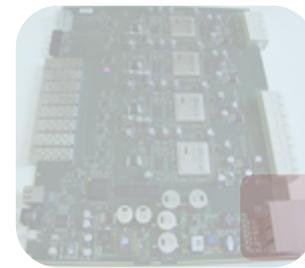


Cluster hits

Sort hits into 64 regions

Second Stage Board

- Second Stage Board (SSB) extrapolates 8-layer tracks from AUX to additional 4 layers from DF and does linear fit in all 12 layers
- Duplicate tracks removed
- 32 SSB boards in VME crates
- Uses Kintex-7 FPGAs



Send to HLT



Fit 12 layer tracks



Fit 8 layer tracks



Match hits to pre-defined track patterns



Sort hits into 64 regions

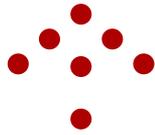
Cluster hits

FTK Level-2 Interface

- FTK Level-2 Interface Crate (FLIC) organizes tracks from SSB and sends them to the High Level Trigger Read Out Systems
- Uses custom LAPP microcontroller + PIC
- 2 FLICs in 1 ATCA shelf
- Uses Virtex 6 FPGAs



Send to HLT



Fit 12 layer tracks



Fit 8 layer tracks



Match hits to pre-defined track patterns



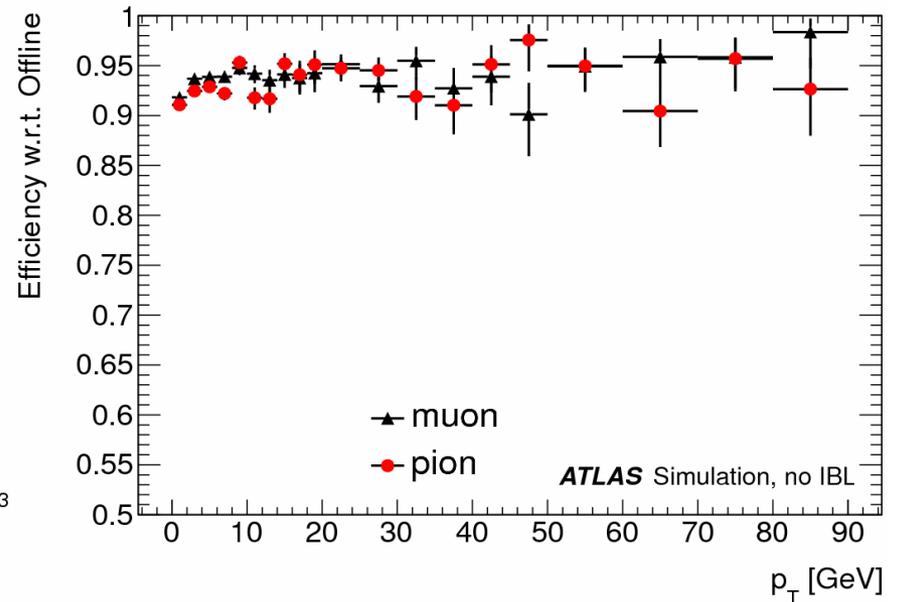
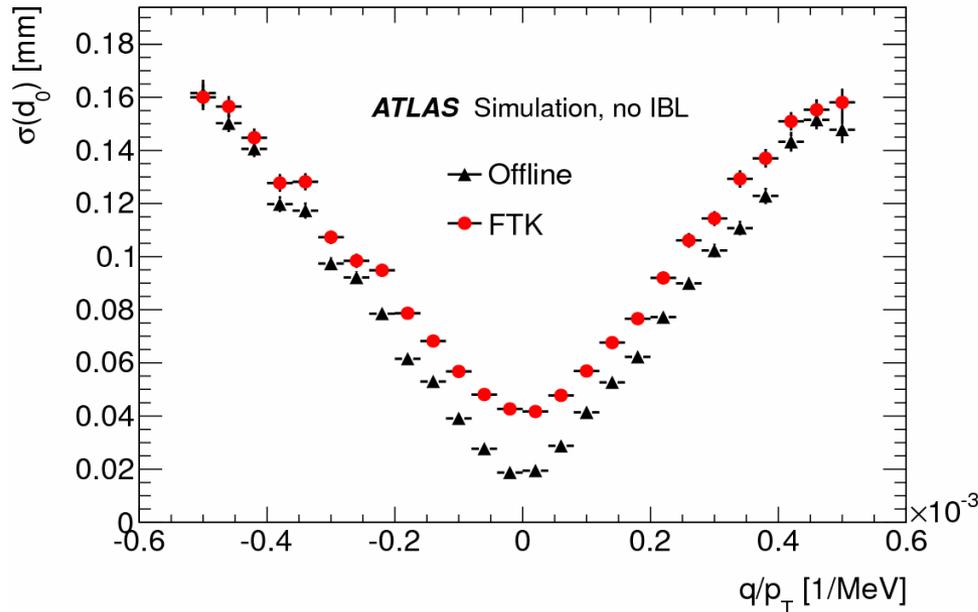
Sort hits into 64 regions

Cluster hits



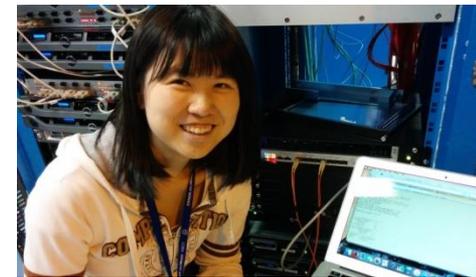
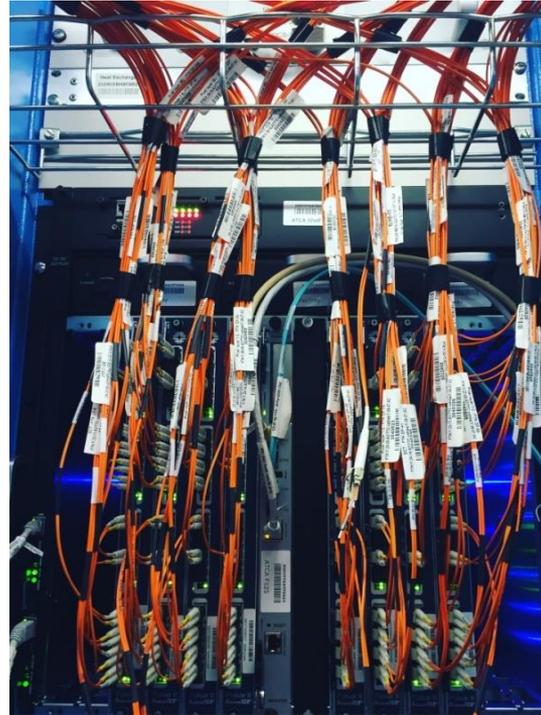
Expected Performance

- FTK reconstruction efficiency with respect to offline reconstruction is greater than 90%
- Small differences due to using only silicon detectors, simplified clustering and considering only tracks with momentum greater than 1 GeV



FTK Commissioning Status

- 65% of IM+DF shelves installed and being commissioned with ATLAS data
- IM+DF+AUX slice integrated and regularly running with the ATLAS detector. FTK hits written into ATLAS event data stream
- Firmware complete and being debugged with simulated and real data
- Board communication being stress tested in a lab
- Data flow through board being matched to simulation



♀	RUNNING	FTK-segment
	RUNNING	FTK-RCD-DF-1
	RUNNING	FTK-MasterTrigger

2016

- Data coming out of FTK, part of FTK system in stable ATLAS data-taking partition

2017

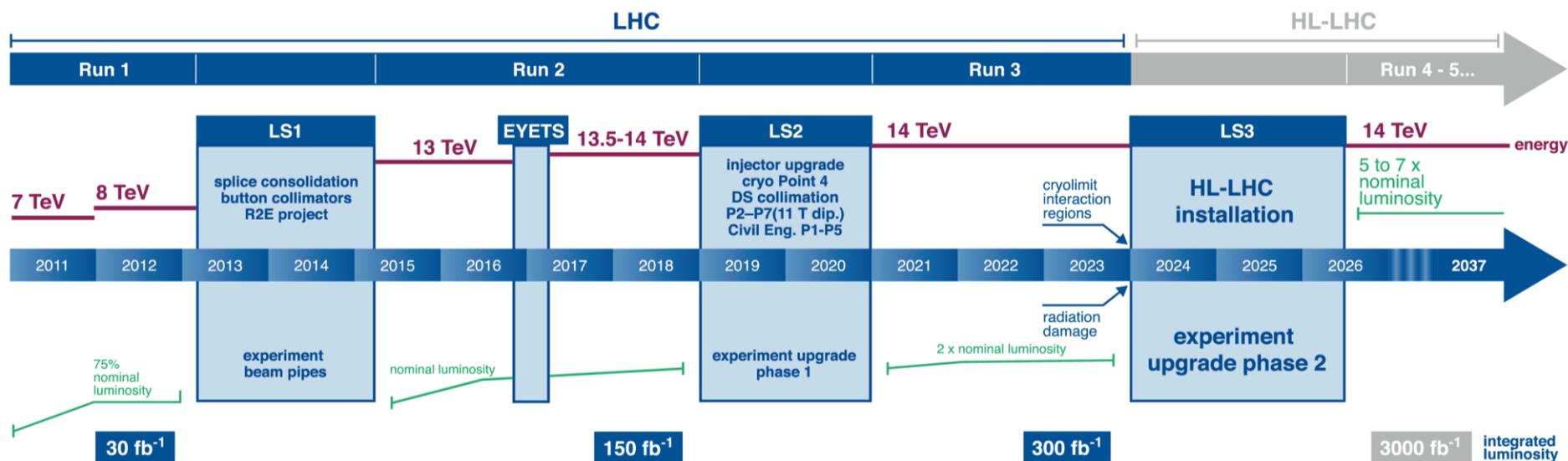
- Commission full detector with half of the processing units (64 AUX+AMB) for pileup 40
- ATLAS trigger will use FTK

2018

- Commission full detector with all processing units (128 AUX+AMB) for pileup 80 by 2018

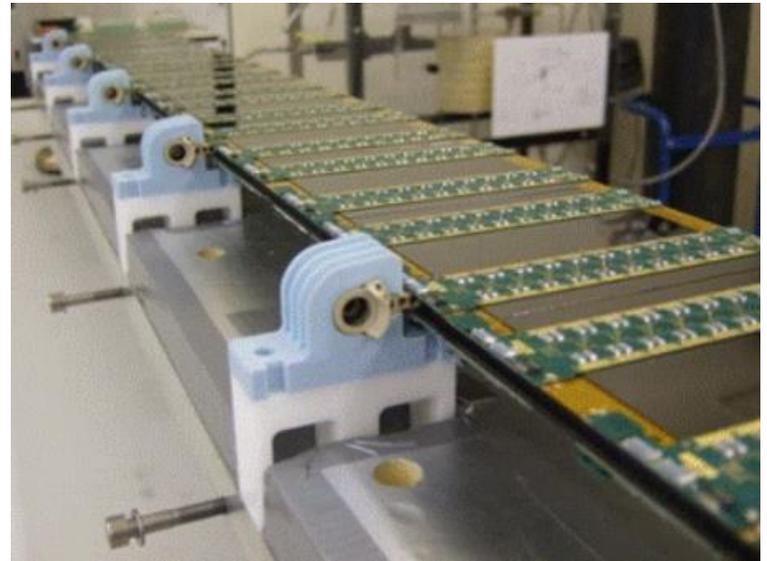
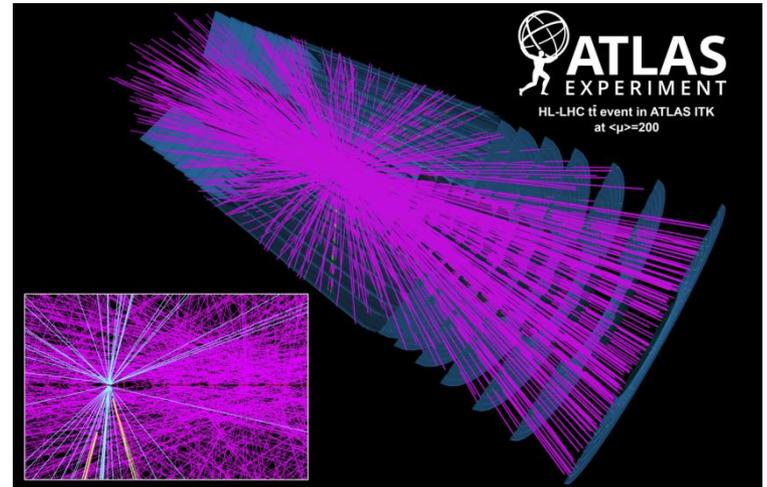
Tracking at High Luminosity LHC

- At High-Luminosity LHC (HL-LHC) number of interactions per bunch crossing will increase to 200
- Single lepton triggers can not deal with this at current momentum thresholds
- Goal is to use tracking information at hardware based L1 Trigger



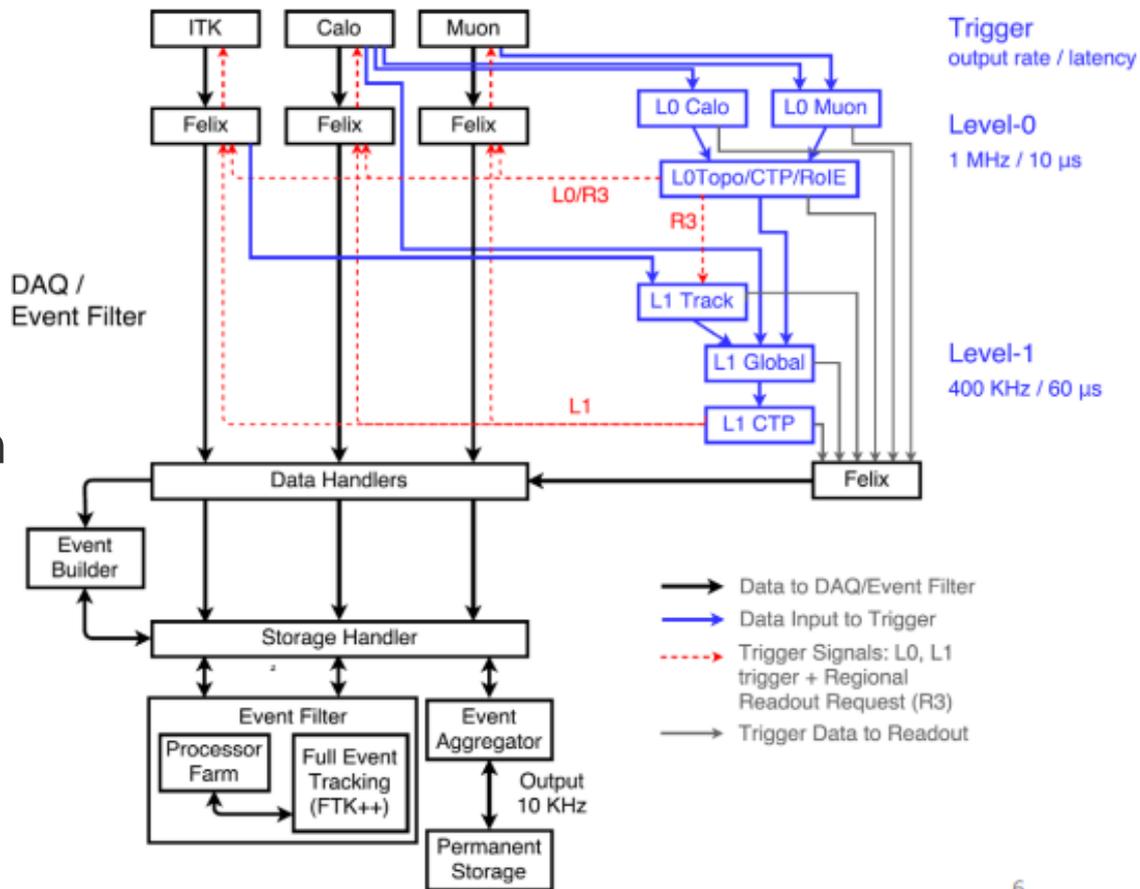
Tracking at High Luminosity LHC

- New all-silicon tracker, ATLAS Inner Tracker (ITK), will be replacing inner detector
- New calorimeter front-end electronics will be replaced to send finer granularity information to trigger at 40 MHz
- Muon spectrometers will be upgraded to include: new small wheel to reject fake muons, new resistive plate chambers for larger acceptance, use of muon drift tubes in 1st level muon trigger
- FTK ++ is an upgraded version of FTK with newer FPGAs and larger number of patterns
 - Will act as HLT co-processor providing global track reconstruction when requested by HLT
 - Looks for tracks > 1 GeV



Tracking at High Luminosity LHC

- L0 trigger will be introduced and operate at 1 MHz, 6 μ s latency
- L1 trigger reduces rate to 400 kHz, latency 24 μ s
 - L1 track trigger is complimentary to FTK++ and will perform tracking in regions of interest for tracks with momentum > 4 GeV
 - L1Global trigger will process finer granularity calorimeter information to improve electron/photon/tau/jets measurement



Conclusion

- ATLAS Fast Tracker (FTK) will reconstruct tracks from all hits and provide them to HLT
- The FTK is being commissioned and integrated into ATLAS, it will be outputting data in some regions by end of 2016
- Tracking at the High Luminosity LHC will include installation of an ATLAS Inner Tracker (ITK), upgrades to the calorimeter electronics, muon hardware upgrades, hardware track finding (L1Track, FTK++), changes in the structure of the trigger

BACKUP

FTK Hardware Status

- >160 mezzanines are produced and tested, at CERN
- 40 DF boards + RTMs produced, 38 boards passed quality tests , 34 are at CERN
- AMB Board + LAMB Versions for AM06 are produced and tested
 - 12 working AM Boards are at CERN
 - 80 LAMBs produced
 - Production of AM06 chip needed for next spring is now starting
- 22 AUX boards tested and working, 18 at CERN
- 10 SSB boards + RTM are assembled , 9 passed tests, 5 are at CERN
- 3 FLIC boards are produced , at CERN



32/32 DF+IMs



16/128 AUX+AMB



8/32 SSB



2/2 FLIC



Boards required for full barrel coverage

- VME Racks
 - 2 racks -1 VME crate each for now
 - “Full Wiener” rack - Wiener bin/PS/fan tray
 - “Custom” rack (Y.05-09.A2) – Wiener bin / CAEN PS and two custom fan trays
 - “Custom” rack will be the prototype of the final version of rack, which we will deploy 4 of them in 2017
- ATCA system is fully installed
 - 2 racks for the DF system each equipped with 2 shelves
 - 1 rack for the FLIC system with 1 shelf

FW DESCRIPTION

IM

DF

Pixel/SCT Hits

Cluster Hits

12 layer hits to
AUX/
4 to SSB

IM

FPGAs

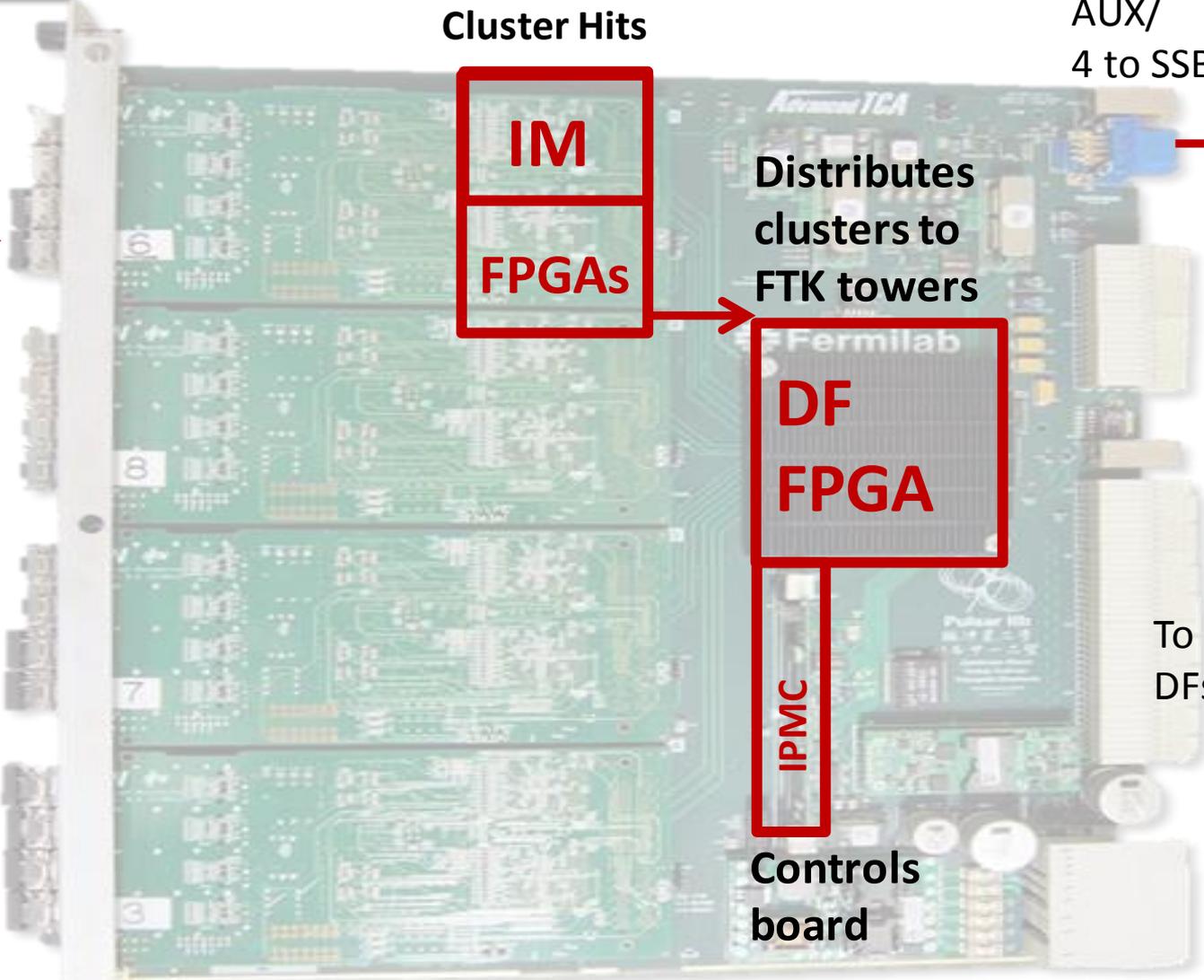
Distributes
clusters to
FTK towers

DF
FPGA

IPMC

Controls
board

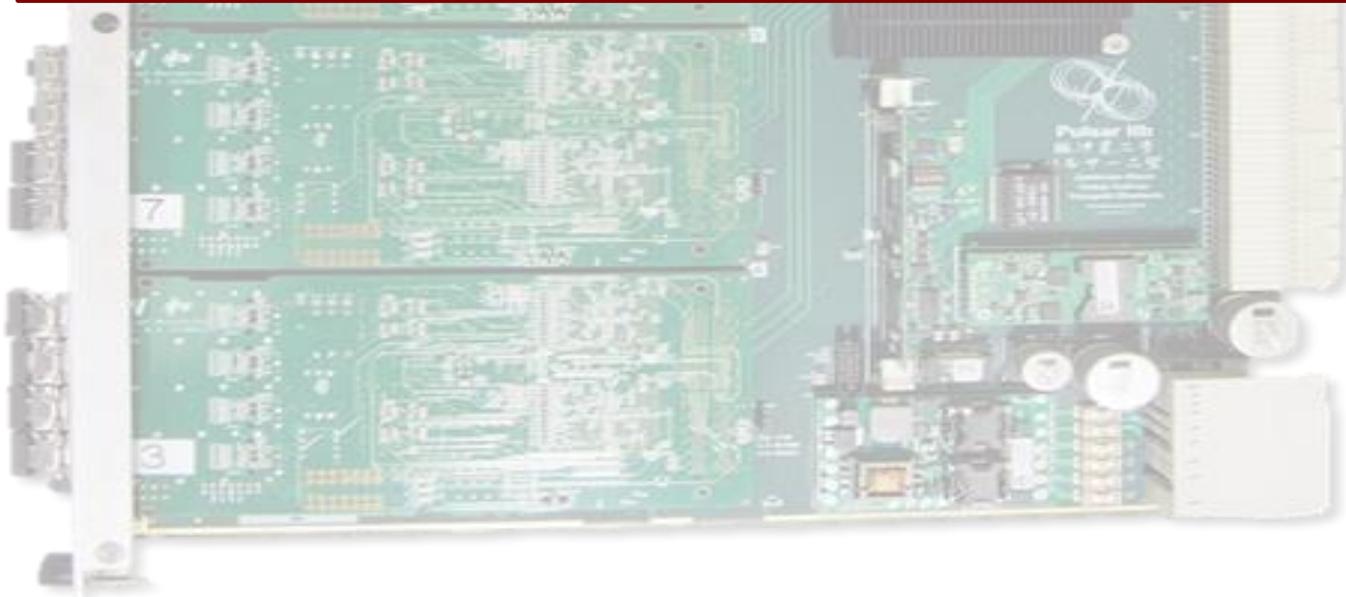
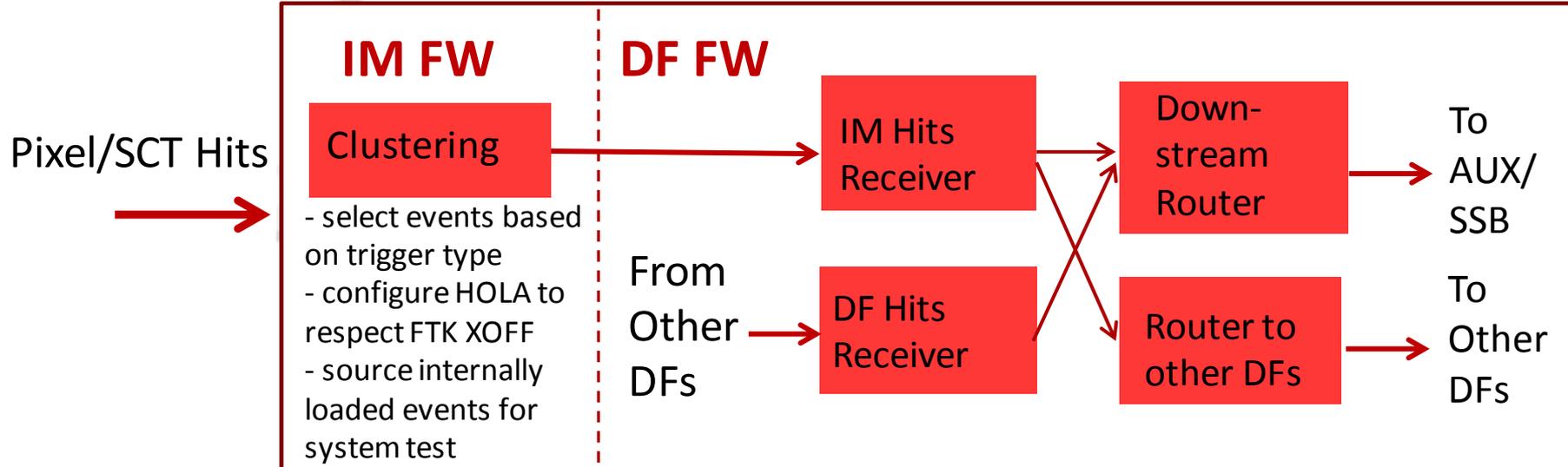
To Other
DFs



IM

DF

FW DESCRIPTION



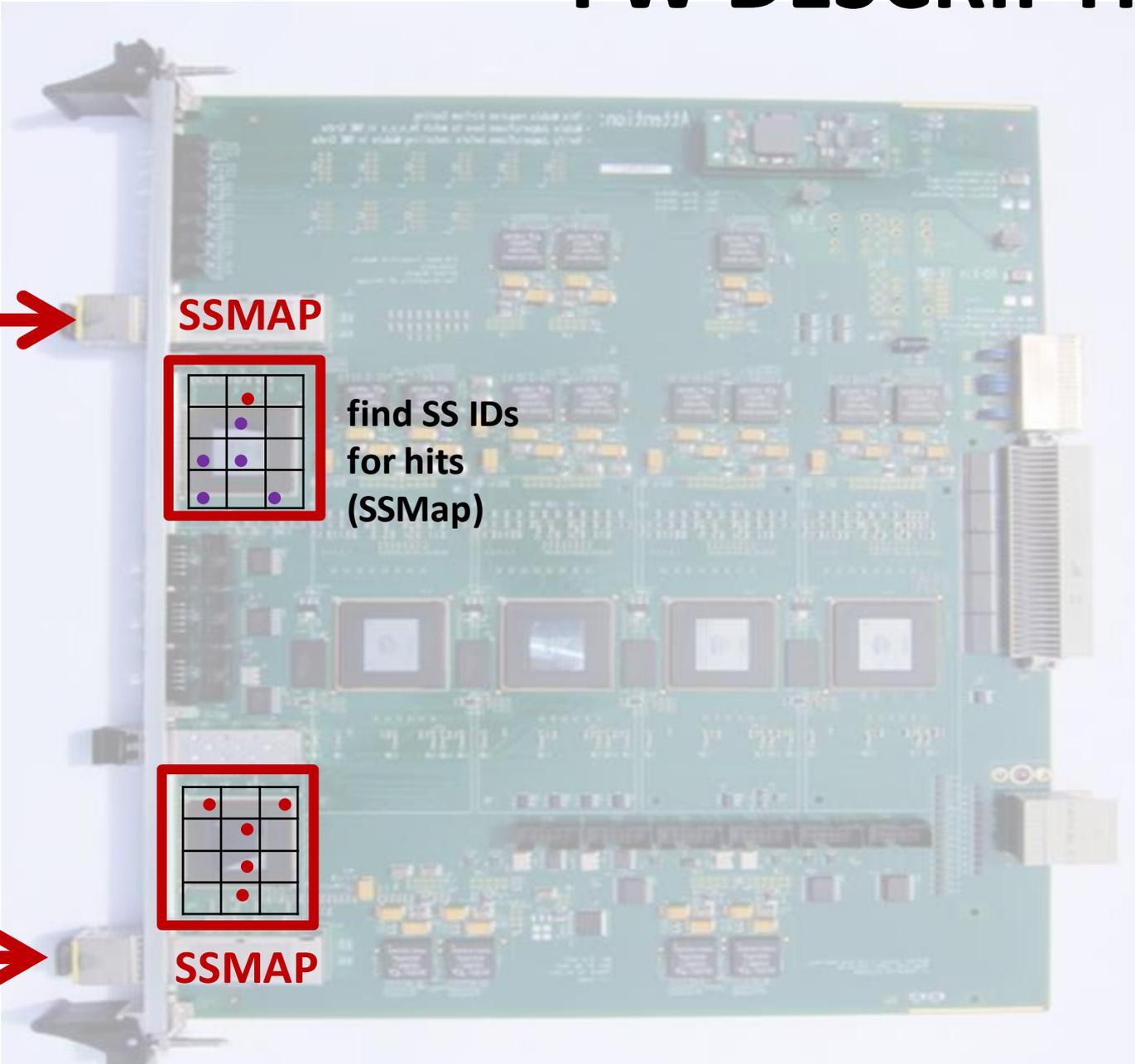
AUX

FW DESCRIPTION

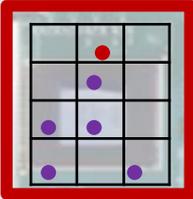
Pix/SCT Hits
from DF

Hits are ganged
into groups of
pixels/SCT
modules called
Super Strips (SS)

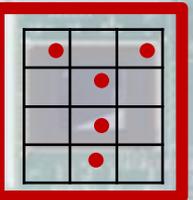
SCT Hits from
DF



SSMAP



find SS IDs
for hits
(SSMap)



SSMAP

AUX

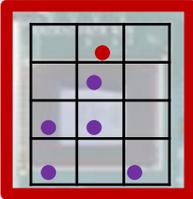
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Pix/SCT Hits
from DF

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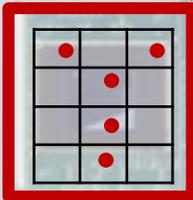
SCT Hits from
DF

SSMAP



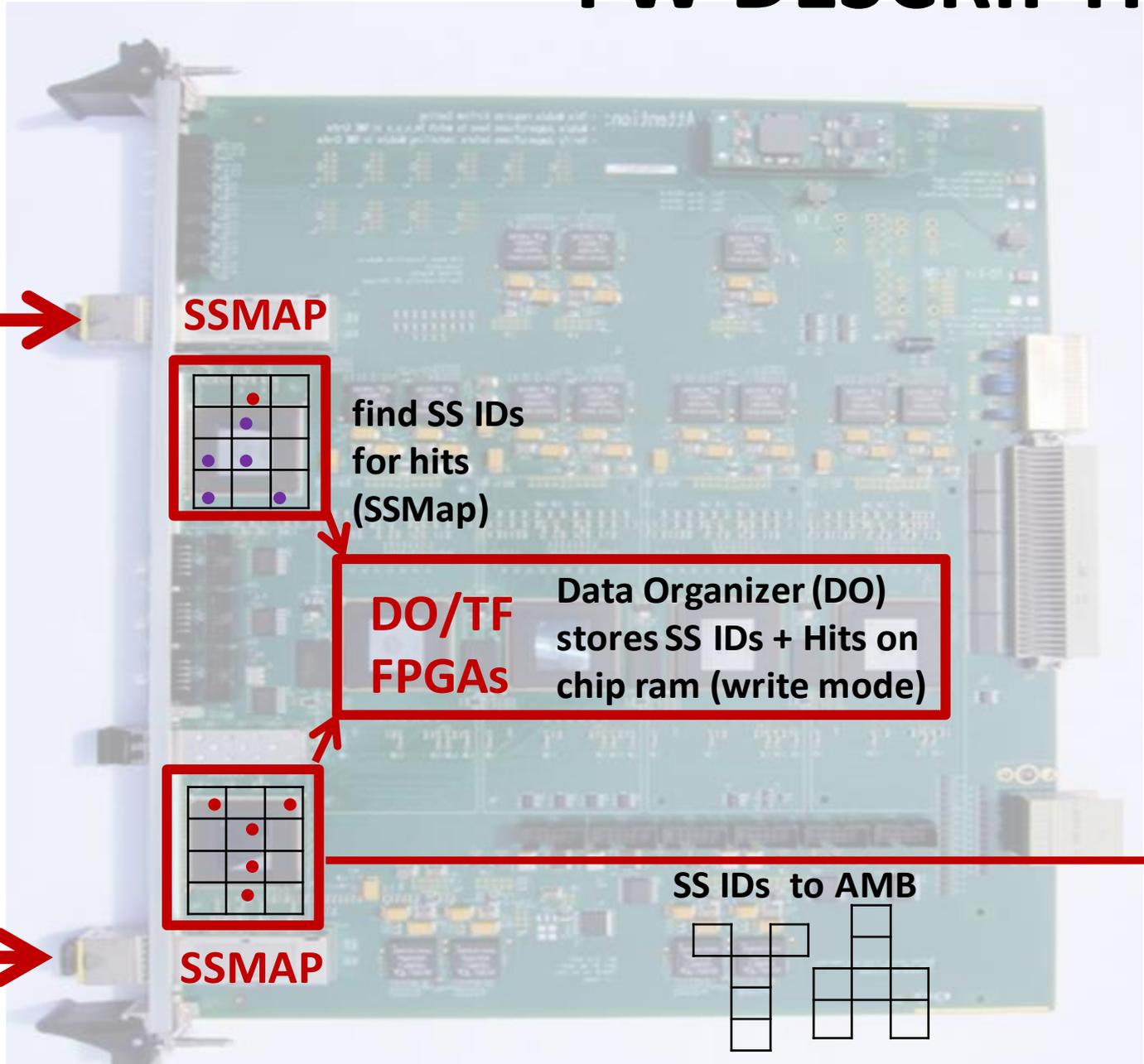
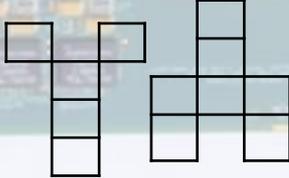
find SS IDs
for hits
(SSMap)

**DO/TF
FPGAs** Data Organizer (DO)
stores SS IDs + Hits on
chip ram (write mode)



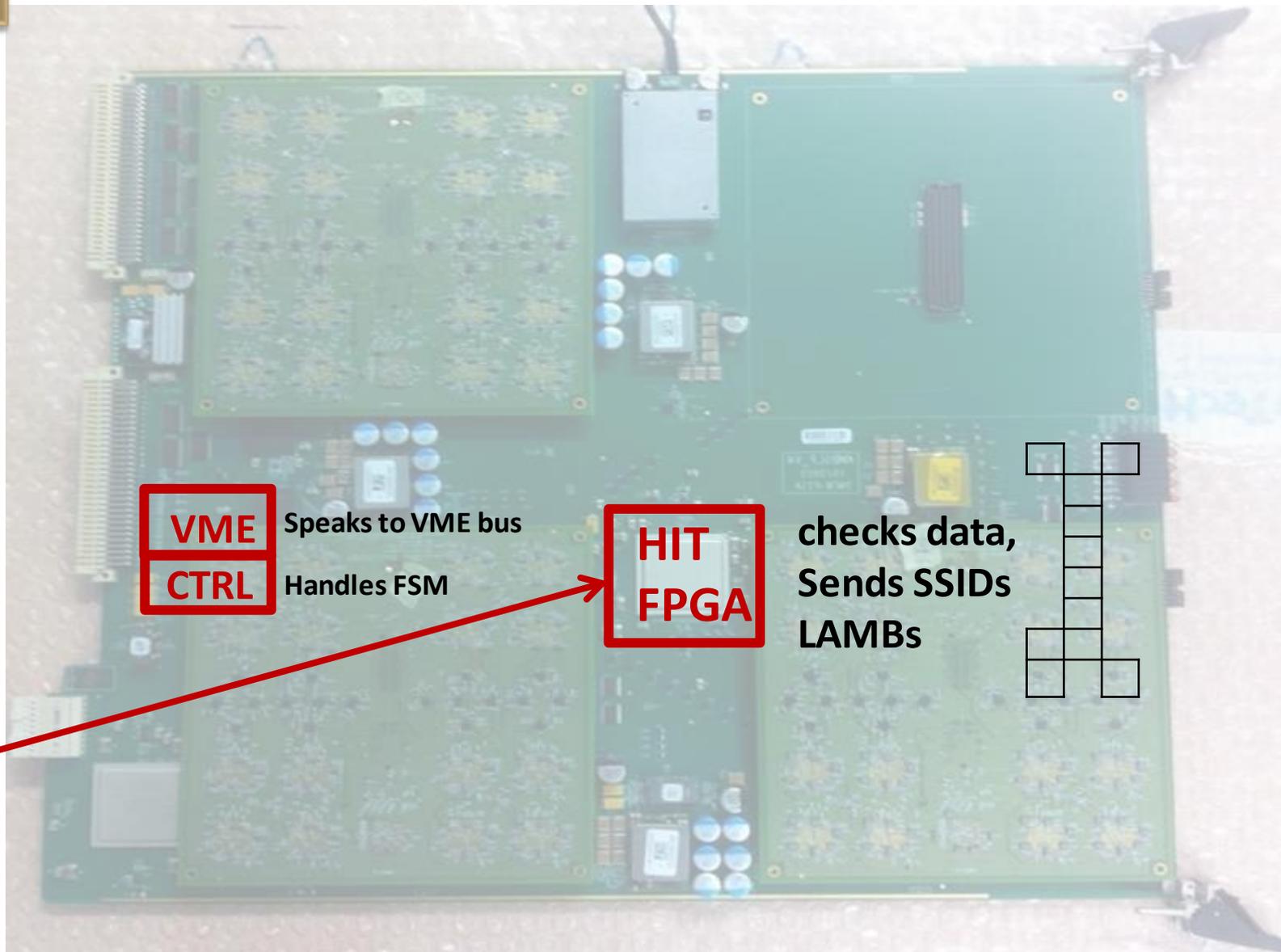
SSMAP

SS IDs to AMB



AMB

FW DESCRIPTION



VME

Speaks to VME bus

CTRL

Handles FSM

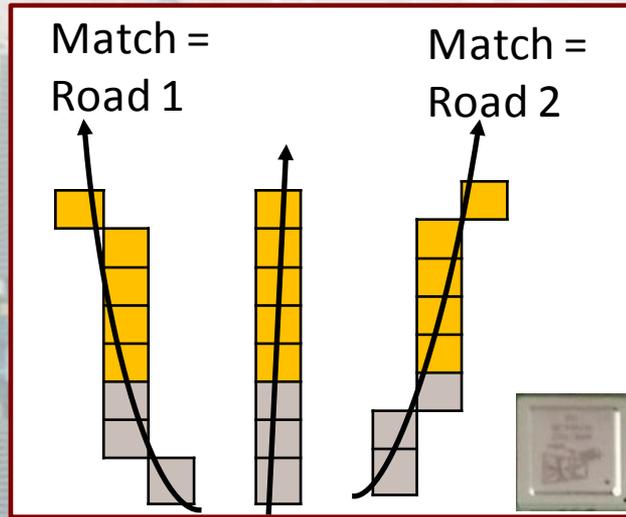
HIT

FPGA

checks data,
Sends SSIDs
LAMBs

SS IDs
from AUX



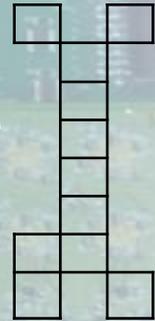


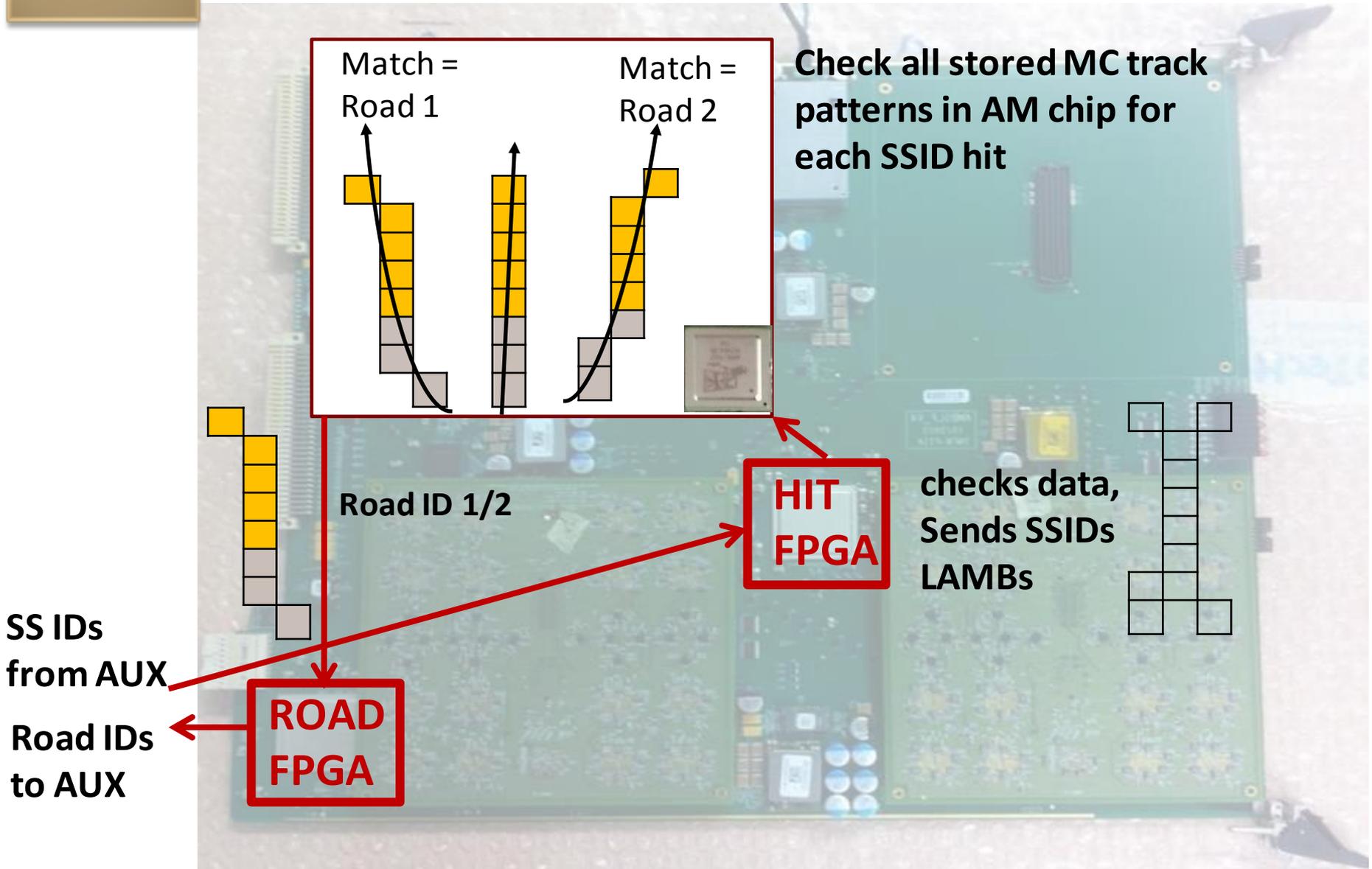
Check all stored MC track patterns in AM chip for each SSID hit

VME Speaks to VME bus
CTRL Handles FSM

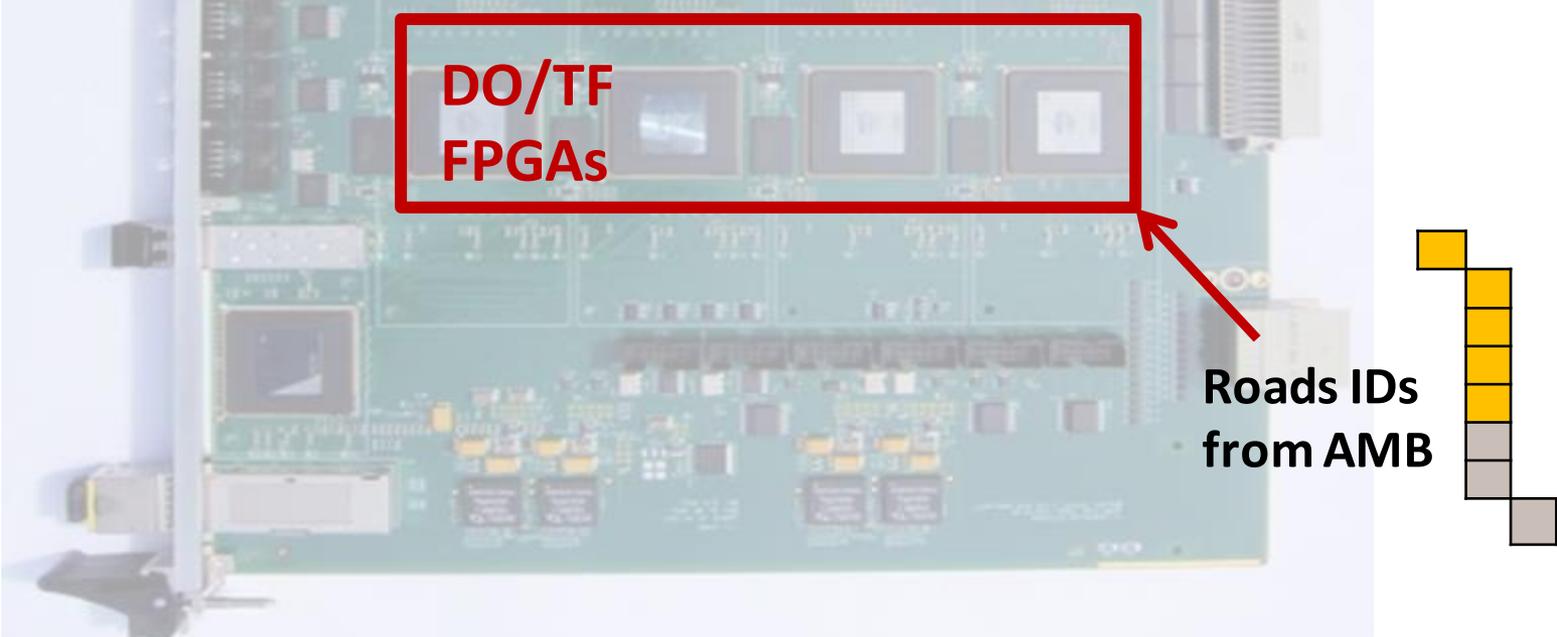
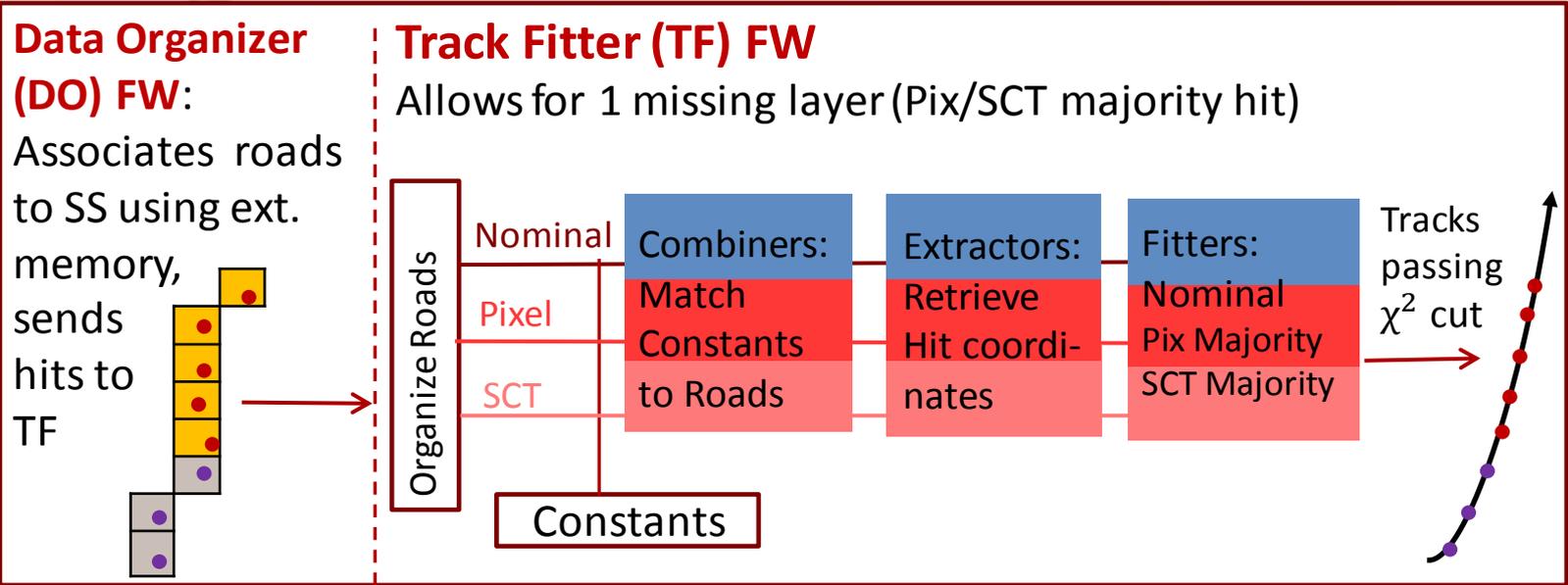
HIT checks data,
FPGA Sends SSIDs
LAMBs

SS IDs from AUX



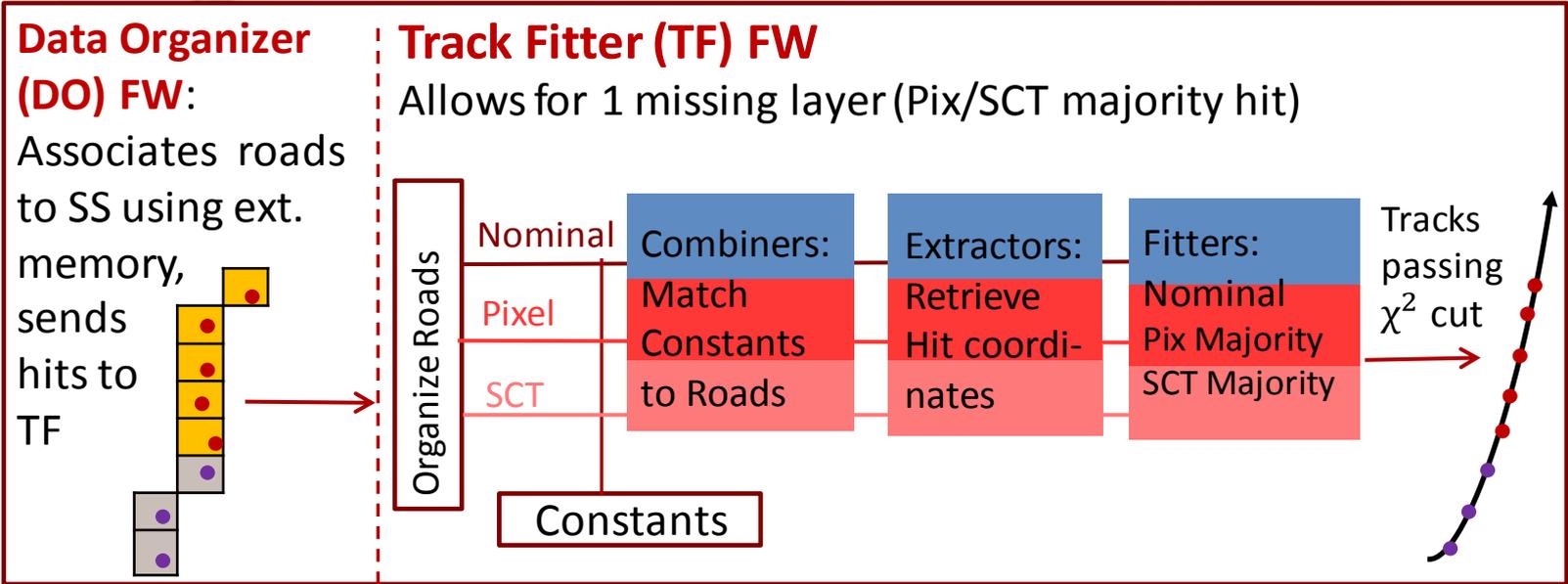


FW DESCRIPTION



AUX

FW DESCRIPTION

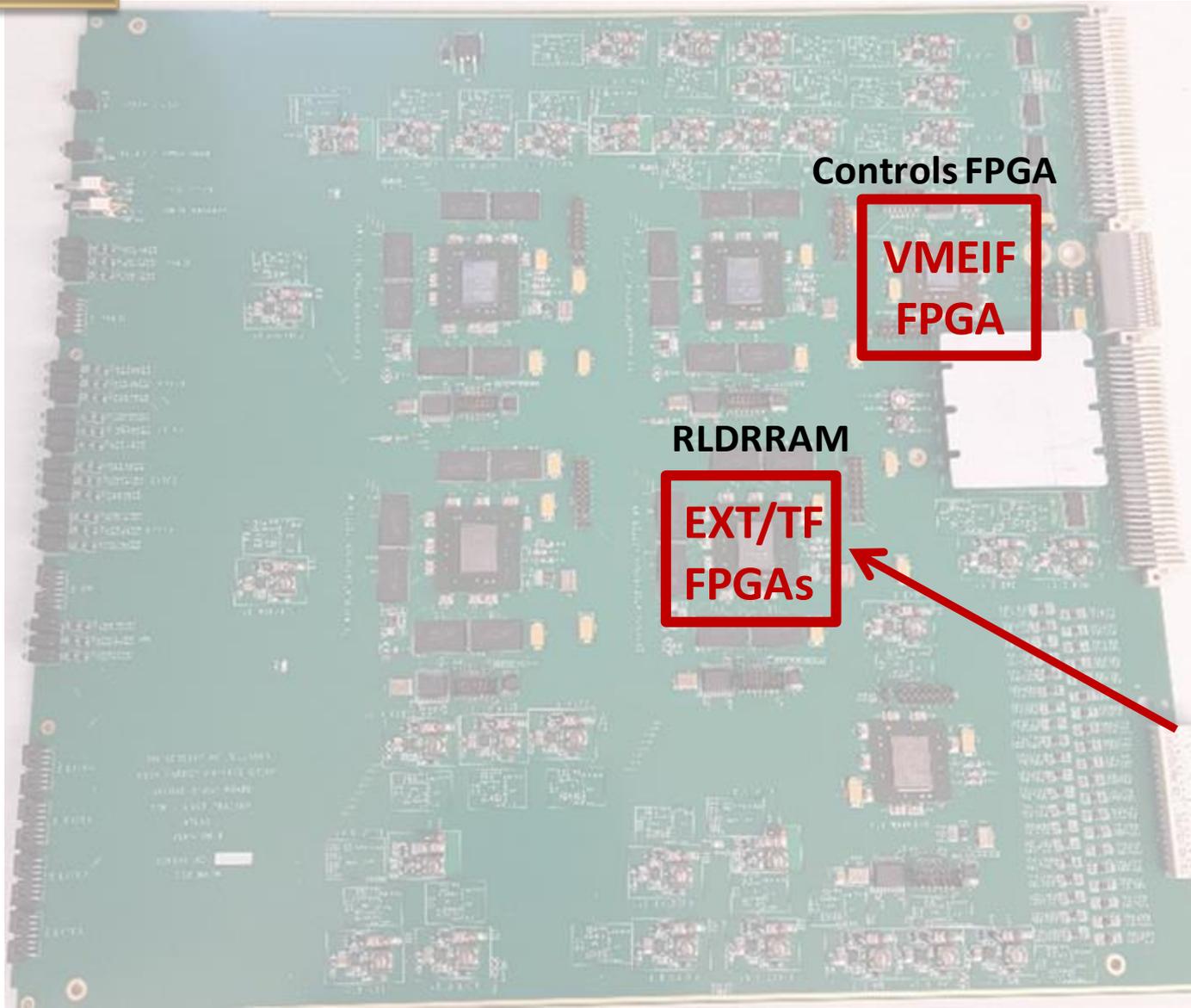


8 layer
Tracks to SSB



FW DESCRIPTION

SSB

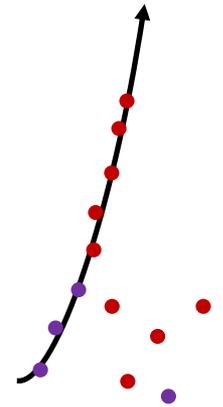


Controls FPGA

VMEIF
FPGA

RLDRAM

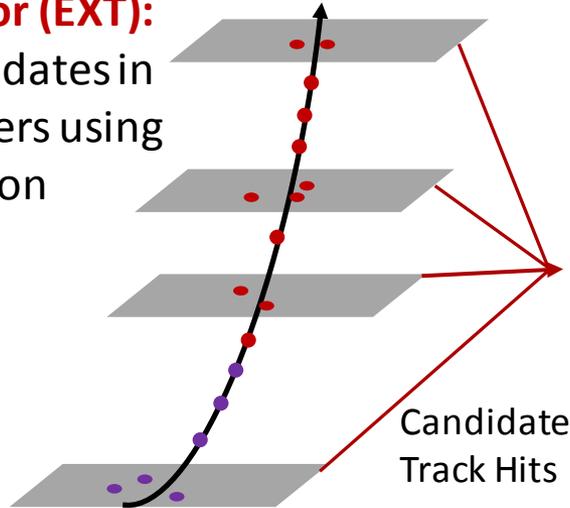
EXT/TF
FPGAs



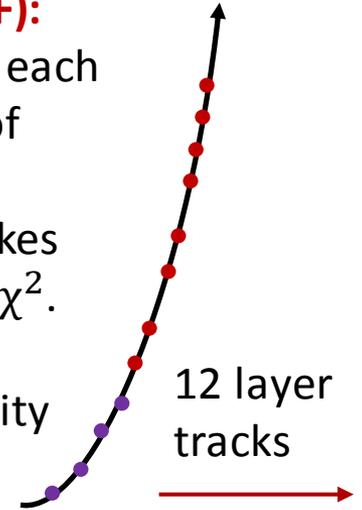
8 layer Tracks
from AUX + 4
layer Hits from DF

Extrapolator (EXT):

Finds candidates in unused layers using extrapolation constants

**Track Fitter (TF):**

Fits track with each combination of possible candidates, takes one with best χ^2 . (Nominal and Pix/SCT Majority Fitters)

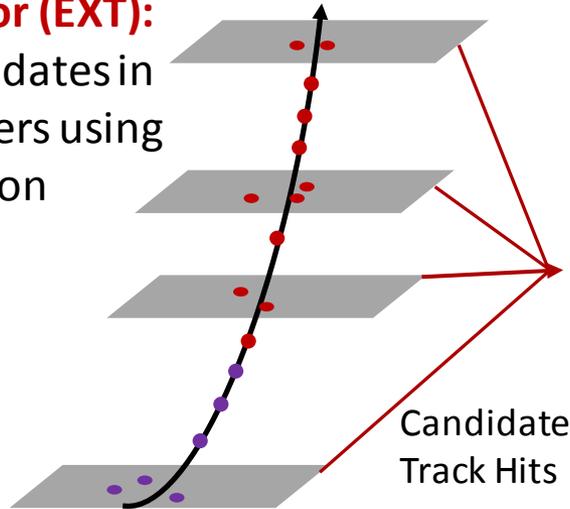


**EXT/TF
FPGAs**

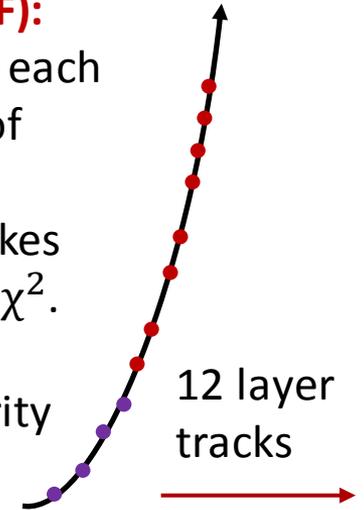
8 layer Tracks
from AUX + 4
layer Hits from DF

Extrapolator (EXT):

Finds candidates in unused layers using extrapolation constants

**Track Fitter (TF):**

Fits track with each combination of possible candidates, takes one with best χ^2 . (Nominal and Pix/SCT Majority Fitters)



**EXT/TF
FPGAs**

**HW
FPGA**

8 layer Tracks
from AUX + 4
layer Hits from DF

Tracks to/from SSB

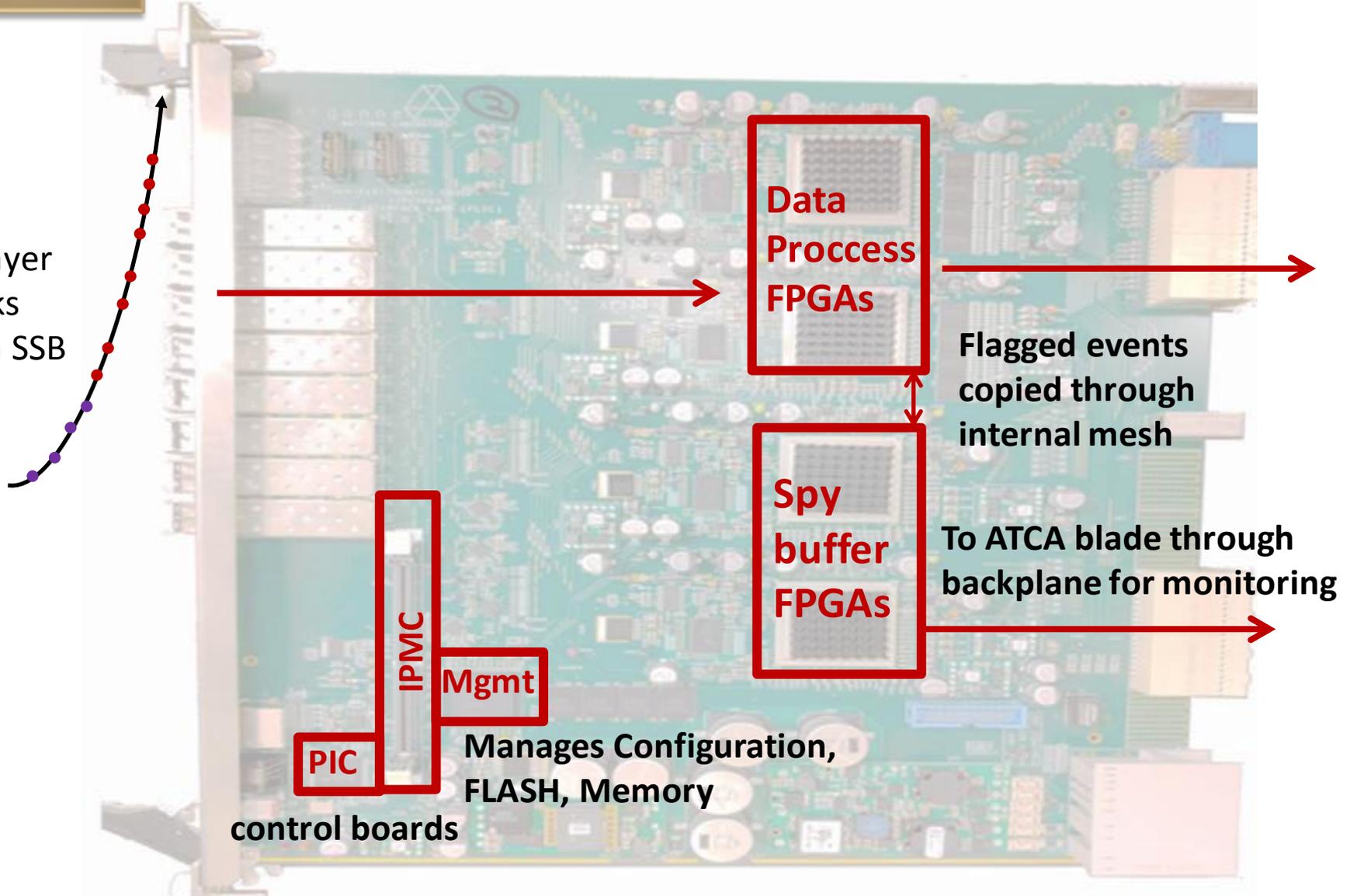
Tracks to FLIC

Hit Warrior (HW) :
removes duplicate
tracks on whole system

FLIC

FW DESCRIPTION

12 layer tracks from SSB



FLIC

FW DESCRIPTION

12 layer tracks from SSB

Data Process FPGAs

To RobinNP

Data Processor FW :
Formats data for HLT

ATLAS Global ID
lookup from
external SRAM

Receive 12
layer tracks

Merge with
input data

Format
for HLT

Copy to spy buffer FPGA

