Microsemi SoC & FPGAs
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European Technical Director

September 2016
Agenda

- SF2/Igloo2
- SmartDebug Advanced Debugging
- LiberoSoC Enhanced Constraints Flow
- SERDES/EPCS mode design tips
- RTG4
Microsemi Company Overview

- **Leading Semiconductor Solutions Differentiated by:**
  - Performance
  - Reliability
  - Security
  - Power
  - Longevity

- **Largest World-Wide Aerospace Semiconductor Supplier**
  - FPGAs
  - Timing
  - Mixed-Signal and RF
  - Discretes
  - Storage
Successful Acquisitions driving.... Broad Product Technology Portfolio

<table>
<thead>
<tr>
<th>Fiscal Year</th>
<th>Company Names</th>
</tr>
</thead>
<tbody>
<tr>
<td>FY2011</td>
<td>ASIC, AML, Actel, BrijoT</td>
</tr>
<tr>
<td>FY2010</td>
<td>White Electronic Designs, VT Silicon, ARXAN Defense</td>
</tr>
<tr>
<td>FY2009</td>
<td>NEXSEM, Spectrum Control Inc., Endwave, Babcock (Power Products Business), (Defense Systems Business)</td>
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<tr>
<td>FY2008</td>
<td>MDT, TSi</td>
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<td>FY2007</td>
<td>PowerDsine</td>
</tr>
<tr>
<td>FY2006</td>
<td>Advanced Power Technology</td>
</tr>
</tbody>
</table>

FY2016: PMC
FY2015: Vitesse, Centellax
FY2013: Symmetricom
FY2012: Zarlink Semiconductor
FY2011: Timing, Synchronization and Synthesis Business

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Microsemi’s BU’s Product Offering

- **SOC: Customizable System-on-Chip Solutions**
  - Low Power, Radiation Tolerant, Crypto Family
  - FPGA + Cortex M3 + Analog (ADC, DAC, Comp, …)

- **CPG: Communications Products**
  - Voice interface, VoIP, Power over Ethernet, WiFi PA, Voice Processor: Acoustic Echo Canceller
  - Timing and Synchronisation, Atomic Clocks, Ethernet PHYs & Switches
  - Low Power ISM Radio

- **PPG: Power Products**
  - Power Discretes: Diodes, MOSFet, IGBT, …
  - « Silicon Carbide » Diodes and Transistors
  - Power Modules, up to 2000V or 800A or 500KHz

- **HRG: Hi-Rel Products**
  - Diodes, Transistors (Bipolar, MOSFet, IGBT, GaN, ..), TVS, …
  - DC/DC, Point-of-Load, Power Supplies, Secured Solid State Memories

- **RFIS: Mixed-signal & RF Integrated Circuits**
  - Diodes, Transistors, up to 5GHz. RF Modules up to 100GHz
SoC Product Group

formerly known as Actel
IGLOO2 FPGAs & SmartFusion2 SoC FPGAs
IGLOO2 FPGAs & SmartFusion2 SoCs

More resources in low density devices
with the lowest power, proven security and exceptional reliability

TS Ethernet MAC
Secure Flash
DDR3 Controller

Low Power
Security
Reliability
# Microsemi FPGA & SoC Families

## Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>SmartFusion ProASIC3, IGLOO</th>
<th>SmartFusion2 IGLOO2</th>
</tr>
</thead>
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<tr>
<td>Logic Elements</td>
<td>100-30K</td>
<td>5K-150K</td>
</tr>
<tr>
<td>Max Transceiver Rate</td>
<td>--</td>
<td>5Gbps</td>
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<tr>
<td>Max I/O Speeds</td>
<td>400Mbps LVDS</td>
<td>667Mbps DDR3</td>
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<tr>
<td>Max I/O Speeds</td>
<td></td>
<td>750Mbps LVDS</td>
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<tr>
<td>Max DSP (18x18 Multipliers)</td>
<td>--</td>
<td>240</td>
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<tr>
<td>Max RAM</td>
<td>144Kb</td>
<td>5Mb</td>
</tr>
<tr>
<td>Processor Options</td>
<td>Soft ARM Cortex-M1</td>
<td>Hard 166 MHz ARM Cortex-M3</td>
</tr>
<tr>
<td></td>
<td>Hard 100 MHz ARM Cortex-M3</td>
<td></td>
</tr>
<tr>
<td>Microsemi Advantages</td>
<td>Lowest Power Proven Security</td>
<td>More Features</td>
</tr>
<tr>
<td></td>
<td>SEU Immunity</td>
<td>Lowest Power Proven Security</td>
</tr>
<tr>
<td></td>
<td>Smallest Form Factor</td>
<td>SEU Immunity</td>
</tr>
</tbody>
</table>

## FPGAs & SoCs With More Resources In Low Density Devices
Differentiated Mainstream FPGA

Flash Based Configuration

Lowest Power Consumption
- 1/10th static power
- Highly optimized SERDES 90mW @ 5Gbps
- Reduce total power by ~30-50%

Highly Optimized SERDES

Highest Security
- Sophisticated key management and distribution
- Built-in clone resistance
- Built-in tamper resistance

Embedded Layers of Security

Highest Reliability
- SEU immune FPGA configuration
- Extensive temperature support
- Multiple generation of defense and space grade products

Microsemi and partner solutions

System Solutions
- IEEE1588
- Carrier Ethernet OAM
- Secure Boot

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Power Matters.™
FPGAs & SoCs Deliver More Resources With Lowest Power, Proven Security And Exceptional Reliability

- 16x 5Gbps SERDES, PCIe, XAUI / XGXS+ Native SERDES
- Up to 150K LEs, 5Mbit SRAM, 4Mbit eNVM
- Hard 667 mbps DDR2/3 controllers
- Integrated DSP processing blocks
- SmartFusion2 166MHz ARM® Cortex™-M3 w/ on chip eSRAM & eNVM
  - Includes ETM and Instruction Cache
  - Extensive peripherals CAN, TSE, USB

- Lowest Power
  - As low as 7mW Standby, Typical

- Proven Security
  - DPA Hardened, AES256, SHA256, On-Demand NVM Data Integrity Check

- Exceptional Reliability
  - SEU immune Zero FIT Flash FPGA Configuration
  - SEU Protected/Tolerant Memories: eSRAMs, DDR Bridges (MSS, MDDR, FDDR), Instruction Cache, Ethernet, CAN and USB Buffers, PCIe, MMUART and SPI FIFOs
SmartFusion2 Architecture
Low Power: Flash Based Configuration

- Atrocious high static power in SRAM FPGAs
  - Six-transistor SRAM cells Vs single-transistor FLASH cell

**Typical Competitors**

**SRAM Cell**

- Substantial Leakage per Cell
- High Static Current

**Flash Cell**

- 1000x lower leakage per cell
- Ultra Low Static Current

*Flash FPGAs inherently lower power*
SmartFusion2: Consumes 34-53% Less Power

Total Power Consumption

- **Cyclone V SX** consumes 52% more power
- **Zynq** consumes 113% more power
- **SmartFusion2** consumes less power

Measured at $T_j = 100^\circ C$, worst case conditions

Note: Flash*Freeze mode will yield larger differences

With 1V devices

**Power Matters.™**

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IGLOO2: Consumes 17-31% Less Power

Total Power Consumption

Cyclone V GX consumes 39% more power

Artix-50 consumes 21% more power

IGLOO2 consumes less power

Artix-7 consumes 46% more power

Measured at $T_J = 100\,^{\circ}\text{C}$, worst case conditions

Note: Flash*Freeze mode will yield larger differences

35% Lower With 1V devices

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The Most Reliable FPGA In the Industry

- **Flash FPGA Fabric**
  - SEU Immune Zero FIT rate configuration

- **Error Corrected Memories**
  - Embedded 32 Kbyte SRAM (eSRAM)
  - Built-in DDR Controllers
  - MSS
    - CAN, USB, TSE

- **HPMS/MSS memories constructed from standard cell components not SRAM**
  - Instruction cache
  - Peripheral Buffers

*Reliability for safety critical or mission critical systems*
RAM Multiple Bit Upsets immunity by design

- **Normal SRAM Memory design**
  - A single radiation event can cause a multiple-bit upset (MBU).
  - If the SRAM bits in a logical word are physically adjacent, the MBU can result in uncorrectable errors.
  - For example, words D and E have uncorrectable multi-bit errors.

- **Microsemi “scrambled” Memory design technique**

- **Absence of multiple bit upsets in all testing in SmartFusion2/Igloo2**
  - In Microsemi FPGAs, the SRAM bits in each logical word are physically separated, and the probability of the MBU resulting in uncorrectable errors is dramatically reduced.
  - For example, words D, E, F, and G have single-bit errors which are correctable.
# Reliability: Flash vs SRAM Configuration SEU Immunity

<table>
<thead>
<tr>
<th>FPGA</th>
<th>Technology</th>
<th>Ground-Level Applications</th>
<th>Commercial Aviation</th>
<th>Military Aviation</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Sea Level</td>
<td>5,000 Ft</td>
<td>30,000 Ft</td>
</tr>
<tr>
<td><strong>Microsemi SmartFusion2</strong></td>
<td>65nm Flash</td>
<td>No Failures Detected</td>
<td>No Failures Detected</td>
<td>No Failures Detected</td>
</tr>
<tr>
<td><strong>Xilinx XC6SLX25</strong></td>
<td>45nm SRAM</td>
<td>870 FITs</td>
<td>3,000 FITs</td>
<td></td>
</tr>
<tr>
<td><strong>Xilinx XC6SLX45</strong></td>
<td>45nm SRAM</td>
<td>1,600 FIT</td>
<td>5,500 FITs</td>
<td></td>
</tr>
<tr>
<td><strong>Altera EP3C25</strong></td>
<td>65nm SRAM</td>
<td>580 FITs</td>
<td>1,900 FITs</td>
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</tr>
<tr>
<td><strong>Altera EP3C55</strong></td>
<td>65nm SRAM</td>
<td>1,500 FITs</td>
<td>5,000 FITs</td>
<td></td>
</tr>
<tr>
<td><strong>Altera EP3C120</strong></td>
<td>65nm SRAM</td>
<td>2,900 FITs</td>
<td>9,700 FITs</td>
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</tr>
<tr>
<td><strong>Altera EPCGX50</strong></td>
<td>60nm SRAM</td>
<td>2,500 FITs</td>
<td>8,200 FITs</td>
<td></td>
</tr>
<tr>
<td><strong>Lattice ECP4-50</strong></td>
<td>65nm SRAM</td>
<td>1,400 FITs</td>
<td>4,600 FITs</td>
<td></td>
</tr>
<tr>
<td><strong>Lattice ECP4-130</strong></td>
<td>65nm SRAM</td>
<td>3,700 FITs</td>
<td>12,000 FITs</td>
<td></td>
</tr>
</tbody>
</table>

FIT = number of errors in $10^9$ hours

Acceptable FIT rates for commercial applications are < 100

Acceptable FIT rates for high-reliability applications are < 20

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SmartFusion2 based on test chip data
Xilinx data – 136 FIT/Mb reported in Xilinx Reliability Data
Altera, Lattice data – estimated at 100 FIT/Mb
SmartFusion2 SoC FPGAs
SmartFusion2 Architecture
SmartFusion2 Microcontroller Subsystem

- 166 MHz ARM Cortex-M3 with Instruction Cache
- 4 Port DDR bridge for data caching
- HS USB OTG
- 10/100/1000 Triple Speed Ethernet
- CAN 2.0a/b with 32 transmit and receive message buffers
- All memories SEU tolerant or SECDED.
- Equivalent to >35K LE’s
# SmartFusion2 Product Family

<table>
<thead>
<tr>
<th>Features</th>
<th>M2S005</th>
<th>M2S010</th>
<th>M2S025</th>
<th>M2S050</th>
<th>M2S060</th>
<th>M2S090</th>
<th>M2S150</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Logic/DSP</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Maximum Logic Elements (4LUT + DFF)(^1)</td>
<td>6,060</td>
<td>12,084</td>
<td>27,696</td>
<td>56,340</td>
<td>56,520</td>
<td>86,184</td>
<td>146,124</td>
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<tr>
<td>Math Blocks (18x18)</td>
<td>11</td>
<td>22</td>
<td>34</td>
<td>72</td>
<td>72</td>
<td>84</td>
<td>240</td>
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<tr>
<td>Fabric Interface Controllers (FICs)</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td></td>
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<tr>
<td>PLLs and CCCs</td>
<td>2</td>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>8</td>
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<tr>
<td>Data Security</td>
<td>AES256, SHA256, RNG</td>
<td>A</td>
<td>S</td>
<td>2</td>
<td>512</td>
<td></td>
<td></td>
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<tr>
<td><strong>MSS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cortex-M3 + Instruction cache</td>
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<td></td>
<td></td>
<td></td>
<td>Yes</td>
<td></td>
<td></td>
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<tr>
<td>eNVM (K Bytes)</td>
<td>128</td>
<td></td>
<td>256</td>
<td></td>
<td></td>
<td>512</td>
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<tr>
<td>eSRAM (K Bytes)</td>
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<td></td>
<td></td>
<td>64</td>
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<tr>
<td>eSRAM (K Bytes) Non SECDED</td>
<td></td>
<td></td>
<td></td>
<td>80</td>
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<tr>
<td>CAN, 10/100/1000 Ethernet, HS USB</td>
<td></td>
<td></td>
<td></td>
<td>1 each</td>
<td></td>
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<td></td>
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<tr>
<td>Multi-Mode UART, SPI, I2C, Timer</td>
<td></td>
<td></td>
<td></td>
<td>2 each</td>
<td></td>
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</tr>
<tr>
<td><strong>Fabric Memory</strong></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>LSRAM 18K Blocks</td>
<td>10</td>
<td>21</td>
<td>31</td>
<td>69</td>
<td>69</td>
<td>109</td>
<td>236</td>
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<tr>
<td>uSRAM1K Blocks</td>
<td>11</td>
<td>22</td>
<td>34</td>
<td>72</td>
<td>72</td>
<td>112</td>
<td>240</td>
</tr>
<tr>
<td>Total RAM (K bits)</td>
<td>191</td>
<td>400</td>
<td>592</td>
<td>1314</td>
<td>1314</td>
<td>2074</td>
<td>4488</td>
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<tr>
<td><strong>High Speed</strong></td>
<td></td>
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<tr>
<td>DDR Controllers (Count x Width)</td>
<td>1x18</td>
<td>2x36</td>
<td>1x18</td>
<td>1x18</td>
<td>2x36</td>
<td>2x36</td>
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<tr>
<td>SERDES Lanes (T)</td>
<td>0</td>
<td>4</td>
<td>8</td>
<td>4</td>
<td>4</td>
<td>16</td>
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<tr>
<td>PCIe End Points</td>
<td>0</td>
<td>1</td>
<td></td>
<td>2</td>
<td></td>
<td>4</td>
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<tr>
<td><strong>User I/Os</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>MSIO (3.3V)</td>
<td>115</td>
<td>123</td>
<td>157</td>
<td>139</td>
<td>271</td>
<td>309</td>
<td>292</td>
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<tr>
<td>MSIOD (2.5V)</td>
<td>28</td>
<td>40</td>
<td>40</td>
<td>62</td>
<td>40</td>
<td>40</td>
<td>106</td>
</tr>
<tr>
<td>DDRIO (2.5V)</td>
<td>66</td>
<td>70</td>
<td>70</td>
<td>176</td>
<td>76</td>
<td>76</td>
<td>176</td>
</tr>
<tr>
<td>Total User I/O</td>
<td>209</td>
<td>233</td>
<td>267</td>
<td>377</td>
<td>387</td>
<td>425</td>
<td>574</td>
</tr>
</tbody>
</table>

- Total logic may vary based on utilization of DSP and memories in your design. Please see the IGLOO2 Fabric UG for details
- Feature availability is package dependent
# SmartFusion2 Packaging Options

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<th>Package Options^4</th>
<th>FCSG325</th>
<th>VFG256</th>
<th>FCSG536</th>
<th>VFG400</th>
<th>FCVG484</th>
<th>TQG144</th>
<th>FGG484</th>
<th>FGG676</th>
<th>FGG896</th>
<th>FCG1152</th>
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<tbody>
<tr>
<td><strong>Type</strong></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
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</tr>
<tr>
<td>Pitch (mm)</td>
<td>0.5</td>
<td>0.8</td>
<td>0.5</td>
<td>0.8</td>
<td>0.8</td>
<td>0.5</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>Length x Width (mm)</td>
<td>11x11</td>
<td>14x14</td>
<td>16x16</td>
<td>17x17</td>
<td>19x19</td>
<td>20x20</td>
<td>23x23</td>
<td>27x27</td>
<td>31x31</td>
<td>35x35</td>
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<tr>
<td><strong>Device</strong></td>
<td></td>
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<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I/O Lanes</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M2S005 (S)</td>
<td>161</td>
<td>171</td>
<td>84</td>
<td>209</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>M2S010 (S/T/TS)^5</td>
<td>138</td>
<td>195</td>
<td>84</td>
<td>233</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M2S025 (T/TS)^1</td>
<td>180</td>
<td>207</td>
<td>267</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M2S050 (T/TS)^1</td>
<td>200</td>
<td>207</td>
<td>267</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M2S060 (T/TS)^1</td>
<td>200</td>
<td>207</td>
<td>267</td>
<td>4</td>
<td>387</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>M2S090 (T/TS)^1,5</td>
<td>180</td>
<td>207</td>
<td>267</td>
<td>4</td>
<td>425</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M2S150 (T/TS)^3</td>
<td>293</td>
<td>248</td>
<td>574</td>
<td>16</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

1. Mil Temp 010/025/050/060/090 devices are only available in the FGG484 package
2. 090 FCSG325 is 11x13.5 pkg dim
3. Mil Temp 150 devices are only available in the FCG1152 package
4. All the packages mentioned above are available with lead and lead free
5. M2S010 (S) device is only available in TQG144 package
6. The M2S090(T/TS) device in the FCSG325 package is available with an ordering code of XZ48. The XZ48 ordering code pre-configures the device for Auto Update mode. Minimum Order quantities apply, contact your local Microsemi sales office for details.

Can migrate vertically in the same package
FPGA Logic Element

- A fully permutable 4-input LUT
- A dedicated carry chain based on the carry look-ahead technique
- A separate flip-flop which can be used independently from the LUT
FPGA Memory Blocks – Large SRAM

- RAM 18,432 bits
  - Dual Port Configuration
    - Both ports are 18 bits wide or less
    - 1kx18, 2kx9, 4kx4, 8kx2, 16kx1
  - Two Port Configuration
    - One port at least 36 bits wide
    - Other port is either
      - 36, 18, 9, 4, 2 or 1 bit wide
  - High performance synchronous operation
    - 400 MHz

Ideal for creating larger memories
FPGA Memory Blocks – µRAM

- µRAM1K bit
  - 18-bit Three Port Memory (2 Reads and 1 Write)
  - Synchronous Writes - always
  - Asynchronous or Synchronous Read Operation
  - 400 MHz
    - Sync Write, Sync Read
  - Configurations
    - 64x18, 128x9, 256x4, 512x2, and 1024x1
  - Implemented as a register file

Ideal for small memory, small FIFO, register file, and small DSP look-up tables
FPGA Math Block

- 11 to 240 math blocks
- Supports 18 x 18 signed, 17 x 17 unsigned
- Internal cascade signals (44-bit CDIN and CDOUUT) to support larger accumulators/adders/subtracters without extra logic
- Loopback capability to support adaptive filtering
- Adder support: \((A \times B) + C\) or \((A \times B) + D\) or \((A \times B) + C + D\)
SERDES Features

- PMA Layer – Electrical Layer (Physical Medium Attachment)
  - 1Gbps to 5Gbps data rates
  - Special Electrical Idle and PCIe Connection Detection Functions

- PCS Layer - (Physical Coding Sublayer)
  - PCI Express Gen1/Gen2 x1, x2, x4
  - 10G Ethernet Physical Layer (XAUI)
  - EPCS Interface (External Physical Coding Sublayer)
    - Direct FPGA access to SERDES (no PCS layer)

- Arranged in groups of 4 SERDES Lanes

<table>
<thead>
<tr>
<th></th>
<th>SmartFusion2</th>
<th>M2S010</th>
<th>M2S025</th>
<th>M2S050</th>
<th>MS2060</th>
<th>M2S090</th>
<th>M2S150</th>
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<td>IGLOO2</td>
<td>M2GL010</td>
<td>M2GL025</td>
<td>M2GL050</td>
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<td>8</td>
<td>4</td>
<td>4</td>
<td>16</td>
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</tr>
</tbody>
</table>
SERDES / Hard IP architecture

PMA - Multi-Protocol 5G transceiver
Organized in blocks of x4
4 blocks max for 16 lanes
Multi Protocol 5Gb/s SERDES

- Physical Media Attachment (PMA) Features
  - Up to 16 lanes at up to 5Gbps
  - Dual based reference clocks with single-lane rate granularity
    - Tx and Rx PLLs programmable for each lane
    - Reference clock is shared per groups of two lanes
  - Transmitter Features
    - Programmable Pre/Post-Emphasis
    - Programmable Impedance
    - Programmable Amplitude
  - Receiver Features
    - Programmable Termination
    - Programmable Linear Equalization
  - Built-In System Debug Features
    - PRBS Gen/Chk
    - Constant Patterns
    - Loopbacks

Eye Diagram
SERDES Rate Granularity

Dual based reference clocks with single-lane rate granularity

- Tx and Rx PLLs programmable for each channel
- Reference clock is shared per groups of two lanes

Example Scenario

- REFCLK0 at 100MHz
  - Lane0 at 5.0Gbps
  - Lane1 at 5.0Gbps
- REFCLK1 at 125MHz
  - Lane2 at 2.5Gbps
  - Lane3 at 3.125Gbps

- Special connectivity for x4 usage using single reference clock.
Hard IP - SERDES-Based Protocol Features

- PCI Express Gen1/Gen2 Controller
  - Single-Function Endpoint Configuration
  - x1, x2, x4 Link Widths
    - Static Lane Reversal support
  - 256 Bytes Maximum Payload Size
  - 64/32-Bit AXI/AHB Master/Slave Interfaces to FPGA
  - APB Interface for control/status

- XAUI/XGXS Physical Layer
  - Full compliance with IEEE 802.3
  - 64-Bit XGMII to FPGA at 156.25MHz
  - MDIO Interface for status/control (802.3ae-clause 45)
Embedded DDR Memory Interfaces

- Up to 2 High Speed 667Mb/s DDRx Memory Controllers plus PHY
  - MSS DDR or MDDR available on all devices
    - Connects to embedded AHB and HPDMA Controller
    - Connects directly to FPGA Fabric
  - FDDR available on larger devices
    - Connects directly to FPGA Fabric
- Supports LPDDR/DDR2/DDR3
  - Burst lengths of 2, 4, 8, or 16
- AMBA AXI or AHB interface
- SECDED Supported
- Supports Command and Data Reordering
- Supports Dynamic changing clock frequency in Self-Refresh.
- External Memory Configurations
  - Memory densities up to 4 GB
  - Maximum of 8 memory banks
  - 1, 2, or 4 ranks of memory
  - Bus Width Modes of x8, x9, x16, x18, x32, x36
# I/O Standard Summary

<table>
<thead>
<tr>
<th>I/O Standards</th>
<th>I/O Types</th>
<th>MSIO</th>
<th>MSIOD</th>
<th>DDRIO</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Single-Ended I/O</strong></td>
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<td>LVTTL 3.3V</td>
<td>Yes</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>LVCMOS 3.3V</td>
<td>Yes</td>
<td></td>
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<tr>
<td>PCI</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
<td></td>
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<tr>
<td>LVCMOS 1.2V</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>LVCMOS 1.5V</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>LVCMOS 1.8V</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>LVCMOS 2.5V</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
<td>Yes</td>
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<tr>
<td><strong>Voltage-Referenced I/O</strong></td>
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<tr>
<td>HSTL 1.5V</td>
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<td></td>
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<td>Yes</td>
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<tr>
<td>SSTL 1.8V</td>
<td>-</td>
<td></td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>SSTL 2.5V</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>SSTL 2.5V (DDR1)</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>SSTL 1.8V (DDR2)</td>
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<td>Yes</td>
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<tr>
<td>SSTL 1.5V (DDR3)</td>
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<td>Yes</td>
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<tr>
<td><strong>Differential I/O</strong></td>
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<tr>
<td>LVPECL (input only)</td>
<td>Yes</td>
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<tr>
<td>LVDS 3.3V</td>
<td>Yes</td>
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<tr>
<td>LVDS 2.5V</td>
<td>Yes</td>
<td>Yes</td>
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<td>RSDS</td>
<td>Yes</td>
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<td>BLVDS</td>
<td>Yes</td>
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<td>MLVDS</td>
<td>Yes</td>
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<tr>
<td>Mini-LVDS</td>
<td>Yes</td>
<td>Yes</td>
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</table>
IGLOO2 FPGAs
IGLOO2 Architecture

Up to 16 Lanes Multi Protocol 5G SERDES
- PMA
- PCI Express x1,x2,x4
- XAUI XGXS
- Direct Attach x1,x2,x4

High Performance Memory Subsystem
- AHB Bus Matrix
- COMM_BLK
- SPI
- eNVM
- eSRAM_0
- eSRAM_1
- PDMA
- HPDMA
- DDR Bridge

System Security
- AES256
- SHA256
- ECC
- NRBG
- SRAM-PUF

FPGA Fabric
- Up to 150K Logic Elements
- Math Blocks (18x18)
- Micro SRAM (64x18)
- Large SRAM (1024x18)

Multi-Standard GPIO
(1.2 – 3.3 V, LVDS, HSTL/SSTL)
High Performance Memory Subsystem

- Included in every device!
  - No other non SoC FPGA has this

- Reduces your design effort, power, and cost

- Embedded memories
  - eNVM – Flash – up to 512KByte
    - Use to secure boot code of an external application processor
  - 32KByte Embedded SRAM’s (2.6Gbps of bandwidth)

- Built-in support for managing embedded memories
  - 2 DMA Engines to move data efficiently in and out of the device
  - DDR bridge – 2 port memory cache
    - Lowers power and increases system throughput

*Embedded Memories with Commonly Used Functions in Serial Protocol Implementations Saves 18K LEs!*
## IGLOO2 Product Family

<table>
<thead>
<tr>
<th>Features</th>
<th>M2GL005</th>
<th>M2GL010</th>
<th>M2GL025</th>
<th>M2GL050</th>
<th>M2GL060</th>
<th>M2GL090</th>
<th>M2GL150</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic/DSP</td>
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<td>Maximum Logic Elements (4LUT + DFF)</td>
<td>6,060</td>
<td>12,084</td>
<td>27,696</td>
<td>56,340</td>
<td>56,520</td>
<td>86,184</td>
<td>146,124</td>
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<td>Math Blocks (18x18)</td>
<td>11</td>
<td>22</td>
<td>34</td>
<td>72</td>
<td>72</td>
<td>84</td>
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<td>PLLs and CCCs</td>
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<td>6</td>
<td>8</td>
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<td></td>
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<td></td>
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<td>SPI/HPDMA/PDMA</td>
<td>1 each</td>
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<td>Fabric Interface Controllers (FICs)</td>
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<td>2</td>
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<tr>
<td>Data Security</td>
<td>AES256, SHA256, RNG</td>
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<tr>
<td>Memory</td>
<td>AES256, SHA256, RNG, ECC, PUF</td>
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<td>eNVM (K Bytes)</td>
<td>128</td>
<td>256</td>
<td>512</td>
<td></td>
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<td>LSRAM 18K Blocks</td>
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<td>21</td>
<td>31</td>
<td>69</td>
<td>69</td>
<td>109</td>
<td>236</td>
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<td>uSRAM1K Blocks</td>
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<td>34</td>
<td>72</td>
<td>72</td>
<td>112</td>
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<td>eSRAM (K Bytes)</td>
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<td>Total RAM (K bits)</td>
<td>703</td>
<td>912</td>
<td>1104</td>
<td>1826</td>
<td>1826</td>
<td>2586</td>
<td>5000</td>
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<td>High Speed</td>
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<td></td>
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<tr>
<td>DDR Controllers</td>
<td>1x18</td>
<td>2x36</td>
<td>1x18</td>
<td>1x18</td>
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<td>SERDES Lanes (T)</td>
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<td>PCIe End Points</td>
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<td>2</td>
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<tr>
<td>User I/Os</td>
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<tr>
<td>MSIO (3.3V)</td>
<td>115</td>
<td>123</td>
<td>157</td>
<td>139</td>
<td>271</td>
<td>309</td>
<td>292</td>
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<tr>
<td>MSIOD (2.5V)</td>
<td>28</td>
<td>40</td>
<td>40</td>
<td>62</td>
<td>40</td>
<td>40</td>
<td>106</td>
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<tr>
<td>DDRIO (2.5V)</td>
<td>66</td>
<td>70</td>
<td>70</td>
<td>176</td>
<td>76</td>
<td>76</td>
<td>176</td>
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<tr>
<td>Total User I/O</td>
<td>209</td>
<td>233</td>
<td>267</td>
<td>377</td>
<td>387</td>
<td>425</td>
<td>574</td>
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</tbody>
</table>

1. Total logic may vary based on utilization of DSP and memories in your design.
2. Please see the IGLOO2 and SmartFusion2 Fabric User Guides for details.
3. Feature availability is package dependent.
# IGLOO2 Packaging Options

<table>
<thead>
<tr>
<th>Type</th>
<th>FCSG325</th>
<th>VFG256</th>
<th>FCSG536</th>
<th>VFG400</th>
<th>FCVG484</th>
<th>TQG144</th>
<th>FGG484</th>
<th>FGG676</th>
<th>FGG896</th>
<th>FCG1152</th>
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<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
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<td>Length x Width (mm)</td>
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<td>17x17</td>
<td>19x19</td>
<td>20x20</td>
<td>23x23</td>
<td>27x27</td>
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<td>35x35</td>
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<td>M2GL005 (S)</td>
<td>161     -</td>
<td>171     -</td>
<td>84      -</td>
<td>209     -</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M2GL010 (T/TS)</td>
<td>138    2</td>
<td>195     4</td>
<td>84      -</td>
<td>233     4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>M2GL025 (T/TS)</td>
<td>180    2</td>
<td>138     2</td>
<td>207     4</td>
<td>267     4</td>
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<td></td>
<td></td>
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<tr>
<td>M2GL050 (T/TS)</td>
<td>200    2</td>
<td>207     4</td>
<td>267     4</td>
<td>267     4</td>
<td>377     8</td>
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<td></td>
<td></td>
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</tr>
<tr>
<td>M2GL060 (T/TS)</td>
<td>200    2</td>
<td>207     4</td>
<td>267     4</td>
<td>387     4</td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>M2GL090 (T/TS)</td>
<td>180    4</td>
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<td></td>
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<tr>
<td>M2GL150 (T/TS)</td>
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<td>293     4</td>
<td>248     4</td>
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</tbody>
</table>

- **Military Devices also available**
  - FG484 Package for 010, 025, 050, 060, 090 devices
  - FC1152 Package for 150 device

- **Automotive Devices available**
Design Ecosystem Components

FPGA Design Flow

- Libero System-on-Chip
  - Design Entry
    - IP Catalog
    - System Builder
    - SmartDesign
  - ModelSim Simulation
  - Synplify Pro Synthesis
  - Timing & Power Driven Layout
  - Timing Analysis
  - Power Analysis
  - SmartDebug

Embedded Design Flow

- SoftConsole
  - Firmware Catalog
  - Sample Projects
  - Compiler
  - Debugger
  - Software Program and Debug
  - Programmer

Graphical Configurators & Applications

- Demo/Eval Boards
  - Hardware Programming File

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Libero SoC Design Suite

- **Comprehensive Tool Suite**
  - System Builder and SmartDesign design entry
  - Synplify Pro® synthesis
  - ModelSim® simulation
  - Power-driven place-and-route
  - SmartPower power analysis
  - SmartTime timing analysis
  - SmartDebug in-circuit FPGA debug

- **Ease of Design Focus**
  - Push button flow
    - Proceed from synthesis to programming in one click
  - GUI wizards guide design process
  - Rich IP library & user block support facilitates design reuse
  - Faster learning curve
FPGA/ SoC FPGA Design Flow

Description of the basic building blocks are provided to the software development toolset
- **SmartDesign, HDL Flow, System Builder, Model Compiler**

Verification of design functionality and perform timing waveforms
- **ModelSim ME**

Transformation of desired functionality to an optimized netlist
- **Synplify Pro ME**

Placement of all the logic elements and routing the placed components
- **ChipPlanner**

Application of timing constraints and power analysis of the design
- **SmartTime, SmartPower**

Download of the STAPL or bitstream file on to FPGAs
- **FlashPro, FlashPro Express**

Verification of design at silicon level
- **SmartDebug, Identify ME**

Tools Supported
- **Tools Supported**
Libero System Builder Wizard

- Correct by construction system design for SmartFusion2
  - Walks the user through
    - basic questions on the system architecture
    - configuration options for each selected feature
  - Adds required peripherals in the fabric
  - Builds complete base system and API

Accelerates architecture design so engineers can focus on their value add.
## Embedded Design Options

<table>
<thead>
<tr>
<th>Software IDE</th>
<th>SoftConsole</th>
<th>Keil MDK</th>
<th>IAR Embedded Workbench®</th>
</tr>
</thead>
<tbody>
<tr>
<td>Free Versions from Microsemi</td>
<td>Free with Libero SoC</td>
<td>32 K Code Limited</td>
<td>32 K Code Limited</td>
</tr>
<tr>
<td>Available from Vendor</td>
<td>N/A</td>
<td>Full version</td>
<td>Full Version</td>
</tr>
<tr>
<td>Compiler</td>
<td>GNU GCC</td>
<td>RealView® C/C++</td>
<td>IAR ARM Compiler</td>
</tr>
<tr>
<td>Debugger</td>
<td>GDB Debug</td>
<td>μVision Debugger</td>
<td>C-SPY® Debugger</td>
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<tr>
<td>Instruction Set Simulator</td>
<td>No</td>
<td>μVision Simulator</td>
<td>Yes</td>
</tr>
<tr>
<td>Debug Hardware</td>
<td>FlashPro4/5</td>
<td>ULINK®2 or ULINK-ME</td>
<td>J-LINK™ or J-LINK Lite</td>
</tr>
<tr>
<td>Trace Capability</td>
<td>No</td>
<td>ULINKpro</td>
<td>JTAGjet-Trace</td>
</tr>
</tbody>
</table>

- **SmartFusion2 development/evaluation kits include:**
  - Free Libero SoC Gold license
  - Free SoftConsole support
  - Optional Embedded Linux design environment
SmartFusion2 Software Stack

Application Layer
- Customer Secret Sauce

Middleware
- TCP/IP, HTTP, SMTP, DHCP, LCD

OS/RTOS
- μC/OS-III, uCLinux, RTX, FreeRTOS

Drivers
- I²C Driver
- SPI Driver
- UART Driver
- CAN Driver
- USB Driver
- Ethernet Driver
- Timer Driver
- eNVM Driver

Hardware Abstraction Layer
- Microsemi CMSIS-based HAL

Hardware Platform
- Microsemi SmartFusion2

SmartFusion stack accelerates application development
Ecosystem of Industry Leaders

Trusted Ecosystem Partners accelerate design in time with IP and Ease of Use
## SmartFusion2 Starter Kit

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Device</th>
<th>Price</th>
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</thead>
<tbody>
<tr>
<td>SF2-STARTER-KIT</td>
<td>M2S050-FFG484</td>
<td>List - $299</td>
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<tr>
<td>SF2-484-STARTER-KIT</td>
<td>M2S010-FFG484</td>
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</table>

### Board Features

- System-On-Module (SOM)
- 10/100 Ethernet
- USB 2.0 OTG interface
- 64MB LPDDR, 16MB SPI flash
- USB based Wi-Fi module
- Breadboard expansion
SmartFusion2 Security Evaluation Kit

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Device</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>M2S090TS-EVAL-KIT</td>
<td>M2S090TS-1FGG484</td>
<td>List - $399</td>
</tr>
</tbody>
</table>

**Board**

- 512Mb LPDDR, 64Mb SPI flash
- x1 PCIe Edge connector
- Four SMA connector
- 10/100/1000 Ethernet
- GPIO expansion
- 1-year Free Libero SoC Platinum license

**Features**

- Evaluate security features
- Develop and test PCI Express Gen2 x1
- Evaluate SerDes transceiver using SMA Pairs
- Power measurement of the SmartFusion2 SoC FPGA
- Create a working PCIe link quickly with the PCIe Control Plane Demo

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## SmartFusion2 Advanced Development Kit

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Device</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>M2S150-ADV-DEV-KIT</td>
<td>M2S150TS-1FCG1152</td>
<td>List - $999</td>
</tr>
</tbody>
</table>

### Board

![SmartFusion2 Board Diagram]

- **FT4232 Header**
- **FMC Connector HPC**
- **SERDES3 TX/RX SMA Pairs**
- **SERDES3 Reference Clock**
- **Bread Board Space**
- **DIP Switch**
- **I2C Header**
- **On-Off Switch**
- **12V Power Supply Input**
- **Debug Switch**
- **JTAG Programming Header**
- **FMC Connector LPC**
- **ETM Trace Debug Header**
- **Marvell PHY**
- **x4 PCIe Edge Connector**
- **DDR3 Memory**
- **SmartFusion2**
- **SPI Flash**
- **Debug LEDs**
- **Debug Switch**
- **RVI/IAR Header**
- **Power Measurement**

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SmartFusion2 Advanced Development Kit

Board

- FMC Connector-LPC (J60)
- FMC Connector-HPC (J30)
- Breadboard Connector
- DDR3 SDRAMs 4 x 256MB
- DDR3 SDRAMs 256MB (SECDED)
- Debug LEDs
- Debug Switches

Features

- Dual Gigabit Ethernet, USB 2.0, SPI, I2Cs, UARTs
- 2 Giga Bits (Gb) SPI flash - 1Gb connected to MSS and other 1Gb connected to FPGA fabric
- Two FMC connector with HPC/LPC pinout for expansion
- x4 PCIe edge connector
- One pair SMA connector
- Core current measurement test points
- Comes with 1 year of Libero Platinum License ($2500 value)

Applications

- Embedded ARM® Cortex™-M3 processor based systems
- PCIe endpoint
- Motor control
- Industrial automation
- Power measurement
- Security
- FMC expansion
- High speed I/O
- Universal serial bus (USB) applications (OTG support)
IGLOO2 Evaluation Kit

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Device</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>M2GL-EVAL-KIT</td>
<td>M2GL010T-1FGG484</td>
<td>List - $399</td>
</tr>
</tbody>
</table>

**Board Features**
- 512Mb LPDDR, 64Mb SPI flash
- x1 PCIe Edge connector
- Four SMA connector
- 10/100/1000 Ethernet
- GPIO expansion

**Applications**
- Develop and test PCI Express Gen2 x1
- Evaluate SerDes transceiver using SMA Pairs
- Power measurement of the IGLOO2 SoC FPGA
- Create a working PCIe link quickly with the PCIe Control Plane Demo
SmartDebug Advanced Debugging
Traditional Debug Methods & Challenges

- **In-Circuit FPGA Debug - External Test Equipment**
  - Insert custom debug code design
  - Implement triggering internally
  - User interface is familiar and frequently used
  - Leverages programmability of FPGA

- **In-Circuit FPGA Debug - Embedded Logic Analyzer**
  - Most FPGA vendors offer Integrated Logic Analyzer cores
  - Logic analyzer functionality is inserted into design
    - Has triggering and trace storage resources
    - Uses FPGA logic and memory resources
    - Core accessed through JTAG
    - Data displayed via PC viewing software
Potential Problems in FPGA

- **Software**
  - Functional definition errors
    - At the FPGA or system level
  - Functional system interaction problems
  - System-level timing issues
    - Asynchronous events
    - Real-world interactions, at speed

- **Hardware (Board Level) Issues**
  - Signal fidelity between ICs
  - Noise, crosstalk, reflections, loading, EMI
  - Power supply issues

- **Increased Complexity**
  - Increased device size and complexity
  - Time-to-market, debug time can account for over 50% of design time
Logic Simulation

- **Potential Problems:**
  - Catching the obvious errors but it won’t catch 100% of the problems
    - Hard to simulate asynchronous system events
    - Hard to simulate real-world interactions, at-speed
    - Difficult to simulate timing violations
  - 100% Code Coverage is difficult to achieve
  - Simulation runs are relatively slow
Microsemi Debug Capabilities

- **SmartDebug**
  - Industry best debug tool suite
  - Accelerates effectiveness of an Integrated Logic Analyzer (ILA)
  - Minimal FPGA resource utilization for debug
  - Saves design cycle time as it does not require recompile or re-program the FPGA to debug the internal signals
  - SmartDebug has observability and controllability features
  - Flexibility to change probe points on the fly

- **Synopsys Identify ME**
  - Debug the FPGA design area using Integrated Logic Analyzer
  - Trigger breakpoints for allowing specific event-driven sampling of the signals within the design
  - Overlay capture information over HDL
  - Monitor dynamic signals with a recompile option
  - Debug internal signals and external IOs
1. Debugging starts here with a large set of design area to explore. Broad scope is required to find stuck at faults, clock gates/locks, incorrect FSM states, etc.

2. The debug process narrows down the logic design until a focus area can be found.

3. Once a narrow focus is found the deep debug begins to determine the root cause of failure. Waveforms, HDL overlay of debug data, etc.

SmartDebug

Identify ME

Debug Time
Unique FPGA Silicon Debug Architecture

SmartFusion2, IGLOO2, and RTG4 architecture

Array of Logic Elements
Logic Element Access

- Every FF in every Logic Element can be monitored in real time using connectivity built into the FPGA fabric.

- FF state information can be read out via JTAG using SmartDebug ActiveProbe.

- FF activity can be broadcast to two defined PROBE pins on the package for real time monitor using LiveProbe.
SmartDebug

- Integrated into Libero SoC since 2013

- Includes several different tools:
  - ActiveProbe
  - LiveProbe
  - Memory Debug
  - Flash Memory
  - ProbeInsertion
  - SERDES

- All available with the FlashPro programming cable.

- No additional FPGA resources
SmartDebug Offering

- SmartDebug Integrated in Libero SoC
  - Launch directly from Libero after programming the design
  - Good for desktop debugging by the FPGA designer

- Stand Alone SmartDebug
  - Installed separately from Libero (no license required)
  - Allows the FPGA designer to provide design details to the lab for debug
  - Isolation between design and lab for sensitive environments
LiveProbe

- Two FPGA IO pins that can be used as probes (PRA and PRB)
  - Any FF outputs can be “routed” to these probe pins

- No need to recompile or re-program the FPGA to change the source of the probes
ActiveProbe

- Dynamic asynchronous read and write to FF
  - Static observation of signal state
- No need to recompile or re-program the FPGA to find and add new FFs
Memory Debug LSRAM/uRAM

1. Select Memory to Read
2. Modify Value
3. Write Memory
Flash Memory

- Flash Memory is used to capture the eNVM content from the FPGA device
- Flexible to access specific memory pages
- Shows the Page number and address of the read memory
Probe Insertion

- Route any internal signals to available FPGA outputs
  - Runs an incremental Place and Route from the selected signal to the IO
  - Not available in Stand Alone SmartDebug (no P&R engine)
SERDES

- Real-time access to SERDESIF Block control and status registers
- Provide testing functions with pseudo-random binary sequence (PRBS) or constant pattern generators and checkers
- Run link tests with various loop back options
SmartDebug Summary

- SmartDebug is a collection of tools
  - ActiveProbe
  - LiveProbe
  - Memory Debug
  - Flash Memory
  - ProbeInsertion
  - SERDES Debug

- SmartDebug requires no additional FPGA resources

- Easily switch between probe points without re-compile

- Limitation is depth of the signal
LiberoSoC Enhanced Constraints Flow
Libero SoC Project Settings: Device Selection

- Change FPGA die, Package, Speed Grade or Operating conditions
  - Family cannot be changed
Libero SoC Design Flow Window

- Single Window Provides Access to tools and shows Design Status
- Tools Can be Run in Background or Launched from Design Flow Window or Menus
- Project Flow Window Displays:
  - Tools
  - Design Creation
    - Includes option to import files into the project
  - Stimulus Creation
  - Processing
    - Simulation
    - Synthesis
    - Place and Route
  - Transitions
  - Current State
  - Tool Tips
Enhanced Constraint Flow

- New Constraint Management Window centralizes all constraints activities (files management, constraint generation, checkers, graphical editors, …)
- Supports the **SAME** timing constraints file for all design phases – Synthesis, Place and Route, and Timing Verification.
Libero v11.7 Constraint Management

- Constraints can be edited as text files or in a graphical editor (I/O editor, Chip Planner, SmartTime Constraint Editor)
- All constraints entered via GUI are now saved in the target text file.
- Constraints are no longer saved in the design database
  - NO MORE MERGE!!!
Constraint Manager tabs

- I/O Attributes – This tab is used for all I/O constraints
- Timing – This tab is used for all timing constraints for the design
- Floor Planner – This tab is used for region constraints from either the Chip Planner or manually
- Netlist – This tab is used for non-timing related synthesis attributes and layout constraints
Timing Requirements / Exceptions

- Timing Requirements Are:
  - Clock Frequency
  - Input Delay
  - Output Delay

- Timing Exceptions Are:
  - Multi-cycle Paths
  - False Paths
  - Maximum Delay
  - Minimum Delay

- Timing Requirements And Exceptions:
  - Direct Synthesis Mapping
  - Guide Place and Route and Timing Analysis of a Design
Libero 11.7 Constraint Manager: Timing Constraints

- Same constraints can be used in synthesis, place and route and timing analysis
  - Synplify Pro preserves the names of objects (nets, registers) with constraints
- Timing constraints saved as SDC files
- All tools available before synthesis
  - Graphical constraint editor
  - Constraint checker
  - Constraint generations
- Derive constraints generates constraints based on IP configuration
Constraint Manager: Timing Constraints

- Create Timing constraint file for synthesis, layout and verification
  - Import or Link to existing file or use constraint Editor; Check timing constraints
  - Supports multiple SDC files and Automatic constraint file generation

- Import or link to existing timing constraint files
- Edit with constraint editor
- Create new timing constraint file
- Constraint Manager: Timing Constraints
  - Analyzes the HDL of the design and identifies clocks in the design that are sourced from known components in the design
Timing Constraints: Creating a Timing Constraint File

- Create SDC file with editor

Enter name for SDC file

Text editor opens

```
#clocks
create_clock -period 10.00 -waveform {0.000 5.000} -name {CLK} -add {get_ports {CLK}}
```
Timing Constraints
Importing a Timing Constraint File

- Import existing timing constraint files
Constraint Manager: Derive Constraints

- Derive constraints use the RTL and IP configurations to generate constraints for all known clocks and additional IP timing.
- Constraints are written to a SDC file compatible with synthesis, place and route and timing analysis.
- Clock/Generated Clock constraints for oscillators, CCC outputs and references, SERDES.
- Timing exceptions for CoreConfigP and CoreResetP.
- Timing exceptions must be given to synthesis to be compatible with post-synthesis netlist.
Constraint Manager: Derived Constraints

```plaintext
#Spacewire appanote design constrain file
create_clock -name {PAP} -period 10 -waveform {0 5} [ PAP ]

#Generated Clock Constraints
# Generated Clock Constraints for the GCC block inside the spacewire_gen block
create_generated_clock -name [SPwire_data_strobe_gen_top_0/SPwire_Data_Strobe_Gen_0/RTC4FCCC_0/GCC_INST/GL0] -divide_by 1 -source [ get_pins { SPwire_data_strobe_gen_top_0/SPwire_Data_Strobe_Gen_0/RTC4FCCC_0/GCC_INST/GL0 } ]

# False Path constrain
set_false_path -from [ get_pins { SPwire_data_strobe_gen_top_0/SPwire_Data_Strobe_Gen_0/RTC4FCCC_0/GCC_INST/GL0 } ] -to [ get_pins { SPwire_data_strobe_gen_top_0/SPwire_Data_Strobe_Gen_0/RTC4FCCC_0/GCC_INST/GL0 } ]
set_false_path -from [ get_pins { SPwire_data_strobe_gen_top_0/SPwire_Data_Strobe_Gen_0/RTC4FCCC_0/GCC_INST/GL0 } ] -to [ get_pins { SPwire_data_strobe_gen_top_0/SPwire_Data_Strobe_Gen_0/RTC4FCCC_0/GCC_INST/GL0 } ]
```
SDC Timing Constraints
More Information

- SDC constraint syntax is available in the Libero Help
Constraint Manager: Constraint Editor

- Create Timing constraints using SmartTime Constraint Editor
Synthesis
Synthesis Options

- Select HDL language
- Manage globals
- Enable retiming
- Specify SRAM optimization options
Synplify Pro ME

- Synplify Pro ME is Equivalent to Synopsys Synplify Pro Product
  - Included in all Libero SoC Editions
  - Limited to Microsemi FPGA products Only
Synplify Pro Features

- Mixed Language design Entry
- HDL Analyst®
- Graphical State Machine Viewer
- FSM Explorer
- Pipelining of Multipliers and ROMs
- Re-timing
- Compile Point Creation
- Generic Cross-Probing of Critical Paths
- Multiple Implementations & Workspace Support
Synplify Pro Interface
Synplify Pro Directives and Attributes
Synplify Pro Directives and Attributes

- Direct analysis, optimization, and mapping of the design during synthesis

- Directives control compiler optimizations
  - Directives must be entered in HDL source code

- Attributes control mapping optimizations
  - Attributes can be entered in the constraint editor or HDL source code
    - Synplify Pro Attributes can be entered in Attribute Pane of the SCOPE Editor or in the VHDL or Verilog Code
## Attribute and Directive Summary

<table>
<thead>
<tr>
<th>NAME</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>syn_black_box</td>
<td>D</td>
<td>Specifies that a module or component is a black box with only its interface defined for synthesis. The contents of a black box cannot be optimized during synthesis.</td>
</tr>
<tr>
<td>syn_noprune</td>
<td>D</td>
<td>Prevents optimizations for instances and black-box modules with unused output ports</td>
</tr>
<tr>
<td>syn_preserve</td>
<td>D</td>
<td>Prevents sequential optimization such as constant propagation, inverter push-through, and FSM extraction</td>
</tr>
<tr>
<td>syn_sharing</td>
<td>D</td>
<td>Enables / disables the resource sharing operators inside a module during synthesis</td>
</tr>
<tr>
<td>syn_keep</td>
<td>D</td>
<td>Prevents an internal signal from being removed during synthesis and optimization</td>
</tr>
<tr>
<td>alspreserve</td>
<td>A</td>
<td>Prevents a net from being removed during Place and Route</td>
</tr>
<tr>
<td>syn_encoding</td>
<td>A</td>
<td>Specifies encoding style for state machines</td>
</tr>
<tr>
<td>syn_insert_buffer</td>
<td>A</td>
<td>Directs Synplify Pro to use specific I/O pads</td>
</tr>
<tr>
<td>syn_maxfan</td>
<td>A</td>
<td>Overrides the default (global) fanout guide for an individual input port, net, or register output</td>
</tr>
<tr>
<td>syn_multstyle</td>
<td>A</td>
<td>Controls the inference of MATH blocks</td>
</tr>
<tr>
<td>syn_noclockbuf</td>
<td>A</td>
<td>Disables automatic insertion of clock buffers</td>
</tr>
<tr>
<td>syn_ram_style</td>
<td>A</td>
<td>Specifies the implementation to use for an inferred RAM</td>
</tr>
</tbody>
</table>
SERDES EPCS Mode design tips
SERDES / Hard IP architecture

PMA - Multi-Protocol 5G transceiver
Organized in blocks of x4
4 blocks max for 16 lanes
High Speed Serial Interface Configurator
EPCS and XAUI (NPSS Block)
# NPSS Configurator: Identification and Protocol

Select SERDES Block

## Protocol Configuration

### Protocol 1
- **Type**: EPCS
- **Number of Lanes**: x1

### Protocol 2
- **Type**: None
- **Number of Lanes**: None

### Protocol 1: XAUI or EPCS
- **Lane Width**: X4
  - **Lane Assignment**: Lane 0, Lane 1, Lane 2, Lane 3
  - **Speed Choices**: 3.125 Gbps

### Protocol 2: EPCS (available if Protocol 1 is not XAUI)

<table>
<thead>
<tr>
<th>Protocol</th>
<th>Protocol #</th>
<th>Lane Width</th>
<th>Lane Assignment</th>
<th>Description</th>
<th>Speed Choices</th>
</tr>
</thead>
<tbody>
<tr>
<td>EPCS</td>
<td>Protocol 2</td>
<td>x1</td>
<td>Users can select Lane 0, 1, 2, or 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Protocol 2</td>
<td>x2</td>
<td>Lane 0, Lane 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Protocol 2</td>
<td>x4</td>
<td>Lane 0, Lane 1, Lane 2, Lane 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Protocol 2</td>
<td>x1</td>
<td>Users can select Lane 2 or 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Protocol 2</td>
<td>x2</td>
<td>Lane 2, Lane 3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NPSS Configurator: Lane Configuration

Configure up to four SERDES block lanes

<table>
<thead>
<tr>
<th>Lane 0</th>
<th>Lane 1</th>
<th>Lane 2</th>
<th>Lane 3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Speed</strong></td>
<td>Custom Speed</td>
<td>Custom Speed</td>
<td>Custom Speed</td>
</tr>
<tr>
<td><strong>Reference Clock Source</strong></td>
<td>REFCLK (Differential)</td>
<td>Custom Speed</td>
<td>Fabric</td>
</tr>
<tr>
<td><strong>PHY RefClk Frequency (MHz)</strong></td>
<td>125</td>
<td>125</td>
<td>125</td>
</tr>
<tr>
<td><strong>Data Rate (Mbps)</strong></td>
<td>2500 Mbps (20 bit)</td>
<td>2500 Mbps (20 bit)</td>
<td>2500 Mbps (20 bit)</td>
</tr>
<tr>
<td><strong>Data Width</strong></td>
<td>20</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td><strong>FPGA Interface Frequency (MHz)</strong></td>
<td>125</td>
<td>125</td>
<td>125</td>
</tr>
<tr>
<td><strong>VCO Rate (MHz)</strong></td>
<td>2500</td>
<td>2500</td>
<td>2500</td>
</tr>
</tbody>
</table>

- **Speed choices:** 3.125 Gbps for XAUI, Custom Speed for EPCS
- **PHY RefClk Frequency:** XAUI: 156.25 MHz, EPCS: 100 MHz to 250 MHz
- **Data Rate (Mbps):** XAUI: Fixed-value, EPCS: select the data rate from the drop-down menu
- **Data Rates are computed based on the PHY RefClk Frequency**
- **Reference clock source options:** Differential or single-ended
- **Options for Protocol 1 and Protocol 2:**
  - REFCLK (Differential)
  - REFCLK0 (Voltage_Referenced)
  - REFCLK1 (Voltage_Referenced)
  - REFCLK0 (Single_Ended)
  - REFCLK1 (Single_Ended)
  - Fabric (Available only for EPCS Protocol)
SERDES EPCS and XAUI

- EPCS and XAUI SERDES modes requires proper floor-planning, via placement constrains, to achieve timing closure at higher speed (> 3.125Gbps)
The RX_CLK incurs significant delay going from the SERDESIF to the CLKINT/RCLKINT driver to the fabric FF to capture the data.

- Hold time violations exist with this large clock delay
- This delay must be matched with the receive data for a clean interface
- CLKINT delay is much larger than RCLKINT delay
The TX_CLK incurs significant delay just like the RX_CLK

- There is a large round trip time from the SERDESIF TX_CLK to the CLKINT/RCLKINT to the last FF clock-to-out back into the SERDESIF.
The EPCS Timing Solution

For small devices (010/025) CLKINT can be used. For larger devices (050/060/090/150) RCLKINT should be used.

Rx solution good up to 5Gbps (250MHz)
Tx solution good up to 3.2Gbps (160MHz).

2 FFs to allow placement flexibility to keep last FF close to SERDESIF.

First stage FF uses negative edge to reduce clock injection time. Also add static data delay to match clock delay.
EPCS Demo Example

- Two modules are provided with the demo.
  - EPCS_TX_INTF – 2 FFs
  - EPCS_RX_INTF – 2 FFs + Delay

- These are 20-bit data wide modules that should be used with any EPCS design.
  - Verilog and VHDL HDL provided

- In the demo example design a CLKINT is inferred in the design.
EPCS Interface at 5Gbps

- Pushing the Tx interface beyond 3.2Gbps requires more work.
  - To go beyond 3.2Gbps you need to use a local clock to the first FF

- Not all lanes work up to 5.0Gbps on the transmit side due to differences in the alignment with the fabric and the SERDESIF lane.
  - All are able to meet 4.8Gbps
- Special synthesis attributes are required to use the local clock path.
RTG4™ High-Speed RT FPGAs
Introducing RTG4 High-Speed RT FPGAs

RTG4 mitigates risks of ASICs and SRAM FPGAs, and has 20X improvement in signal processing throughput

- High-Speed Signal Processing
  - 300 MHz
  - 150 KLE
  - 5 Mbit SRAM
  - 462 Multipliers
  - 24 x 3.125 Gb/sec SERDES
  - TID > 100 Krad
  - SEL immune
Why RTG4 is Compelling

- More flexible than an RH ASIC
  - Reprogrammable, no NRE, no cost and schedule risk
- More signal-processing features than any other RT FPGA
  - More registers, combinatorial logic, multiply blocks, and transceivers
  - Lower power, live at power-up, no external boot memory needed
- Radiation enhanced for Geosynchronous Earth Orbit and deep space
  - RTG4 65nm Flash has complete immunity to configuration upsets (SEU)
  - Total ionizing dose (TID) and single event effects (SEE) hardened by design

**RTG4 offers groundbreaking features for satellite applications**
• Total-dose hardening of Flash cells
• Single-event hardening of registers, SRAM, multipliers, PLLs

**Comprehensive radiation-mitigated architecture for signal processing applications**
# RTG4 Family Resources

<table>
<thead>
<tr>
<th>Resources</th>
<th>RT4G150</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Elements (TMR Register + 4-Input C Logic)</td>
<td>151,824</td>
</tr>
<tr>
<td>18x18 Multiply-Accumulate Blocks</td>
<td>462</td>
</tr>
<tr>
<td>RAM Mbits (1.5 Kbit and 24 Kbit Blocks, with ECC)</td>
<td>5.2</td>
</tr>
<tr>
<td>UPROM Kbits</td>
<td>374</td>
</tr>
<tr>
<td>DDR2/3 SDRAM Controller (with ECC)</td>
<td>2x32</td>
</tr>
<tr>
<td>PCI Express Endpoints</td>
<td>2</td>
</tr>
<tr>
<td>Globals</td>
<td>24</td>
</tr>
<tr>
<td>PLLs (Rad Tolerant)</td>
<td>8</td>
</tr>
<tr>
<td>SpaceWire Clock &amp; Data Recovery Circuits</td>
<td>16</td>
</tr>
<tr>
<td>User IO (excluding SERDES)</td>
<td>720</td>
</tr>
<tr>
<td>SERDES lanes (3.125 Gbit/sec)</td>
<td>24</td>
</tr>
</tbody>
</table>

### Hermetic, Ceramic Column-Grid Packages

- CG1657 (Six Sigma Columns)

- RT4G150 is available now Devices, PROTO & Development Kit
**RTG4 Radiation Mitigation**

- Radiation hardening by design
  - Total ionizing dose (TID) immune to > 125 kRAD
  - Single event latch-up and configuration upset immune
    - Tested to 103 MeV-cm²/mg (facility limit) at 100°C
  - Single event upsets in fabric < 1x10⁻¹¹ errors/bit/day
  - Single event transient mitigation in logic can be enabled/disabled globally or individually for higher performance
TID Mitigation in RTG4 Flash FPGAs

- RTG4 TID-tolerant interconnect
  - RTG4 FPGAs functional after TID > 125 Krad
  - Change in propagation delay ~ 0% after TID > 125 Krad
  - Pass transistor is indirectly coupled to floating gate devices
  - $V_T$ changes in Flash cells don’t change pass transistor prop. delay
RTG4 Logic Element Radiation Mitigation

- Dedicated register with efficient triple module redundant (TMR) hardening
- Single event transient (SET) filter mitigates radiation glitches from comb. logic
- Hierarchical routing architecture enables >95% module utilization
**RTG4 Mathblock**

- 18 x 18 multiplier with advanced accumulate
- High performance for signal processing throughput
- Optional SEU-protected registers on inputs and outputs (including C input)
RTG4 Memory Blocks

- **Radiation Tolerant**
  - Resistant to multi-bit upset
  - Built-in optional EDAC (SECDED)

- **LSRAM – up to 24 KBit**
  - Dual-port and two-port options
  - High performance synchronous operation
  - Example usage
    - Large FFT memory

- **uRAM – up to 1.5 KBit**
  - Three Port Memory
    - Synchronous Write Port
    - Two Asynchronous or Synchronous Read Ports
  - Example usage
    - Folded FIR filters and FFT twiddle factors
RTG4 General Purpose IO

- Single ended standards
  - LVCMOS from 1.2V to 3.3V
  - LVTTL
  - PCI

- Voltage reference standards (600+ Mbps)
  - Includes on-chip termination
  - SSTL2, SSTL18 and SSTL15
    - For DDR2/DDR3 SDRAM memories
  - HSTL18 and HSTL15
    - For SRAM memories

- Differential I/O standards
  - Includes on-chip termination
  - Mini-LVDS, M-LVDS, RSDS, LVPECL
RTG4 Radiation-Tolerant PLL

- Radiation-Tolerant PLLs are used in CCC, SERDES and DDR blocks

- Triple module redundant (TMR) PLL in internal feedback mode
  - Reference clock is fed back to all 3 sub-PLLs independently
  - Sub-PLL is SEL immune

- Single PLL in external feedback mode
  - PLL output travels through clock network and is fed back to PLL
  - Common mode used for clock network delay compensation
  - Only 1 sub-PLL is enabled in this mode
  - Sub-PLL is SEL immune

![PLL Diagram](image-url)
Hardened SpaceWire Clock Recovery

- SpaceWire interface used for command-and-control and data
  - Data and Strobe are XORed to recover SpaceWire clock
  - Hardwired and SET protected
  - Delay compensation available to align data and SpaceWire clock
  - 16 SpaceWire Clock Recovery circuits on each RTG4

Unique Microsemi RTG4 Feature
3.125 Gb/sec SERDES

PMA Based on PCIe Gen 1 PHY
Performance 1 to 3.125 Gb/sec
Up to 6 blocks with 4 lanes
SERDES EPCS and XAUI

- EPCS and XAUI modes are improved from commercial SERDES (For example: SmartFusion2 and Igloo2)
  - A flywheel FIFO improves read timing to the FPGA fabric and provides clock compensation to transfer Rx data to the Tx clock domain in the FPGA fabric
  - Dedicated routing from SERDES clocks to the global clock network

⇒ Efficient routing and high performance up to 3.125 Gb/sec
RTG4 Performance

- **FPGA logic**
  - 250 MHz system performance with SET mitigation
  - 300 MHz system performance without SET mitigation

- **DSP mathblock**
  - 250 MHz pipelined performance with SET mitigation
  - 300 MHz pipelined performance without SET mitigation

- **LSRAM24K and uRAM1.5K**
  - > 300 MHz

- **IO**
  - > 600 Mb/sec LVDS and 667 Mb/sec DDR2/3 SDRAM data
  - SERDES > 3.125 Gb/sec
RTG4 Packaging

- Hermetically sealed, ceramic packages
  - Embedded decoupling capacitors
    - Flight models will have Precious Metal Electrode (PME) capacitors
  - Column Grid Array, Ball Grid Array, Land Grid Array
RTG4 Design Ecosystem

- **Libero SoC Design Suite**
  - Synplify Pro® synthesis
  - ModelSim® simulation
  - Power-driven place-and-route
  - SmartPower power analysis
  - SmartTime timing analysis
  - SmartDebug in-circuit FPGA debug

- **Ease of Design Focus**
  - Push button flow - Proceed from synthesis to programming in one click
  - Reduced learning curve
  - Rich IP library & user block support facilitates design reuse
  - Working with IP partners to expand the RTG4 Ecosystem

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RTG4 Product Availability

- RTG4 devices for space flight applications
  - RT4G150-FC1657 FPGAs: NOW
  - Libero SoC Design Software: NOW
  - RT4G150 development kit: NOW
  - Daisy chain packages: NOW
  - MIL-STD-883 class B flight units: 3Q2016
  - QML class Q qualification: 4Q2016 or 1Q2017
  - QML class V qualification: 2Q2017
Microsemi FPGA Space Heritage

- **Microsemi Space heritage**
  - Broad space portfolio since 1957
  - First FPGAs screened for space in 1992
  - First FPGAs with radiation hardening by process in 1996
  - First FPGAs with radiation hardening by design in 2001

- RTSX-SU (Introduced 2004)
- RTAX-S/SL/DSP (Introduced 2005)
- RT ProASIC3 (Introduced 2008)

- Mars Reconnaissance Orbiter
  - RTSX-SU on board (2005)
- Curiosity (Mars Science Lab)
  - RTAX on board (2011)
- NASA IRIS
  - RT ProASIC3 on board (2013)
RTG4 High-Speed RT FPGAs

- High-bandwidth signal and data processing in radiation applications
- Flexible and reliable alternative to ASICs
- Immune to radiation-induced configuration upsets
- Radiation enhancements suitable for earth orbits and deep space

Solving Signal Processing Congestion in Space Systems

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SmartFusion2/Igloo2 Ordering Codes

- earlier revision of SmartFusion2/Igloo2 devices are not fully featured
  - Ordering Codes to have the right
    - SEL enhanced devices
    - Programming Modes
Q & A
Microsemi Corporation (MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 4,800 employees globally. Learn more at www.microsemi.com

Thank You