Radiation Hard High-Speed Optical Links for HEP

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Karlsruhe Institute of Technology (KIT)
Germany

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Outline

- **Optical links in HEP**
- **Phase II upgrade radiation constraints on links**
- **Developments for phase II**
  - **The LpGBT ASIC**
  - **The path from the GBTX into the LpGBT**
    - **Power / Radiation requirements**
- **Ways into the future!**

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Why Optical Links in HEP?

- Transmission distance?
  - Telecom: up to transcontinental distances! (long – haul)
  - HEP: at most a few hundreds of meters (short – haul)
- Bandwidth?
  - Telecom: the larger the better!
  - HEP:
    - The larger the better?
    - Does using THz bandwidths per fibre makes sense?
      - Needs data aggregation systems inside the detectors!
      - “Third generation” systems are complex, power hungry [and costly]
    - 5 to 10 Gb/s systems are being engineered for Phase II upgrades
- Especially important for HEP:
  - Small optical fibre cross section (material budget)
  - Immunity to interferences
  - Non EMI generator
  - No contribution to ground loops

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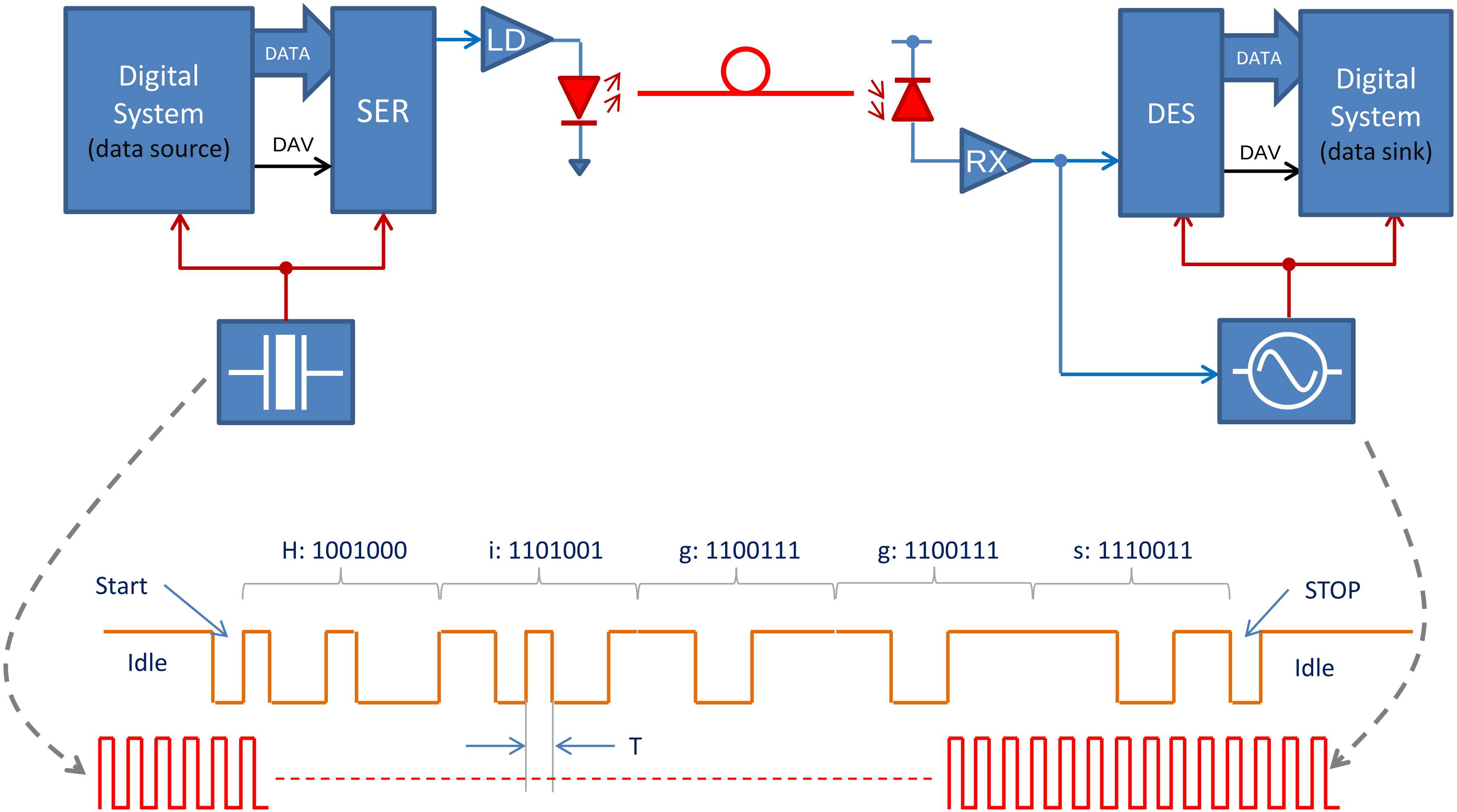
Optical Link Architecture



Frame, 37 bits:

- 35 data bits
- 2 control bits
- “Code efficiency” : 35/37 = 94%

Bit-Rate = 1/T

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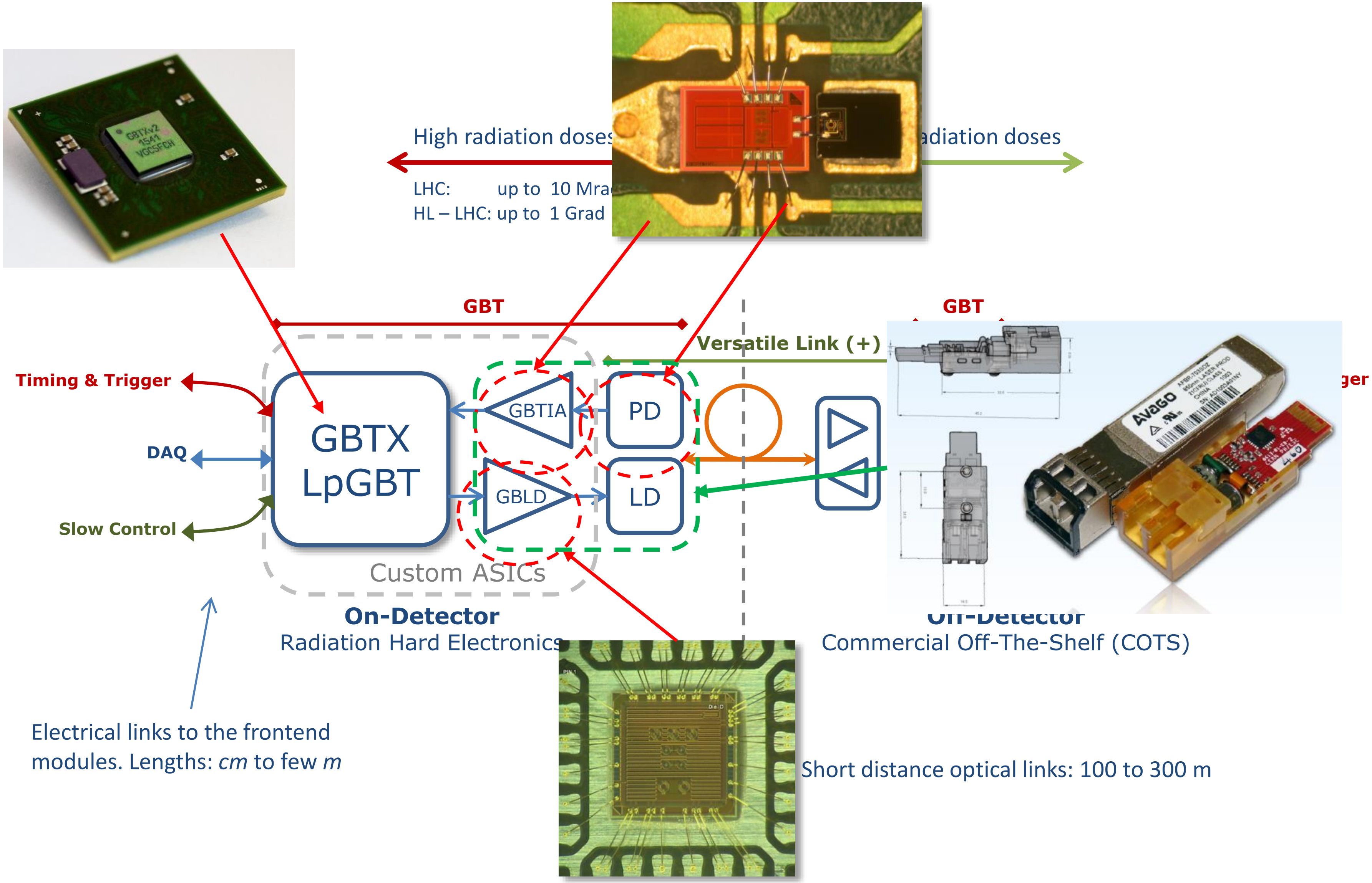
HEP Optical Link Architecture



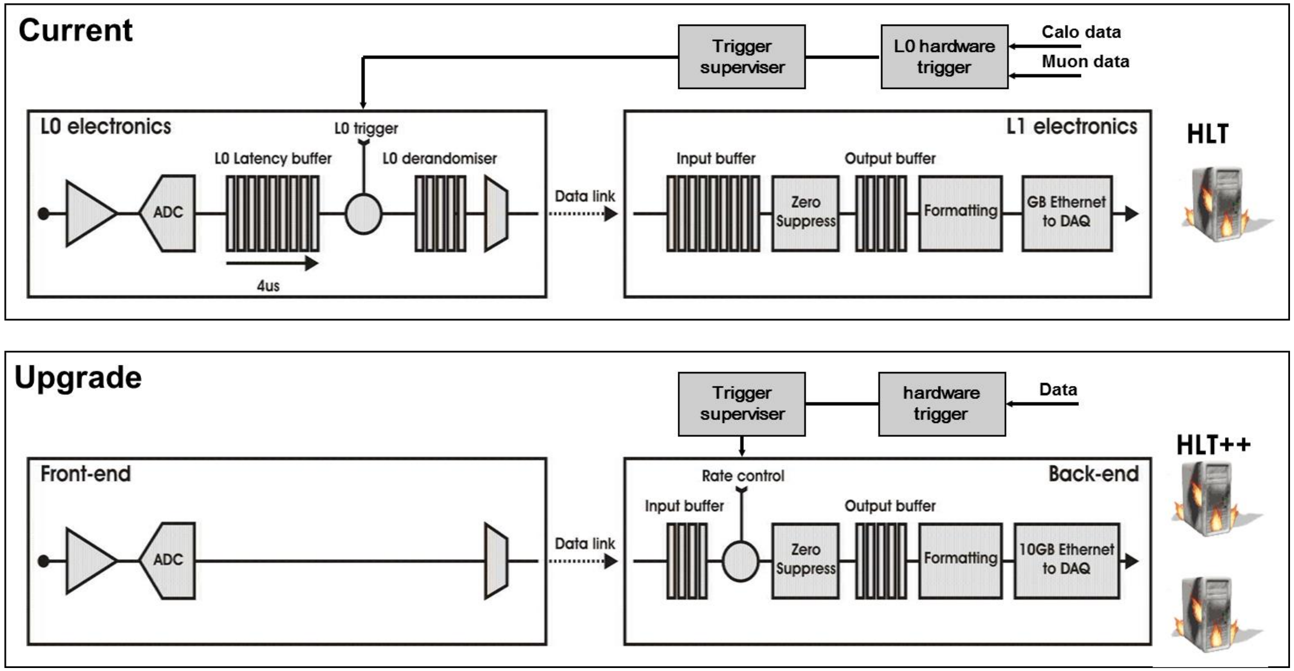
On-Detector
Radiation Hard Electronics

Off-Detector
Commercial Off-The-Shelf (COTS)

Electrical links to the frontend modules. Lengths: *cm* to few *m*

Short distance optical links: 100 to 300 m

LHCb Electronics Phase I Upgrade (2018)



- Full readout of the detector data!
  - Approximately 12k links in total
- Powerful trigger systems in the counting room profit from today’s computing power
- Architecture enablers:
  - Bandwidth of the optical links: 4.8 Gb/s
  - Versatile Link Modules: VTRx and VTTx
  - GBT chipset: GBTIA, GBLD and GBTX
  - Link components at affordable prices!

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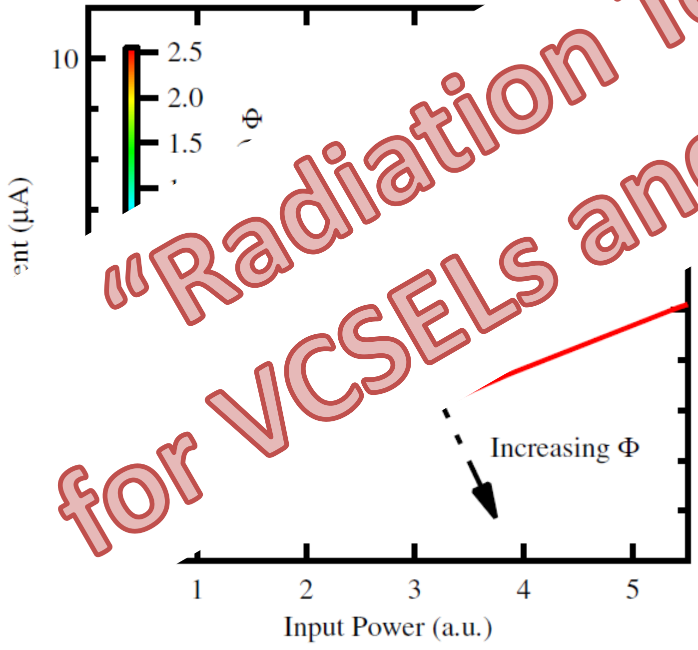
Radiation Damage in Optoelectronics

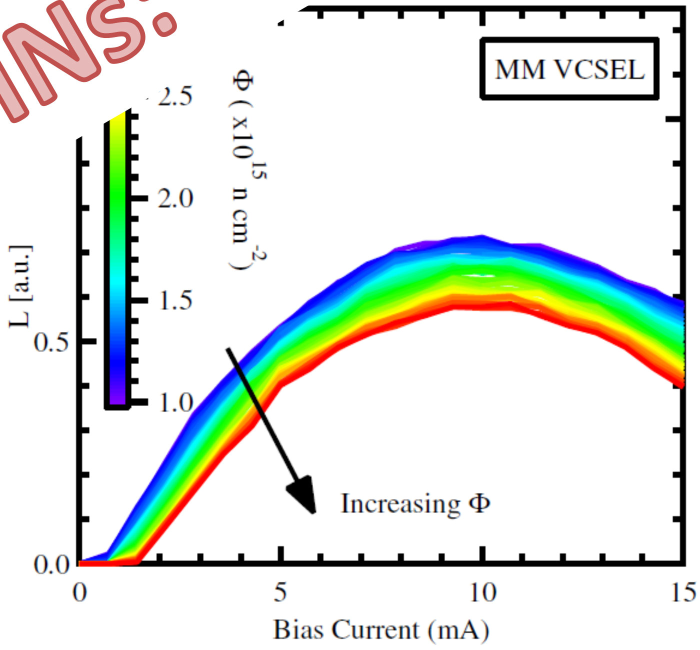
- Damage mechanism dominated by Displacement Damage (DD) caused by Non-Ionizing Energy Loss (NIEL) from heavy particles (neutral/c hadrons, energetic leptons).

- **PIN - Diodes:**
  - Increasing of the dark current by several orders of magnitude (from pA to mA)
  - Reduction of the responsivity (R = I_{ph}/P_{opt})
- **VCSEs:**
  - I

  er radiation
  EE diodes

“Radiation Tolerance Limit” for VCSELs and PINs: ~10^{15} n/cm2

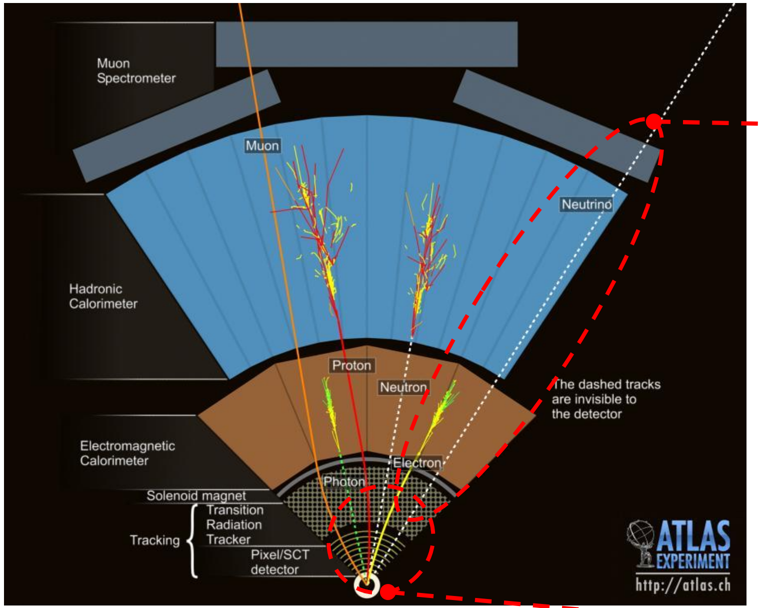




[At least] Two "Strategies" Necessary!

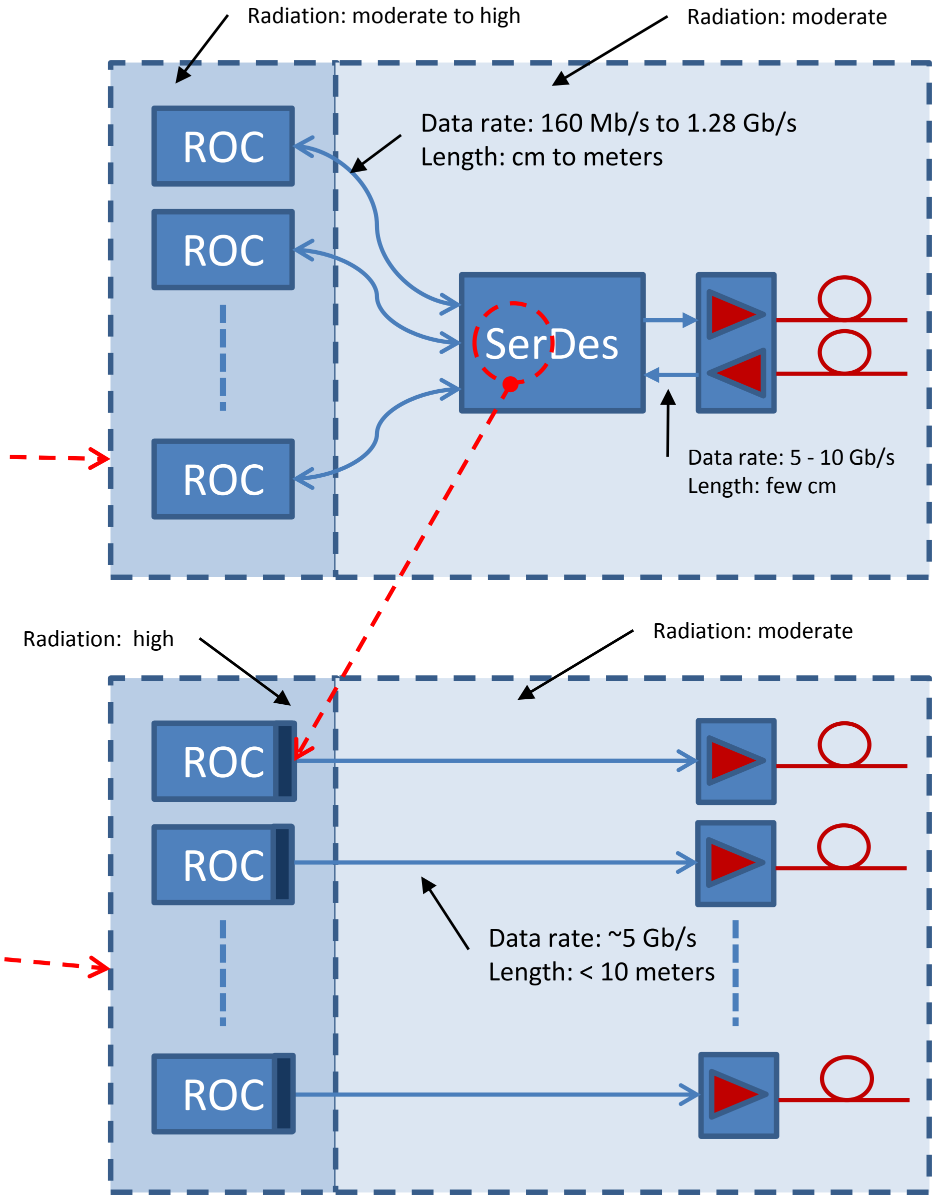
Outer detector systems
E.g. Tracker systems;

- Very high readout rates:
  - **5 – 10 Gb/s per Module**
- Moderately high radiation (10 years):
  - **100 Mrad**
  - **10^{15} n/cm^2**
- **ROC connects to the SerDes: 320 - 640 Mb/s**



Pixel systems (ATLAS)

- Very high readout rates:
  - **2 – 4 Gb/s per PROC in inner layer**
- Very high radiation (10 years):
  - **1 Grad**
  - **2 10^{16} n/cm^2**
- **PROC drives directly the VCSEL driver: ~5 Gb/s**



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The VL+ & LpGBT Projects

- Development of Radiation Hard Optical Links
  - For the Phase II Upgrades of the experiments (HL – LHC)
    - Installation during the Long Shutdown 3 (Centred around ~2024)
- Main objectives
  - Data rates:
    - 5.12 to 10.24 Gb/s for up links
    - 2.56 Gb/s for down links
  - Environment
    - Total Dose: 100 Mrad qualification (200 Mrad LpGBT chipset)
    - Total Fluence: $2x10^{15}$ n/cm2 and $1x10^{15}$ hadrons/cm^2
    - Temperature: -35 to + 60 °C
  - Reduce the power consumption of the data transmission systems
  - Reduce the footprint of the electronic and optoelectronic components
  - Optoelectronic components (VL+):
    - A low-profile package
    - Configurable:
      - Number of channels
      - Unidirectional / bidirectional

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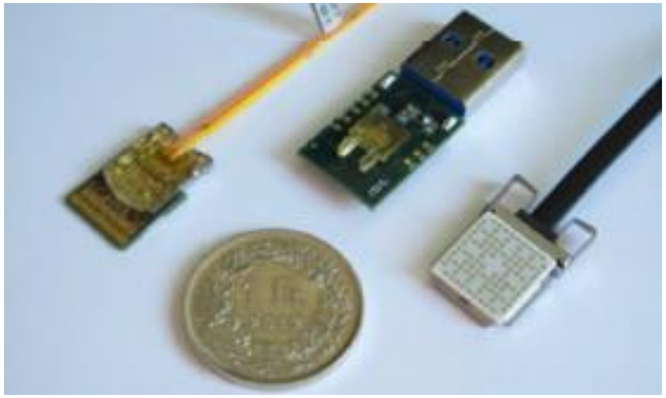
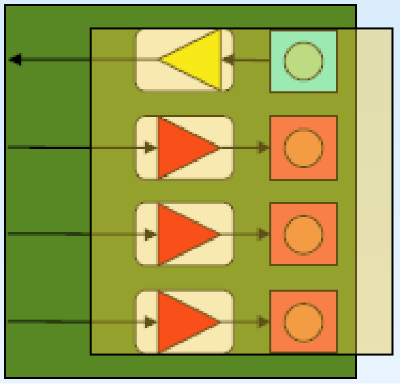
VL+ Module Concept

- Module
  - 4-channel, Rx/Tx count configurable at build time
- Multi Mode only
  - 850 nm VCSEL
  - InGaAs PIN (TBC)
- Miniaturized
  - Target dimensions:
    - **20 mm x 10 mm x 2 mm**
- Pluggable:
  - Optical and/or electrical connector



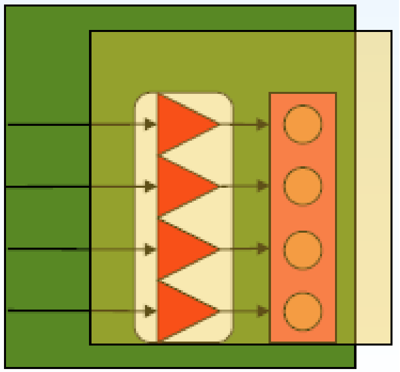
Based on single channel die

- E.g.: 3 TX (single channel LDD) + 1 RX



Based on multi-channel die

- E.g.: 4/8 TX (using LDD arrays)



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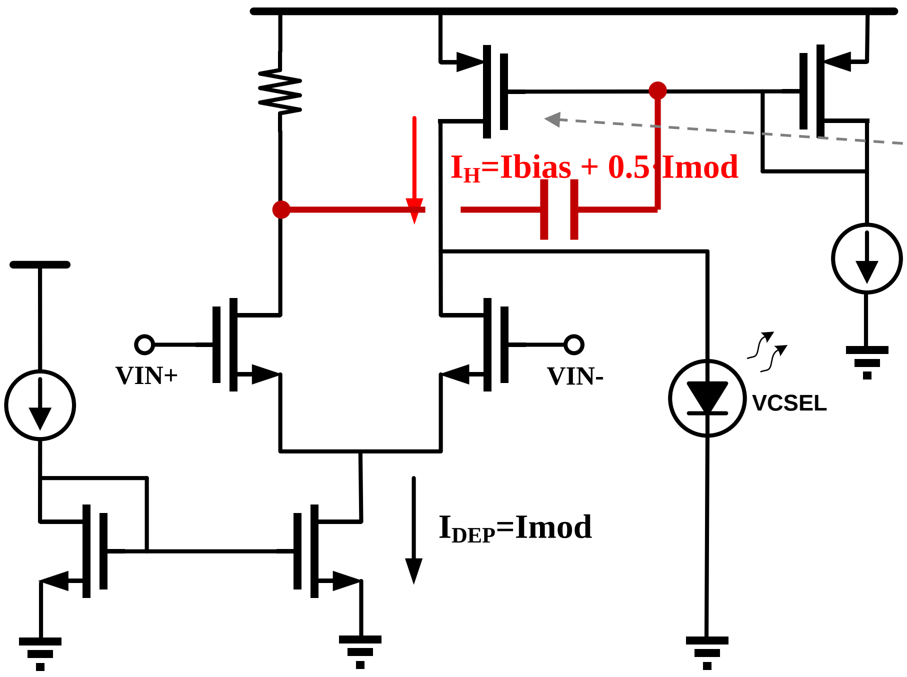
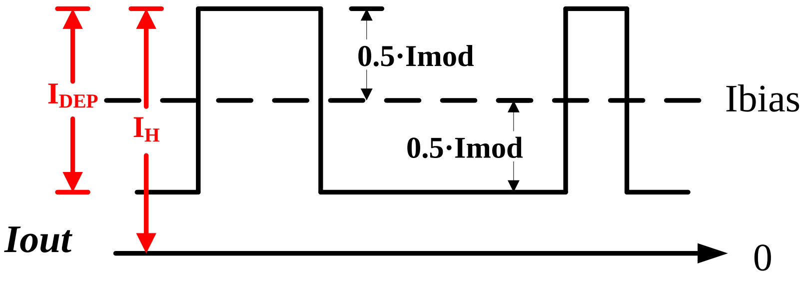
VCSEL Driver Topology



Low mobility → Large PMOS
Safeguard for radiation damage → Large PMOS



- Biasing and modulation functions are combined!
  - No external components required for biasing the laser
- Main circuit parasitics are due to the NMOS switch which carries $0.5 \cdot I_{mod}$ and the **PMOS current source which carries $I_{bias} + 0.5 \cdot I_{mod}$**
- Speed is mainly limited by the parasitics of the large PMOS needed to provide large currents
- A feedforward capacitor lightly modulates the large PMOS current source enhancing the bandwidth of the circuit.

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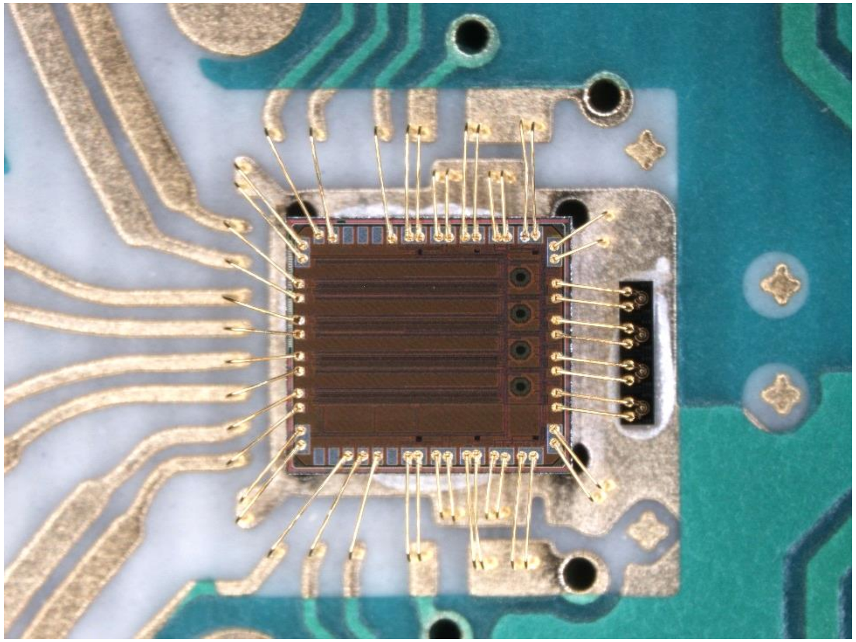
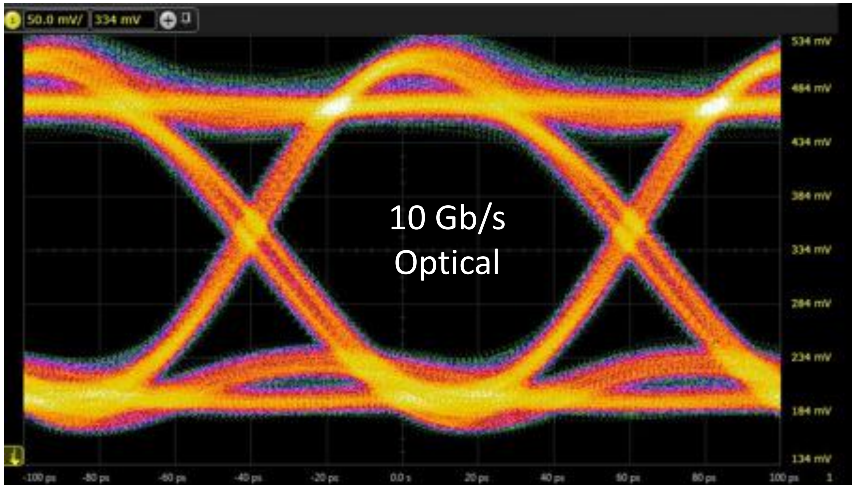
VCSEL Driver Arrays

- Three architectures studied (SMU university):
  - 4-way VCSEL driver array
  - Designed for direct bonding VCSEL arrays:
    - Single ended driving
  - Internal bias
  - Modulation and bias currents programable through I2C:
    - Modulation: 0 – 12 mA
    - Laser bias: 0 – 12 mA
- Designs fabricated and tested during 2016:
  - 10 Gb/s operation
  - Power consumption: 32 mW/ch
  - No crosstalk between channels
  - Robust up to 300 Mrad





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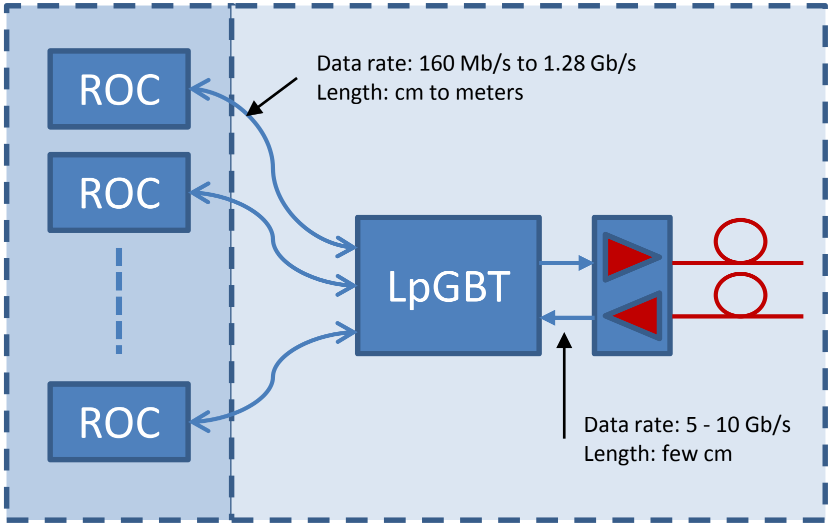
LpGBT ASIC – High Speed SerDes

- Data transceiver with fixed and "deterministic" latency both for up and down links.
  - Clocks and Data
- Down link:
  - 2.56 Gb/s
  - FEC12
- Up link:
  - 5.12 Gb/s or 10.24 Gb/s
  - FEC5 or FEC12
- E-Links:
  - Data rates:
    - 160 /320 / 640 / 1280 Mb/s
  - Count:
    - FEC5
      - Up to 28 @ 160 Mb/s
      - Up to 7 @ 1.28 Gb/s
    - FEC12
      - Up to 24 @ 160 Mb/s
      - Up to 6 @ 1.28 Gb/s



- Power dissipation:
  - Target: ≤ 500 mW @ 5.12 Gb/s
  - (GBTX is ~2W, all functions active)
  - Small Footprint:
  - Size: 9 mm x 9 mm
  - Fine Pitch: 0.5 mm
  - Pin count: 289 (17 x 17)
- Radiation tolerance:
  - 200 Mrad
  - SEU robust

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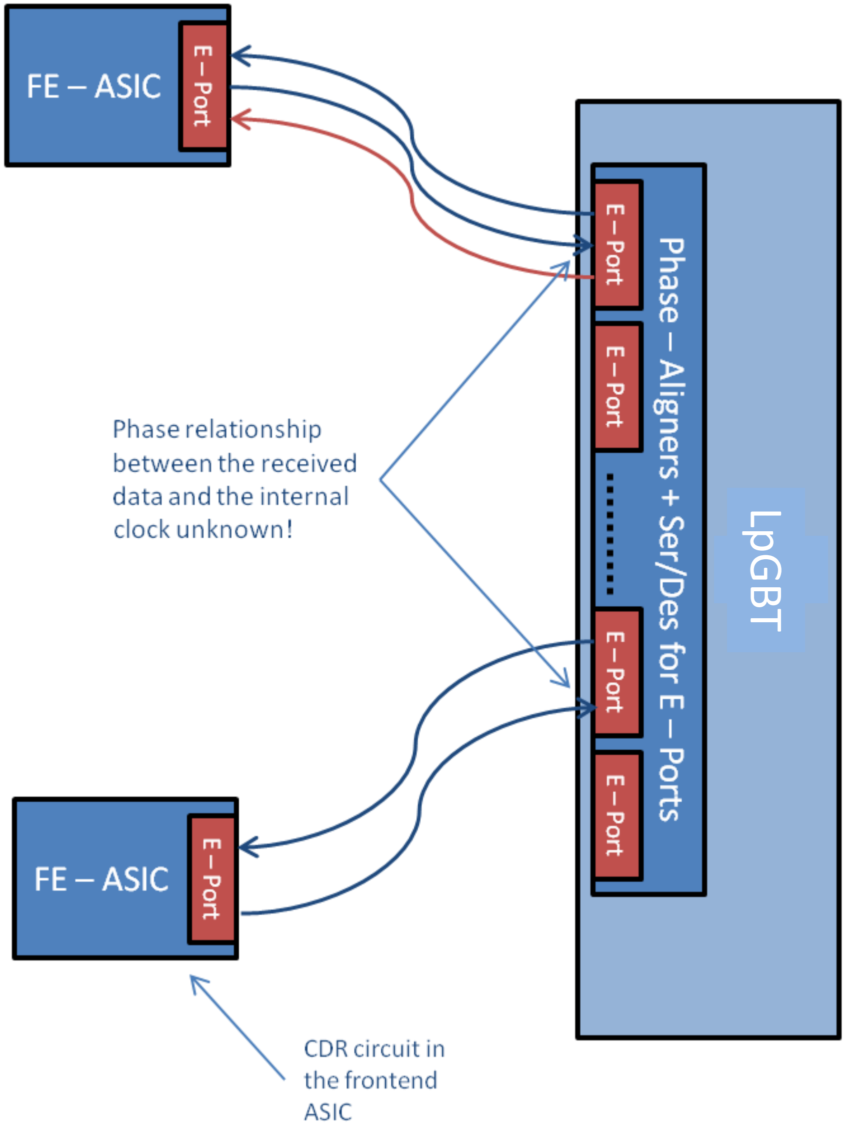
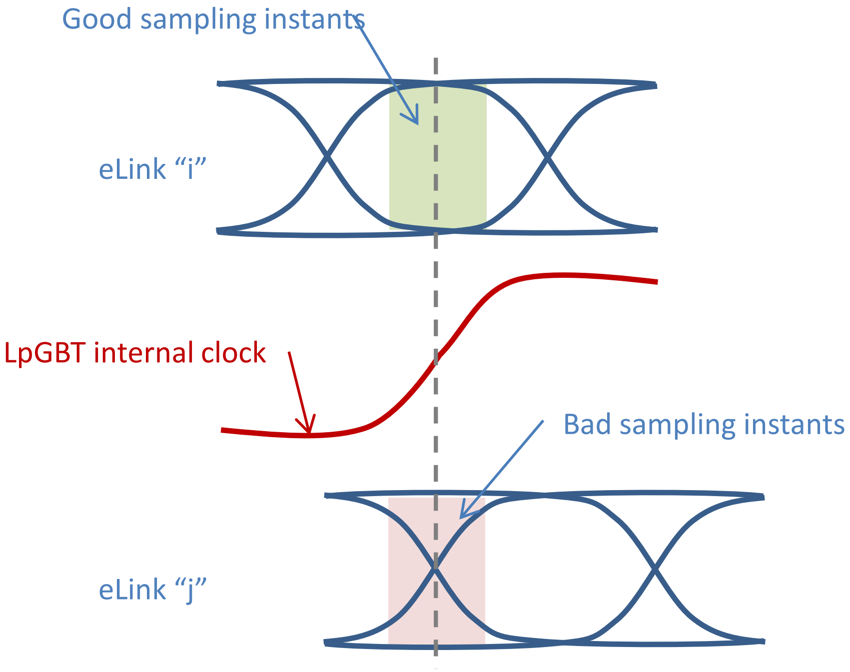
Up eLink – Phase Alignment



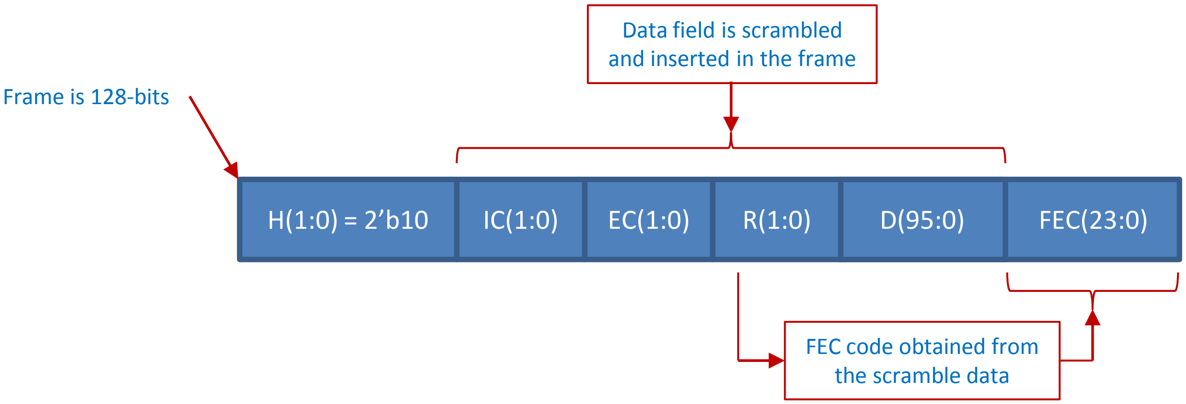
Phase relationship between the received data and the internal clock unknown!

CDR circuit in the frontend ASIC



- The phase of the incoming data signals is "unknown" in relation to the internal sampling clock!
- There are up to 28 eLink inputs (potentially) all with random phase offsets
- The solution:
  - "Measure" the phase offset of each eLink input
  - Delay individually each incoming bit stream to phase align it with the internal sampling clock

Uplink Frame: FEC 12 @ 5.12 Gb/s



- Header delimits the frame:
  - Header detection uses a robust algorithm for SEU tolerance
- Data to be transmitted is first scrambled:
  - Scrambling randomizes the data ensuring "DC balance" and a high density of "0-to-1" and "1-to-0" transitions to enable clock recovery
  - Scrambling adds no bandwidth overhead
- Forward Error Correction field is added to the frame:
  - Reed - Solomon FEC code used
  - FEC12: correction up to 12 consecutive wrong bits
  - H + FEC12 imposes a bandwidth penalty:
    - Efficiency 80% (as 8B/10B but with error correction capability)
  - Optionally, FEC5 can alternatively be used for applications requiring higher bandwidth efficiency (efficiency 91%)

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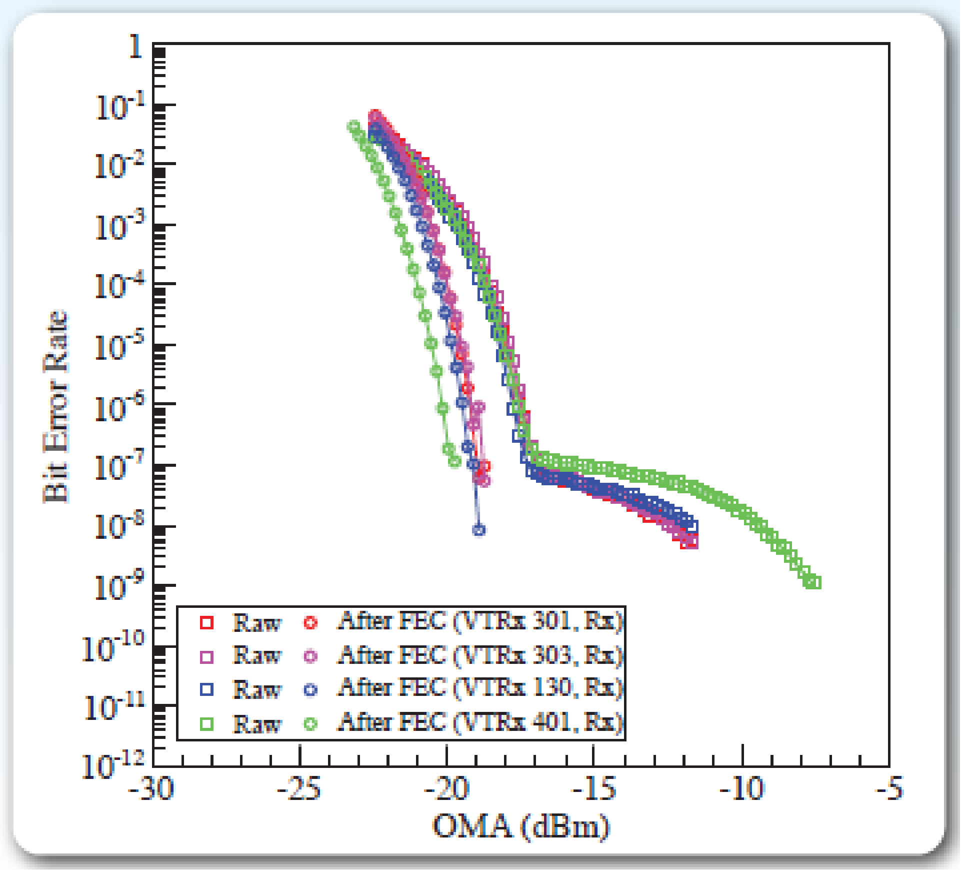
SEU Mitigation with the GBT Protocol

- FEC codes can achieve orders of magnitude improvement of BER on:
  - Systems dominated by random noise
  - Systems dominated by error burst, provided the burst length falls inside the error correction capability of the code:
    - Errors on PIN - Receivers are within this category (with occasional exceptionally long bursts)



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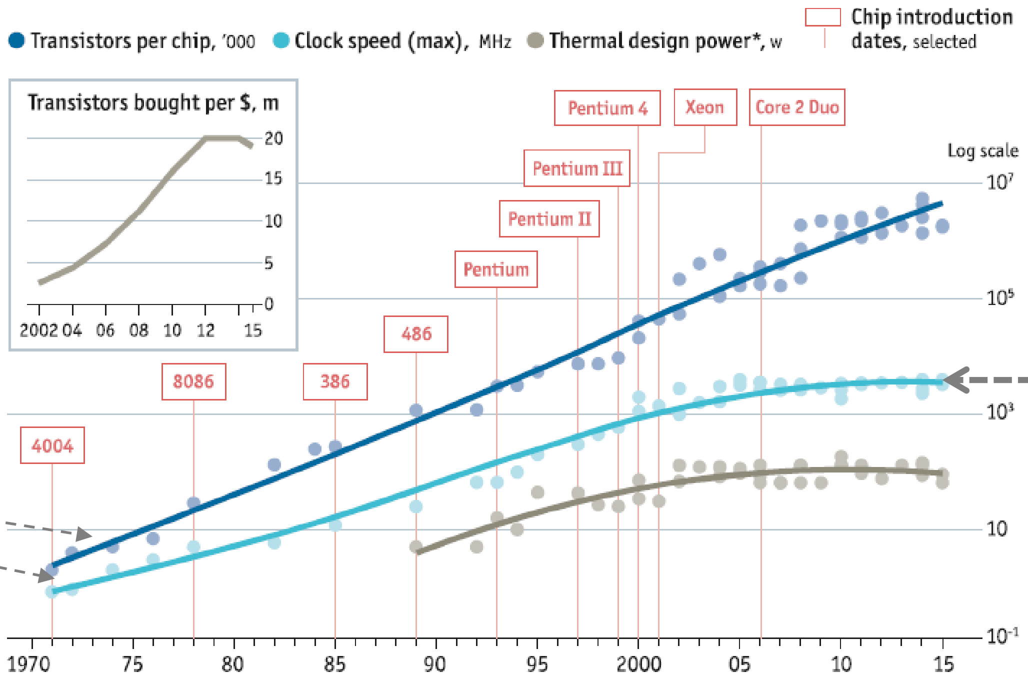
LpGBTX Power and Scaling (1/2)

- The LpGBTX power consumption dream is:
  - P = 500 mW (¼ of the GBTX!)
- Bandwidth:
  - Higher ePorts: 320 Mb/s (max) → 1.28 Gb/s
  - Up link: 4.8 Gb/s → 5.12 / 10.24 Gb/s
- How much can we get from technology scaling?
  - Scaling:
    - Two generations: 130 nm → 65 nm
    - $\alpha = 1.43 \rightarrow$ [Two generations] $\rightarrow \alpha_{IDEAL} = 2$
    - $\alpha_L = \alpha_W = \alpha = 130\text{ nm} / 65\text{ nm} = 2$
    - $\alpha_V = 1.5\text{ V} / 1.2\text{ V} = 1.25$
    - $\alpha_{OX} = 3.03\text{ nm} / 2.69\text{ nm} = 1.13$



Sources: Intel; press reports; Bob Colwell; Linley Group; IB Consulting; *The Economist*

*Maximum safe power consumption

Scaling allows to:
- Increasing integration
- Increasing speed
- Improving power efficiency of transistors

- Transistor speed gains “slowing down”!
- Interconnects accounting for a larger fraction of the delays!
- Power density has to be contained!

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LpGBTX Power and Scaling (2/2)

- CMOS Power:
  - Ideal:
    - $C \times V^2 \times f \rightarrow (1/\alpha)^2 = 0.49 \rightarrow$ [Two generations] $\rightarrow 0.25$
  - Actual:
    - $\alpha_{OX} / \alpha_V{}^3 \rightarrow 0.58$

Assuming the circuit is being speedup as allowed by scaling!

- Some parts of the LpGBT, like for the GBTX, will run at 40 MHz:
  - $f \rightarrow 1$
  - Ideal
    - $C \times V^2 \times 1 \rightarrow (1/\alpha)^4 = 0.25 \rightarrow$ [Two generations] $\rightarrow 0.062$
  - Actual
    - $\alpha_{OX} /(\alpha_L \times \alpha_W \times \alpha_V{}^2) \rightarrow 0.18$

Not accounting for interconnect capacitance and leakage currents!

- eLink drivers:
  - If signal amplitude remains the same (SLVS), only the supply voltage scales:
    - $I \times V \rightarrow 1/\alpha_V \rightarrow 0.8$

For significant gains, the signalling amplitudes need to be reduced!

- Fast Current Mode Logic:
  - Ideal:
    - $V_{DD} \times W \times J_{opt} \rightarrow 1/\alpha^2 = 0.49 \rightarrow$ [Two generations] $\rightarrow 0.24$
  - Actual:
    - $1/\alpha_V \times 1/\alpha_W \times 1 \rightarrow 0.4$

Keeping current density constant for optimum speed operation

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Low Power: Architecture Optimization, a Must!

Technology Scaling: 130 nm → 65 nm

Voltage Scaling: 1.5 V → 1.2 V

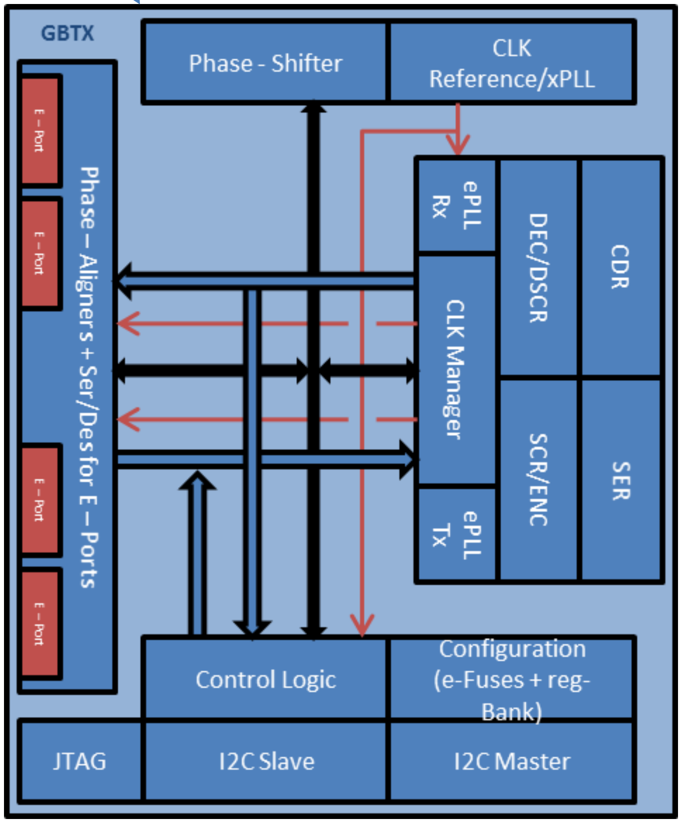
Signaling Scaling (eLinks): 200 mV → 100 mV

Clock multiplication simplified: × 120 → × 128

Function sharing: One PLL serves all!

Up to 7 PLLs can be active

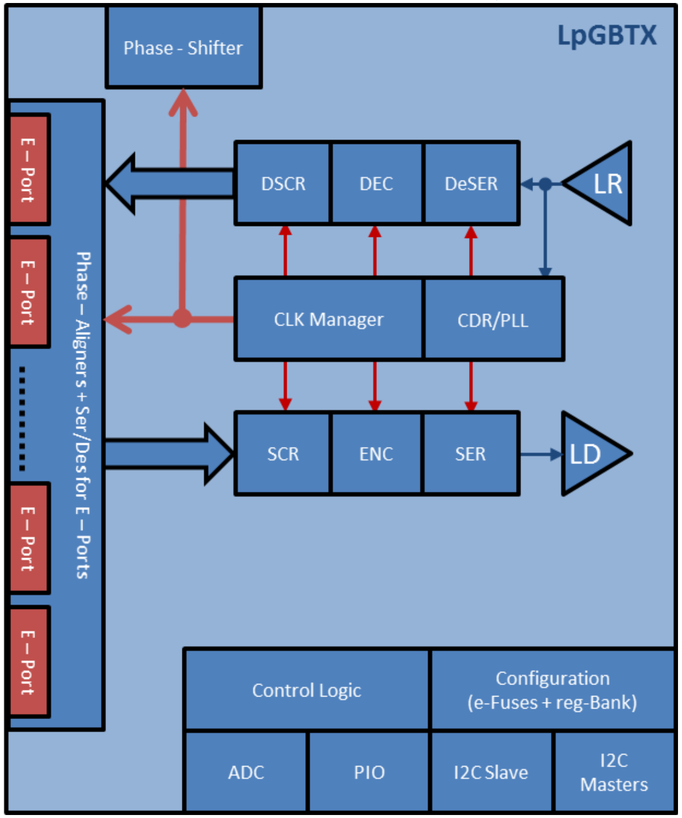
GBTX



Simplified clock generation scheme

Single PLL implements all the functions

LpGBT



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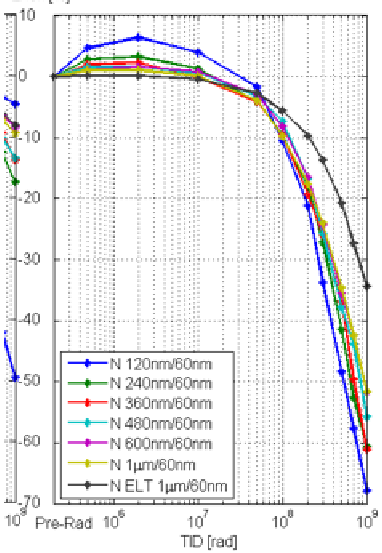
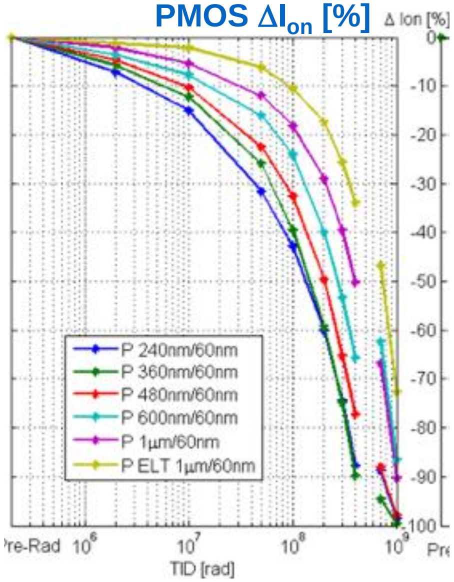
TID Induced "I_{on}" Degradation – 65 nm Technology

- PMOS are more sensitive to TID than NMOS:
  - Minimum size NMOS: -20% @ 200 Mrad
  - Minimum size PMOS: -60% @ 200 Mrad
- TID induced ΔI_{on} degradation is a function of the channel length L!
  - The longer, the smaller the degradation, but
  - <u>High speed circuits need minimum L transistors!</u>
- ΔI_{on} degradation is also a function of the channel width W:
  - The wider, the smaller the degradation
- Enclosed Layout Transistors (ELT) are the least sensitive!
- Depending on the circuit function, the use of large W might introduce a power penalty!
  - Particularly important for digital circuits where the gate count is high!

NMOS ΔI_{on} [%]



PMOS ΔI_{on} [%]



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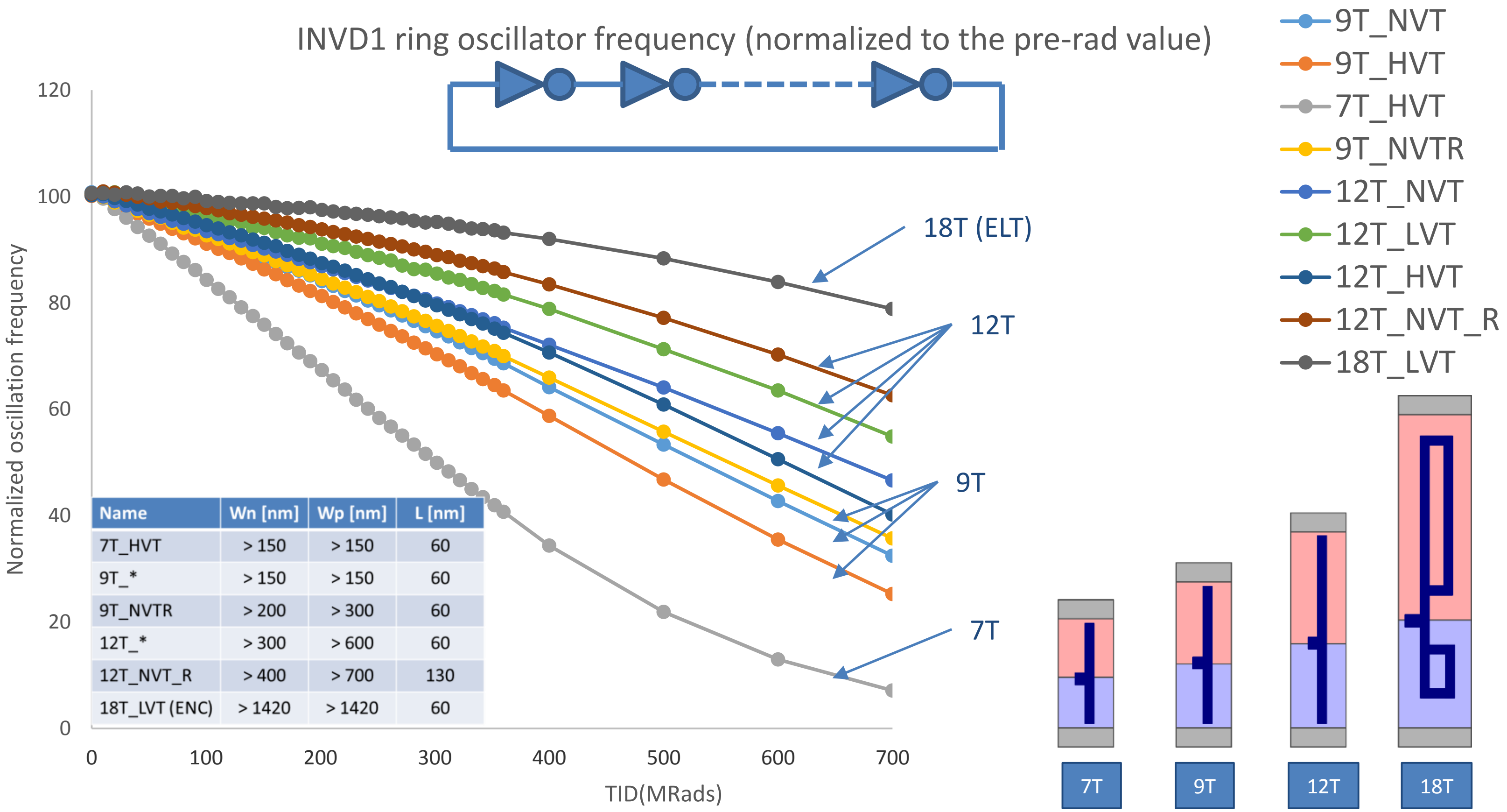
Evaluating the Sensitivity of Standard Cell Libraries (DRAD)

- Set of ring oscillators irradiated up to 700 Mrad (at room temperature):
  - No annealing step shown
- As expected, from the tests of individual devices, libraries made out of large devices are more tolerant than the smaller devices counter parts
  - Large devices lead to large power dissipation!


INVD1 ring oscillator frequency (normalized to the pre-rad value)

Name	Wn [nm]	Wp [nm]	L [nm]
7T_HVT	> 150	> 150	60
9T_*	> 150	> 150	60
9T_NVTR	> 200	> 300	60
12T_*	> 300	> 600	60
12T_NVT_R	> 400	> 700	130
18T_LVT (ENC)	> 1420	> 1420	60

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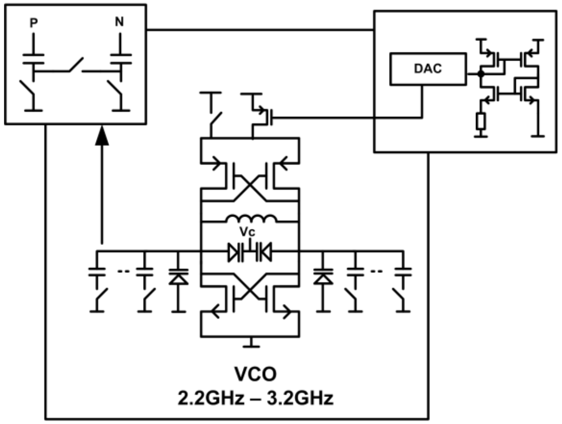
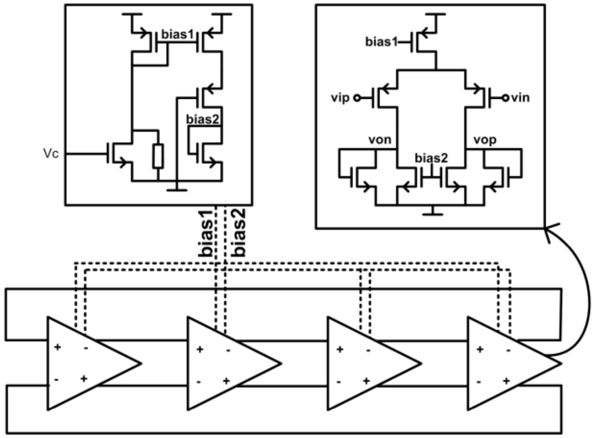
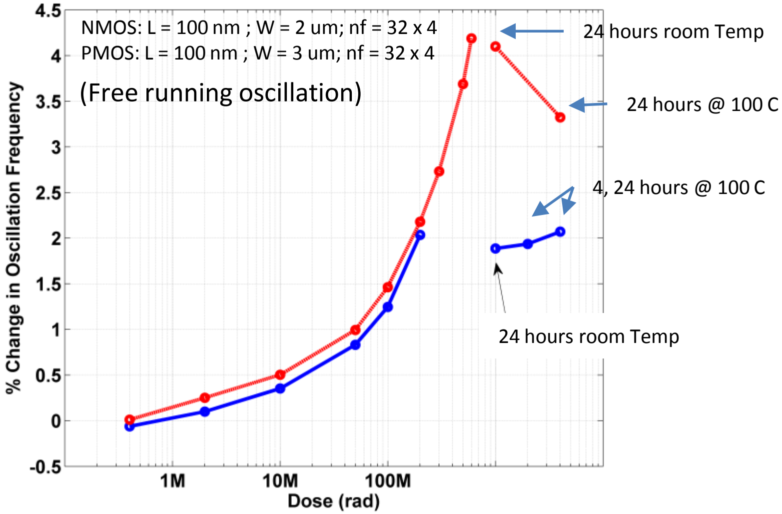
Topology Matters!





- Two PLLs working at 2.5 GHz
- Same circuits except the VCO:
  - LC VCO
  - Ring oscillator VCO
- Same power dissipation
- Same loop dynamics

- Pre/post-rad jitter (rms):
  - LC: 0.3 / 1.0 ps
  - RO: 5.6 / 22 ps
- 600 Mrad + Annealing:
  - LC: Δf < 5% (LC: Passives set the frequency)
  - RO: Δf < 40% (Ring: Actives set the frequency)



NMOS: L = 100 nm ; W = 2 um; nf = 32 x 4
PMOS: L = 100 nm ; W = 3 um; nf = 32 x 4

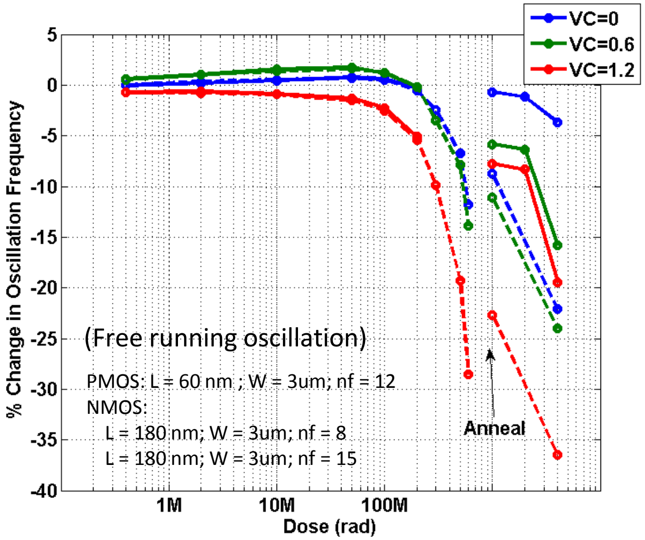
(Free running oscillation)

24 hours room Temp

24 hours @ 100 C

4, 24 hours @ 100 C

24 hours room Temp



(Free running oscillation)

PMOS: L = 60 nm ; W = 3um; nf = 12
NMOS:
L = 180 nm; W = 3um; nf = 8
L = 180 nm; W = 3um; nf = 15

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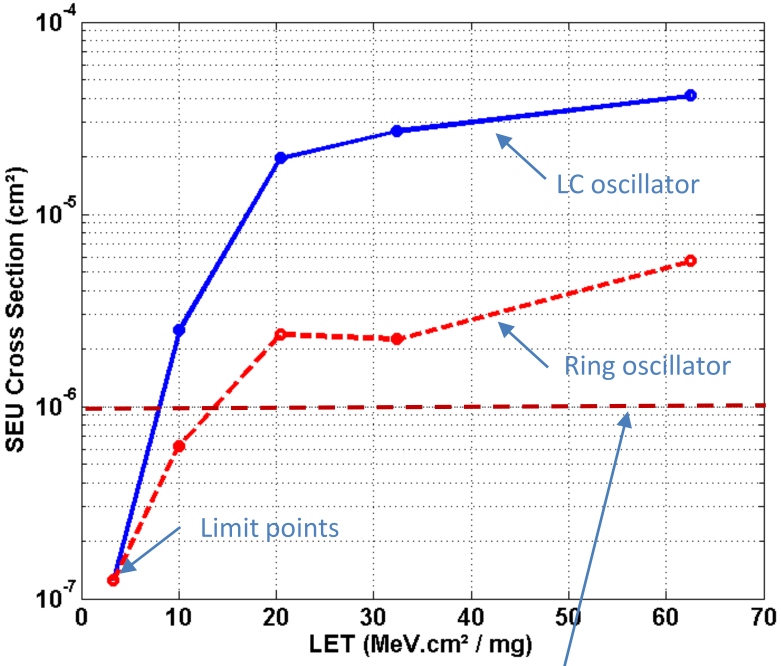
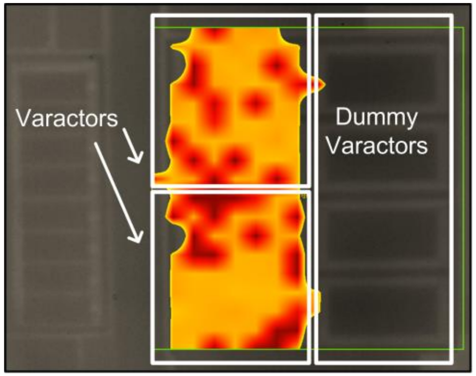
Ring / LC oscillator test PLL – SEUs

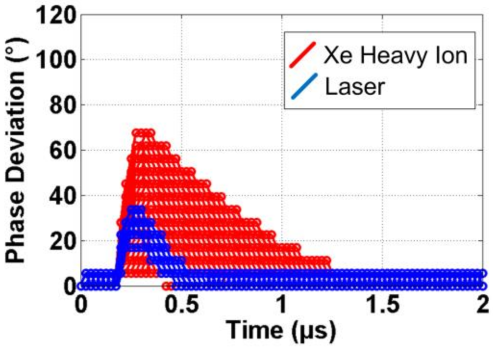
- Heavy ion testing:
  - LET: 3.2 to 69.2 MeV.cm^2/mg
- LC oscillator displays a significantly higher sensitivity than the ring oscillator!
  - Contrary to expectations!
- SEU Phase jumps:
  - Type: phase unlock
  - Ring oscillator: both polarities
  - LC: Mainly positive
- Two-Photon Absorption (TPA) laser tests point to the VARACTOR as the main culprit!
  - Total cross section of the LC-oscillator is 4 10^{-5}cm^2 from which 70% is contributed by the varactor area!
- A new design prototyped to test the hypothesis:
  - Smaller varactor area
  - Different frequency tuning topology

See: J. Prinzie et. al. TNS submitted for publication 2016



GBTX cross section ~10^{-6} cm^2!





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TID and SEU Conspire Against Low Power in HEP

- Digital libraries with transistor sizes from: 133 % to 940% might be needed to achieve TID tolerance (depending on the operation speed):
  - Power consumption “scales up” proportionally
- CML logic will provide the ultimate TID tolerance for very fast logic circuits (>2.5 Gb/s) however CML is power hungry!
  - Only NMOS used (resistive loads)
- Ultimate SEU protection requires TMR logic, both for the data path and the clock tree:
  - 3 fold increase in the power consumption
  - Fortunately “full protection” is not always necessary
    - Although for the LpGBT “full protection” is the target, power dissipation figures might force the GBT team to review the position!
- For SEU tolerance oscillators and ring oscillators need to be implemented with large devices and large currents!

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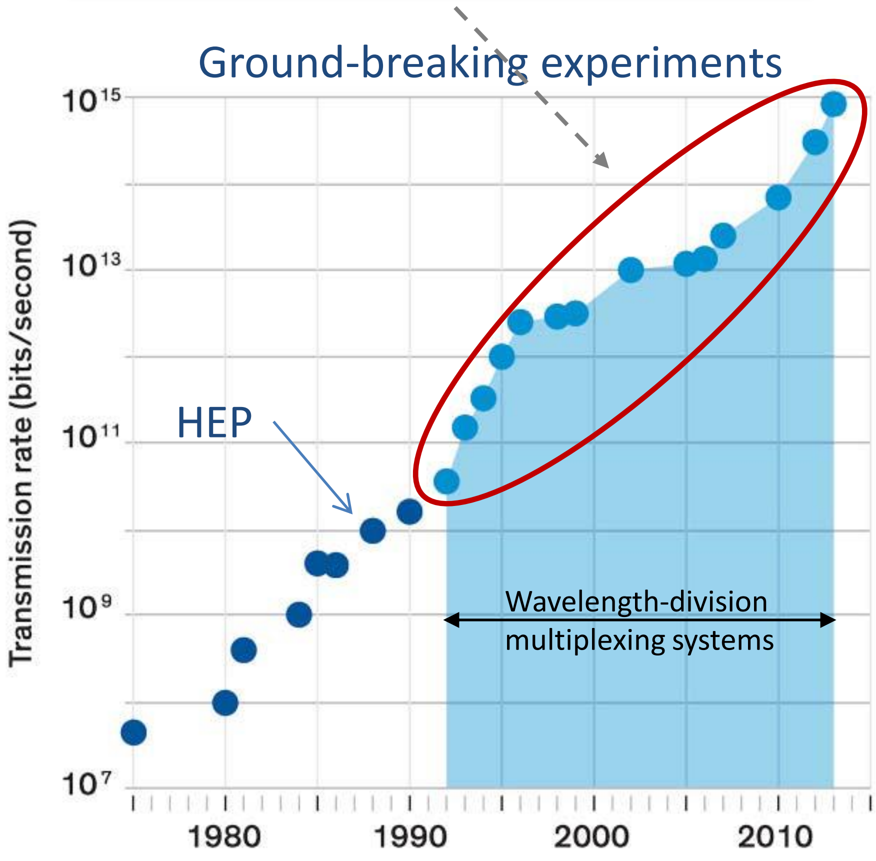
Where does HEP Stands?

- Erbium-doped fibre optical amplifiers
- Wavelength-division multiplexing (~100 channels/fibre)
- Phase modulation: Differential quadrature-shift keying
- Coherent optical systems
- Polarization-division multiplexing
- Signal processing: FEC
- Spatial-division multiplexing
- **100 Gb/s × 100 channels/fibre → ~10 Tb/s/fibre!**



Source: Jeff Hecht, IEEE Spectrum, 2016

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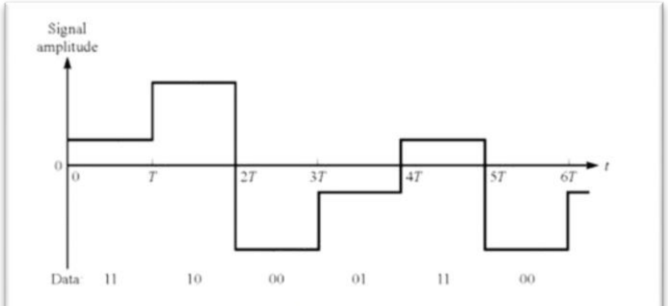
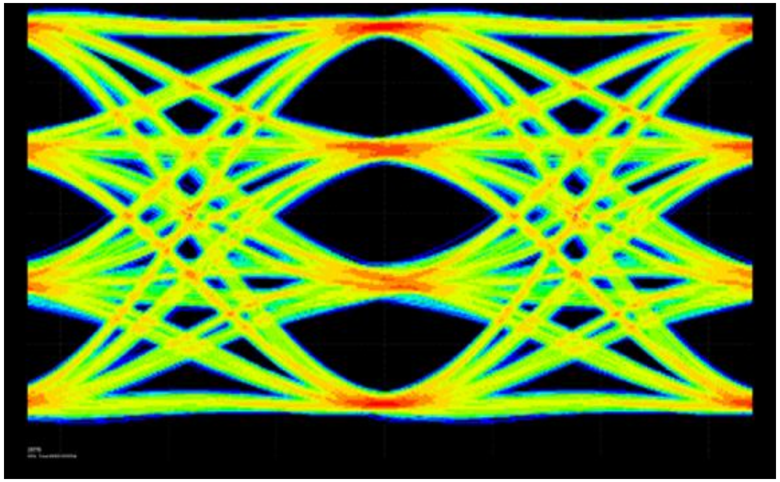
Keeping Up with the Industrial World

- On – Off Shift Keying (OOK):
  - "Symbols" represent one bit
    - "0" – dark
    - "1" – light
- Pulse – Amplitude – Modulation with Four amplitude levels PAM-4
  - "Symbols represent two bits
    - Two bits transmitted by symbol period
    - Level 0: 00
    - Level 1: 01
    - Level 2: 10
    - Level 3: 11
  - PAM-4 enables twice the transmission capacity when compared with OOK
  - The SNR is reduced (BER exponentially dependent on SNR)!
  - Transmitter and receiver circuits become rather complex!



A PAM-4 signal in time domain. T= symbol period.



- Both ALTERA and Xilinx will release FPGAs with 56Gb/s transceivers:
  - PAM4
  - 28 Gbaud/s (56 Gb/s)
- ALTERA:
  - Stratix 10
  - 14 nm Intel Tri-Gate technology
  - https://www.altera.com/solutions/technology/transceiver/overview.html
- Xilinx (FinFET):
  - UltraScale+
  - 16 nm TSMC FinFET technology
  - https://www.xilinx.com/products/technology/high-speed-serial/56g.html

Market introduction likely in two yeas' time

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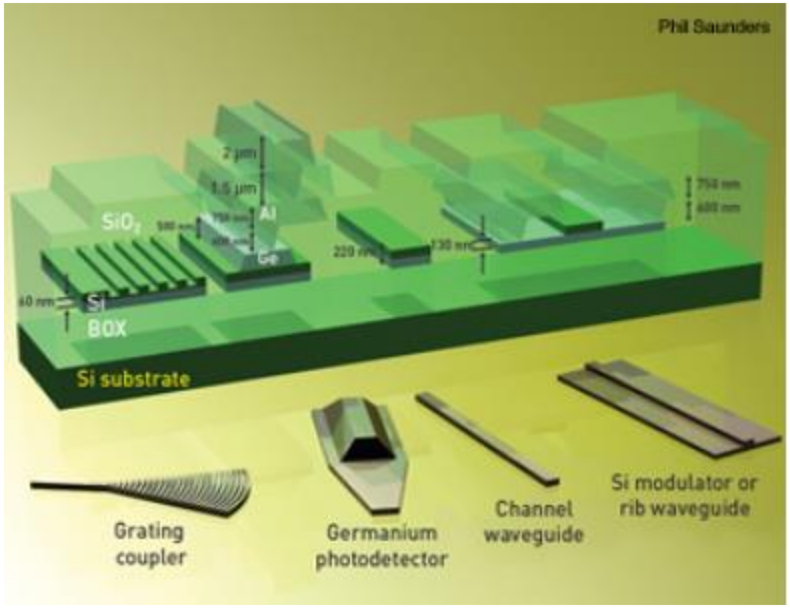
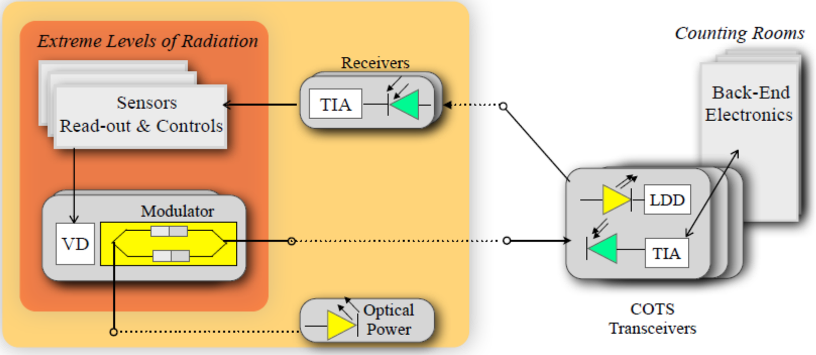
Silicon Photonics

- Silicon photonics Dream:
  - Dream: Lasers, waveguides, photo-detectors, modulators, and electronics all "grown" on the same piece of silicon
- Implementation:
  - A photonic system using silicon as an optical medium
  - Silicon is patterned with sub-micron precision into planar micro-photonic components:
    - Precise lithography technology already developed for CMOS
  - Lasers and PIN-diodes have to be made in other technologies rather than Si
- Silicon photonics research in HEP
  - Study of radiation hardness of *Mach-Zehnder* modulators:
    - Naturally hard to NIEL but not TID
  - Successful design of a TID tolerant MZ modulator
  - 10 Gb/s RadTol modulator driver design started
- It has a high integration potential and it "opens the door" to:
  - Multi channel links
  - Advanced modulation schemes
- But several challenges still to be solved for HEP systems to become a reality!





See: Francois Vasey, "Silicon Photonics for HEP Applications, Myth or Reality?"

Summary

- Optical links have enabled the construction of LHC detector systems
- Devices for Phase I upgrades are now well into the industrial production phase and R&D has started for Phase II
- Phase II upgrades will require even higher data bandwidths, very low power consumption and unprecedented tolerance to radiation:
  - TID up to **1 Grad** and NIEL up to **10^{16} n/cm^2** for inner pixel systems
- The HEP community is now developing ASICs with 65 nm CMOS technology:
  - This technology display radiation damages still not well understood by the community!
  - Testing methodologies are being developed to characterize the technology and set engineering guidelines for the ASIC designs
- The VL+ project and the LpGBT chips set are being developed to serve the Phase II upgrade requirements.
- Experiments beyond the Phase II upgrades are likely to require even higher data rates and radiation tolerance. The HEP has now turned its attention to Silicon Photonics systems as a possible answer to future HEP data transmission needs

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Acknowledgements

- This talk is based on the work done by many people across the high energy physics community.
- Impossible to make an explicit list without (unintentionally and unfairly) forgetting someone!!!

In this workshop:

- Characterization of Radiation Effects in 65nm Digital Circuits with the DRAD Digital Radiation Test Chip, Luis Miguel Jara Casas (Centro de Investigaciones Energ. Medioambientales y Tecn. - (ES)
- RD53: Radiation hard 65nm Macro Cells, Libraries and simulation models, Jorgen (CERN) Christiansen (CERN)
- Developments of two 4 × 10-Gbps radiation-tolerant VCSEL array drivers in 65 nm CMOS, Dr. Di Guo (Southern Methodist University)
- LDQ10P: A Compact Low-Power 4x10 Gb/s VCSEL Driver Array IC, Mr. Zhiyao ZENG (SOUTHERN METHODIST UNIVERSITY)
- Radiation Hardened by Design, Low Jitter, 2.56 Gbps LVDS/SLVS Based Receiver in 65 nm CMOS, Bram Faes (KU Leuven)
- The Versatile Link Demonstrator Board (VLDB), Raul Martin Lesma (Centro de Investigaciones Energ. Medioambientales y Tecn. - (ES)
- Versatile Transceiver Production and Quality Assurance, Lauri Juhani Olantera (CERN)
- Versatile Link PLUS Transceiver Development, Csaba Soos (CERN)
- A System-Level Model for High-Speed, Radiation-Hard Optical Links in HEP Experiments Based on Silicon Mach-Zehnder Modulators, Marcel Zeiler (CERN)
- WG 3 196. GBT-FPGA tutorial, Julian Maxime Mendez (CERN), Sophie Baron (CERN)

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Supporting Slides

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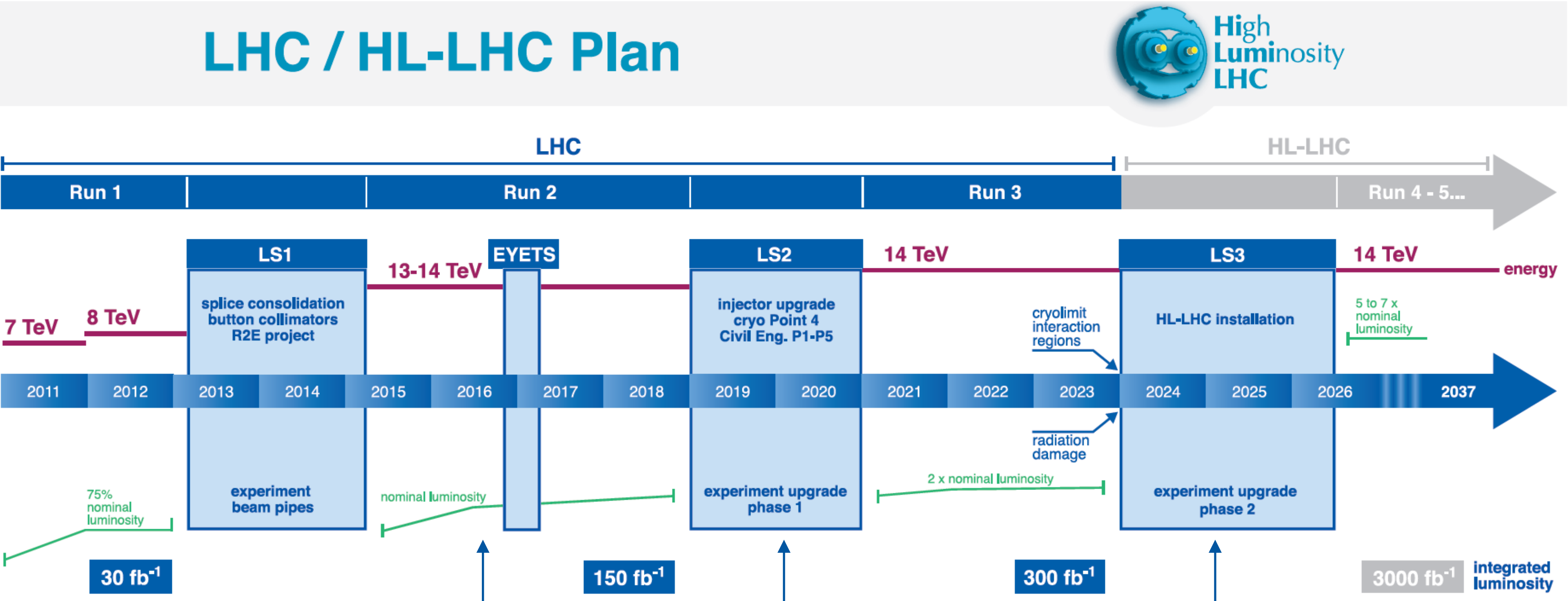
LHC / HL – LHC



NOW

PHASE I
UPGRADES

PHASE II
UPGRADES
(HL-LHC)

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ASICs & VL Procurement Quantities

	VTRx		VTTx	GBTX	GBT-SCA	GBLD	GBTIA
Experiment/User	**SM**	**MM**	**MM**				
LHCb		1955	6957	14442	6159	15869	1955
CMS HCAL	125	260	2600	0		5585	385
CMS GEM		2930		2930		2930	2930
CMS ECAL		55	120	230	45	295	55
ATLAS SmallWh		1088	512	2112	6432	2112	1088
ATLAS LArg		600		600	600	600	600
ALICE		5030	3853	8869	4960	12736	5030
BE-BI-BL	500					500	500
BE-BI-QP	500			500		500	500
BE-CO-FE							
CBM@FAIR		2500	2100	6700	2500	6700	2500
PANDA1@FAIR		220		220		220	220
PANDA2@FAIR		500		0		500	500
Total	***1125***	***15138***	***16142***	***36603***	***20696***	***48547***	***16263***

Quantities represent approximately 65k optical fibres (RX+TX)

Mainly supplied with the VTRx and VTTx

- CERN organized the procurement on behalf of the users
- ASICs Manufactured:
  - GBTIA & GBLD: full production quantities
  - GBTX: ~29k (full production Q4 2016)
  - GBT – SCA:
    - Q1 2017 prototyping quantities
    - Q3 2017 full production quantities

- Production of the Optical assemblies:
- Pre-series production concluded:
  - VTTx: 650 units (Q1 2016)
  - VTRx MM: 500 units (Q3 2016)
  - VTRx SM: 200 units (Q3 2016)
  - VTRx MM/SM Q.A. ongoing
- VTTx production launched:
  - 3000 units received
- Production devices available Q4 2016

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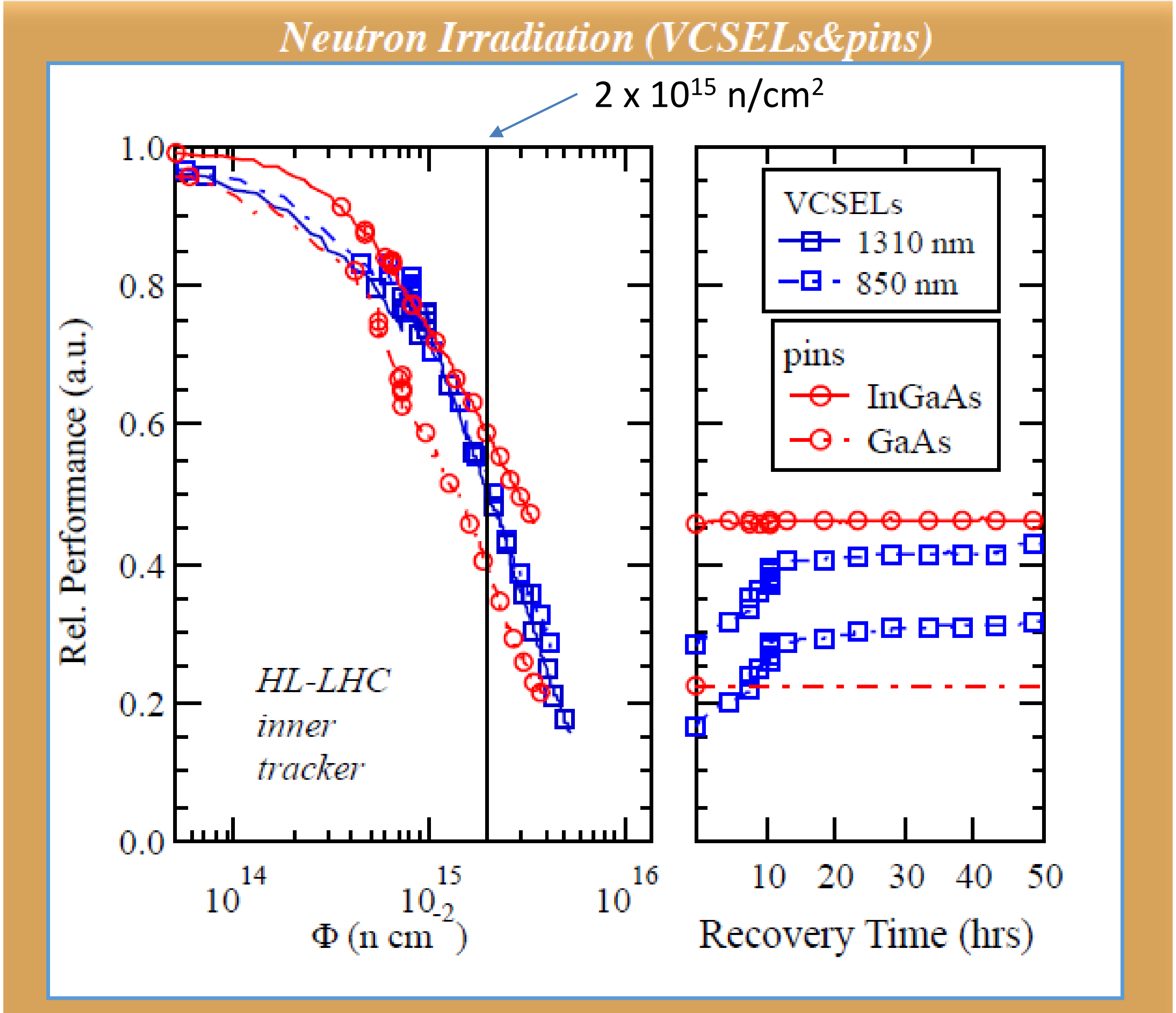
“Radiation Tolerance Limit” for VCSELs and PINs



Source: François Vasey, “Silicon Photonics for HEP Applications”, CERN-EP-ESE seminar 2016/09/16

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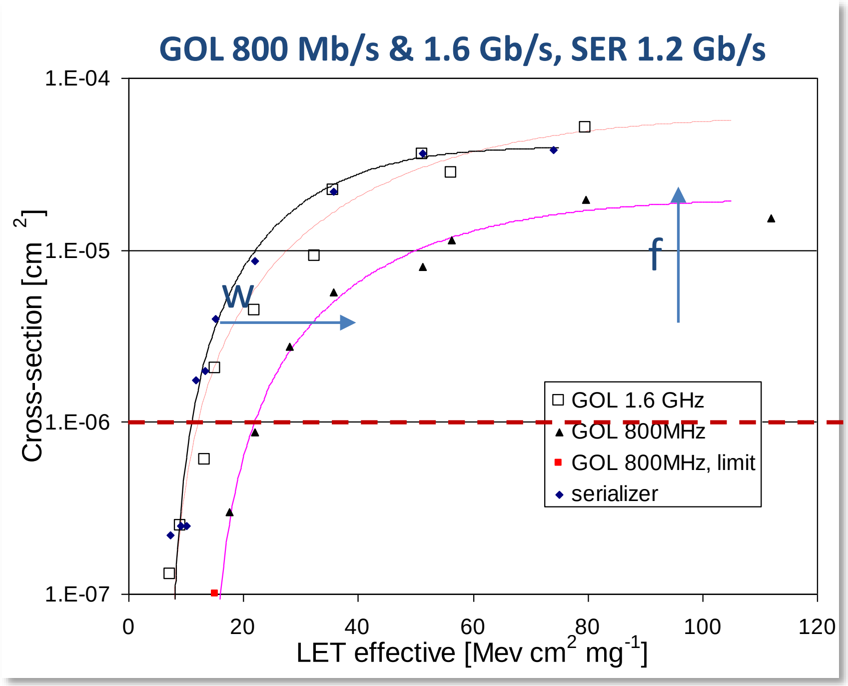
SEU – Loss of Lock Events in PLLs

GOL

GOL uses transistors four times bigger than the Serializer!

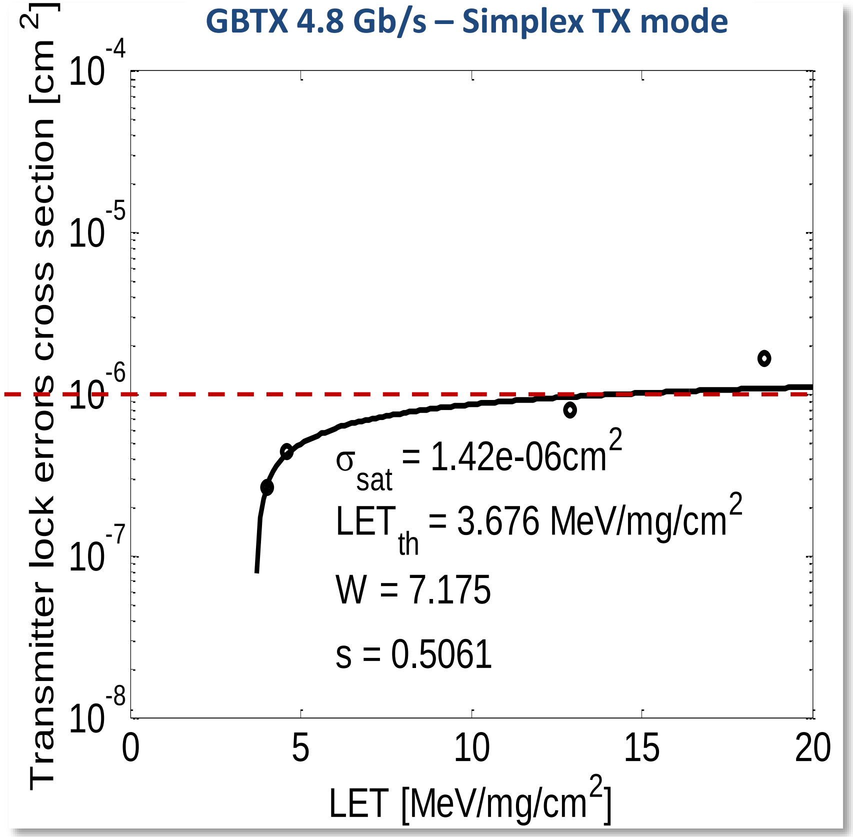


GOL 800 Mb/s & 1.6 Gb/s, SER 1.2 Gb/s

See: P. Moreira et. al., LEB 2001

GBTX

GBTX VCO design criteria: 0.3 pC injected charge (±) should result in less that 20 ps phase jump!



GBTX 4.8 Gb/s – Simplex TX mode

See: P. Leitão et. al., TWEPP 2014, JINST_053P_1114

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LpGBLD10+

Prototype:

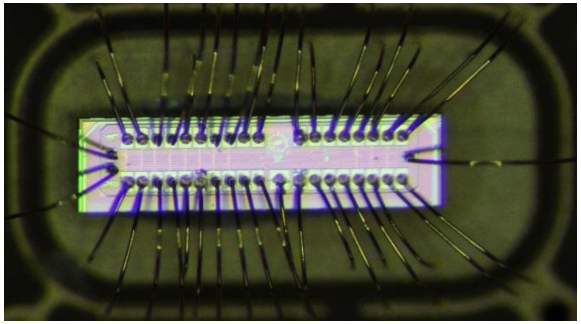
- 10 Gb/s laser driver
- A low-power
- Small-size
- 65 nm CMOS

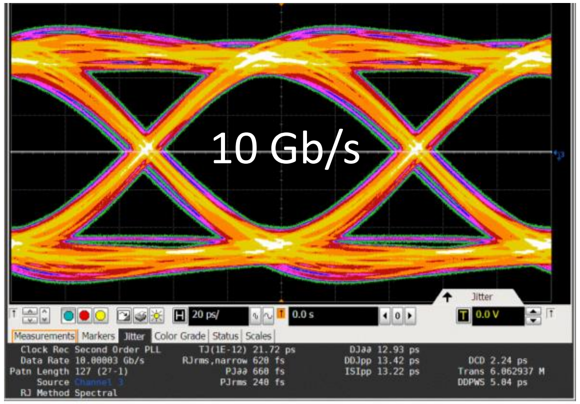
Main Features:

- **VCSEL driver**
- Laser coupling:
  - Single-ended direct bonding
- Minimum bit rate : **10 Gb/s**
- Programable rise/fall pre-emphasis
- Modulation current: 0-10 mA
- Biasing current 0-12 mA
- QFN package, and ESD protection
- Area: 1.75 mm x 0.4mm

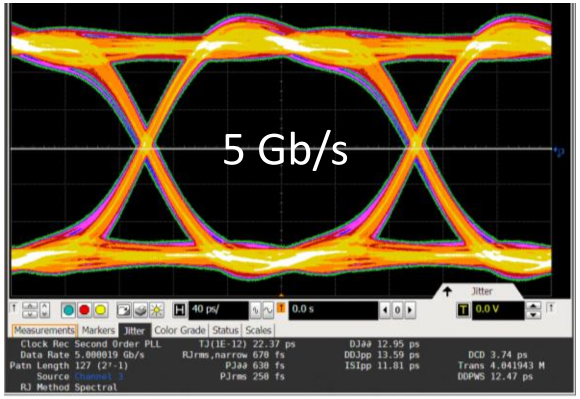
Measurement results (electrical only):

- Data rate: **10 Gb/s**
- Power dissipation: **31 mW** (typical settings)
- Jitter: **< 25 ps**





```
  Clock Rec Second Order PLL      TJ(1E-12) 21.72 ps          DJδδ 12.93 ps
  Data Rate 10.00003 Gb/s       RJrms,narrow 620 fs         DDJpp 13.42 ps          DCD 2.24 ps
Patn Length 127 (2⁷-1)                  PJδδ 660 fs         ISIpp 13.22 ps        Trans 6.062937 M
     Source Channel 3                  PJrms 240 fs                               DDPWS 5.04 ps
  RJ Method Spectral
```



```
  Clock Rec Second Order PLL      TJ(1E-12) 22.37 ps          DJδδ 12.95 ps
  Data Rate 5.000019 Gb/s       RJrms,narrow 670 fs         DDJpp 13.59 ps          DCD 3.74 ps
Patn Length 127 (2⁷-1)                  PJδδ 630 fs         ISIpp 11.81 ps        Trans 4.041943 M
     Source Channel 3                  PJrms 250 fs                               DDPWS 12.47 ps
  RJ Method Spectral
```

See: Zhang et all, TWEPP 2015

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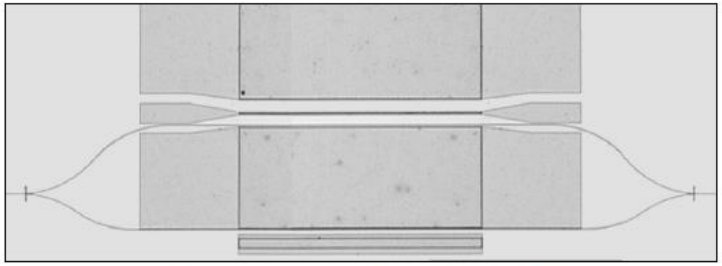
Si Modulators Performance: Power

40 Gbit/s Mach Zehnder modulator

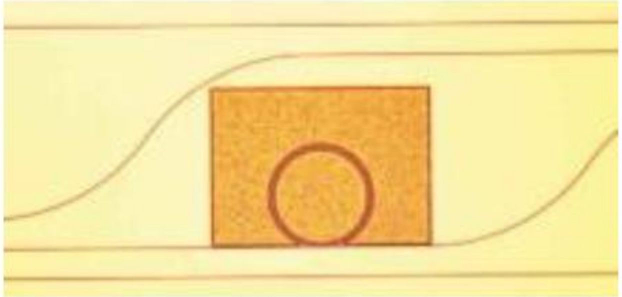


L=1.8mm => C ~0.5 pF

V_{pp} = 7 V

Energy/bit ~ 6 pJ/bit

10 Gbit/s ring modulator



Ring radius of 50 µm => C ~0.08 pF

Energy/bit ~ 0.7 pJ/bit

1pJ/bit = 1mW/Gbps

Optical wavelength-division multiplexed (WDM) links in internet
  - ~ 10 nJ/bit (total) (Tucker, 2008)

Reading from DRAM
  - ~ 30 pJ/bit (Dally, 2009)

Communicating a bit off chip
  - Several to 10's pJ/bit

Floating point operation (FLOP)
  - ~ 1pJ/bit (50 pJ for double precision (64b) operation) (Dally, 2009)

Energy stored in DRAM cell
  - ~ 10 fJ

Switching one CMOS gate
  - < 1 fJ

(1 electron at 1V, or one photon ~ 0.16 aJ)

W. Dally, "Power Efficient Supercomputing," talk at ACS, 2009
R. S. Tucker, "Energy and the Internet," OECC '08, Sydney, Australia, July 2008; also J. Baliga, K. Hinton, and R. S. Tucker, "Energy Consumption of the Internet," Optical Internet, 2007 and the 2007 32nd Australian Conference on Optical Fibre Technology. COIN-ACOFT 2007. Joint International Conference on 24-27 June 2007, Page(s):1 – 3; K. Hinton et al., "Power Consumption and Energy Efficiency in the Internet," IEEE Network 25, 2, SI pp6-12 (Mar. Apr. 2011)

Source: Francois Vasey, "Silicon Photonics for HEP Applications, Myth or Reality?"

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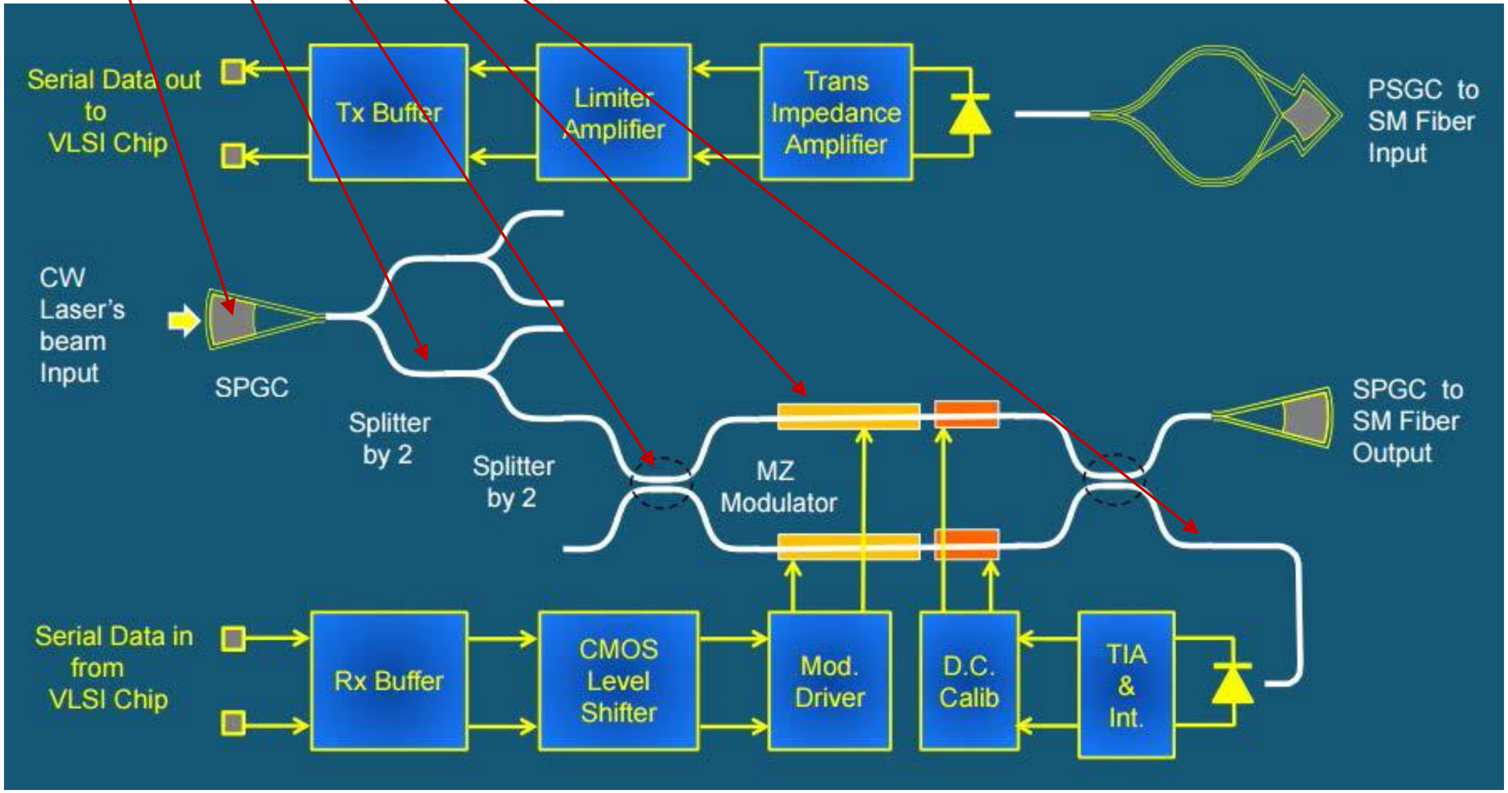
Si-Ph Transceiver System on a chip

The Insertion Loss challenge (typical loss values shown):

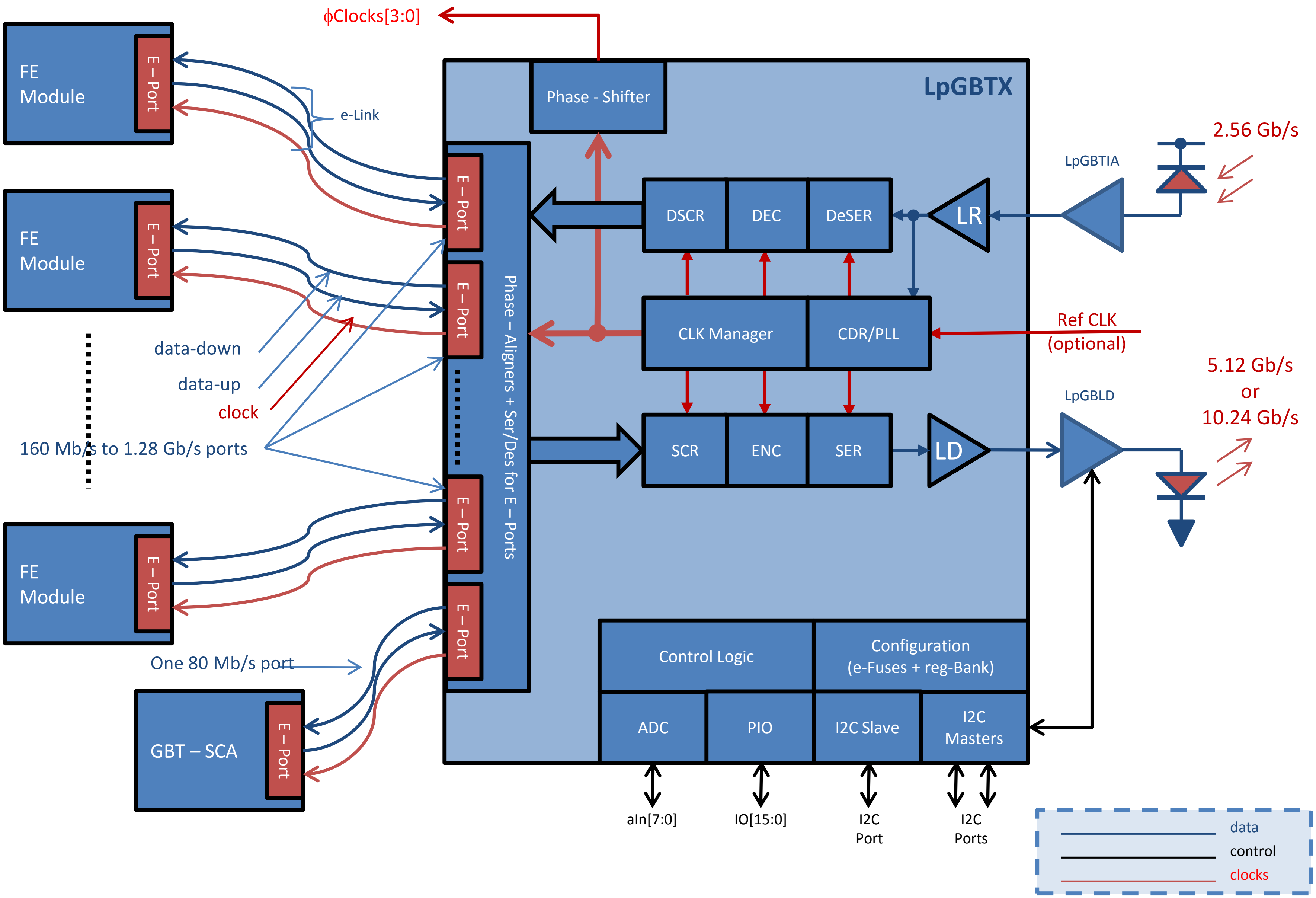
- Grating coupler: 2dB
  - Waveguide loss: 2dB/cm
    - Quadrature point: 3dB
      - Modulator loss: 4dB/mm
        - Taps and misc.: 2dB

Excess loss: typ 15dB



Source: Francois Vasey, "Silicon Photonics for HEP Applications, Myth or Reality?"

LpGBT Block Diagram (Simplified)



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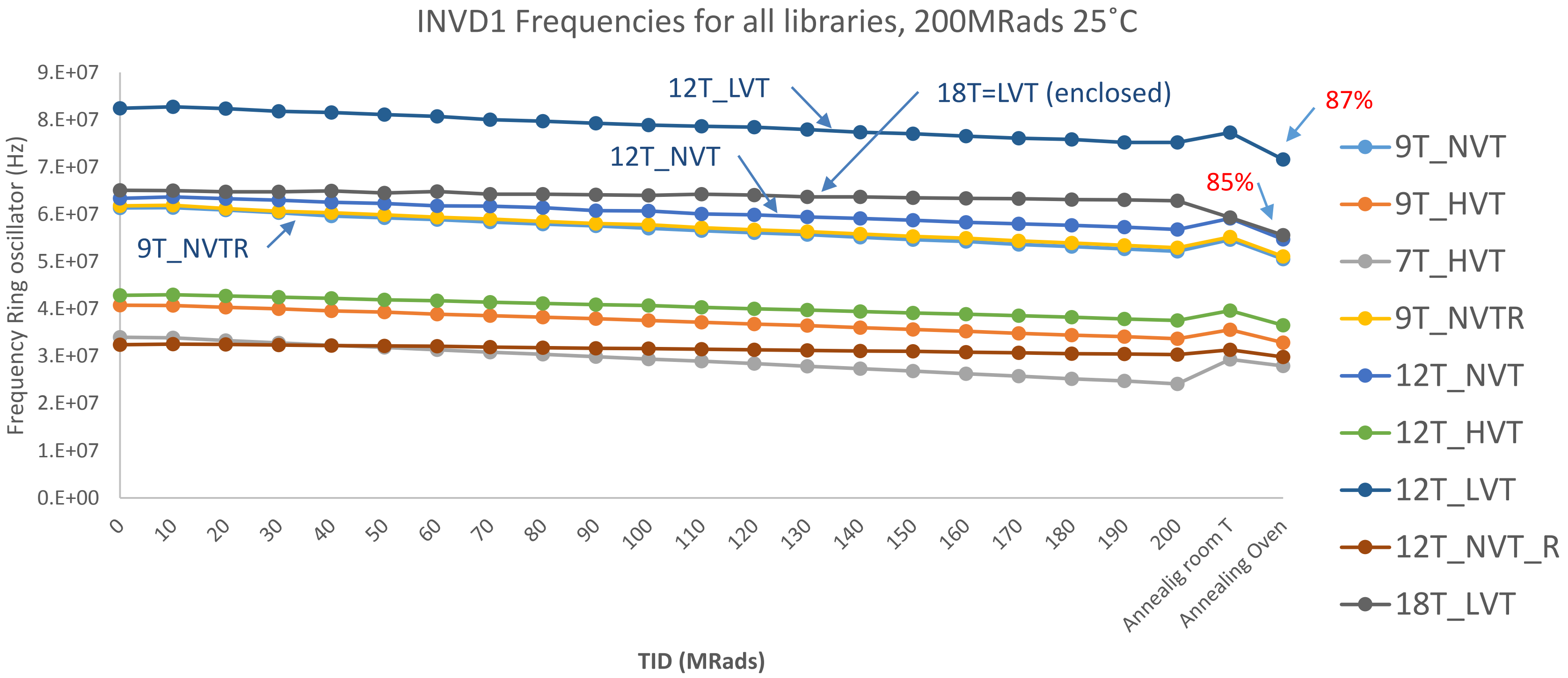
Which Library for the 1.28 Gb/s Clock Domain?

- 200 Mrad @ room temperature
  - Annealing at room temperature for 1 week
  - Annealing in the oven, 100˚C
- LpGBT targets a radiation tolerance of 200 Mrad
  - 12T_LVT library faster than the 18T_LVT (ELT & balanced) due to smaller parasitics
  - The 12T_LVT <u>seems</u> to offer the best speed/power – radiation tolerance compromise!
  - Irradiation results at <u>low</u> temperature + <u>high</u> T annealing will "tilt the scale"



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