



# xTCA Interest Group Meeting - TWEPP 2016

## Present and future xTCA developments in CMS DAQ Group

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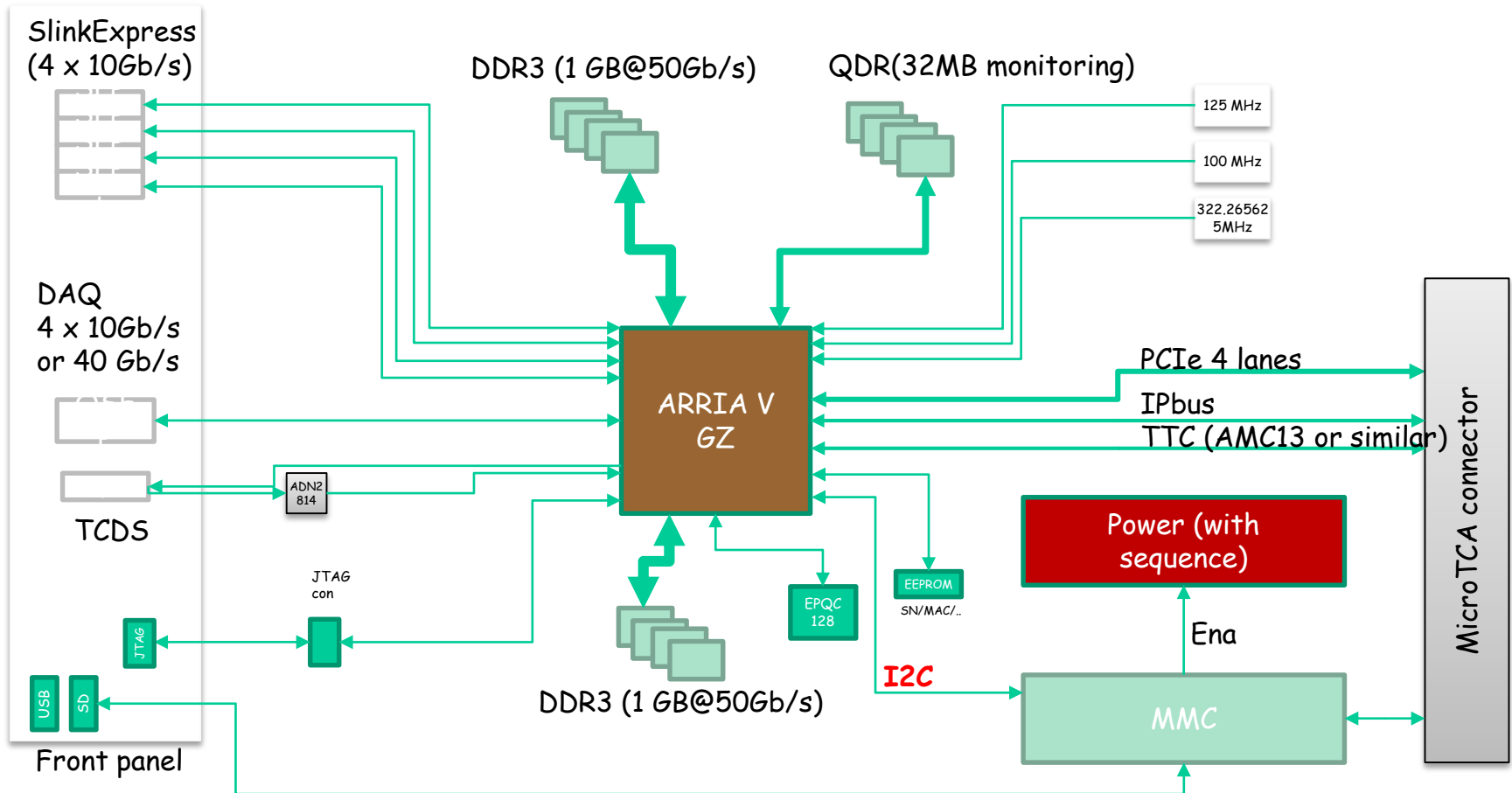


# Today's development : FEROL40

- During LS1, many new FEDs appeared under the uTCA form factor
  - Trigger systems, HCAL readout, TCDS, pilots...
- During EYETS 2016/2017, new Pixel detector will be installed
  - 112 links @ 10Gbit/s
- We don't have enough FRLs/FEROLs to cover the above needs
  - FEROL is replacing the run1 Myrinet card sitting on the FRL
  - FEROL is 1x 10Gb/s OR 2x 5Gb/s SlinkExpress input and 1x 10 GbE output
- FEROL40 project launched last year to connect those new data sources in a more efficient way, and recuperate spares needed to run until LS3
  - 4 SlinkExpress @ 10Gb/s inputs <-> 4x10GbE/40GbE output
  - Re-use of MMC design & code from EP-ESE (Julian Mendez)
  - One FEROL40 replaces 4 FRL/FEROL, is a uTCA double width AMC
  - 4 functional prototypes delivered in May
  - Production of ~50 PCBs on-going, to be received in October
  - If everything goes well, deployment in CMS early January 2017



# FEROL40 Block Diagram

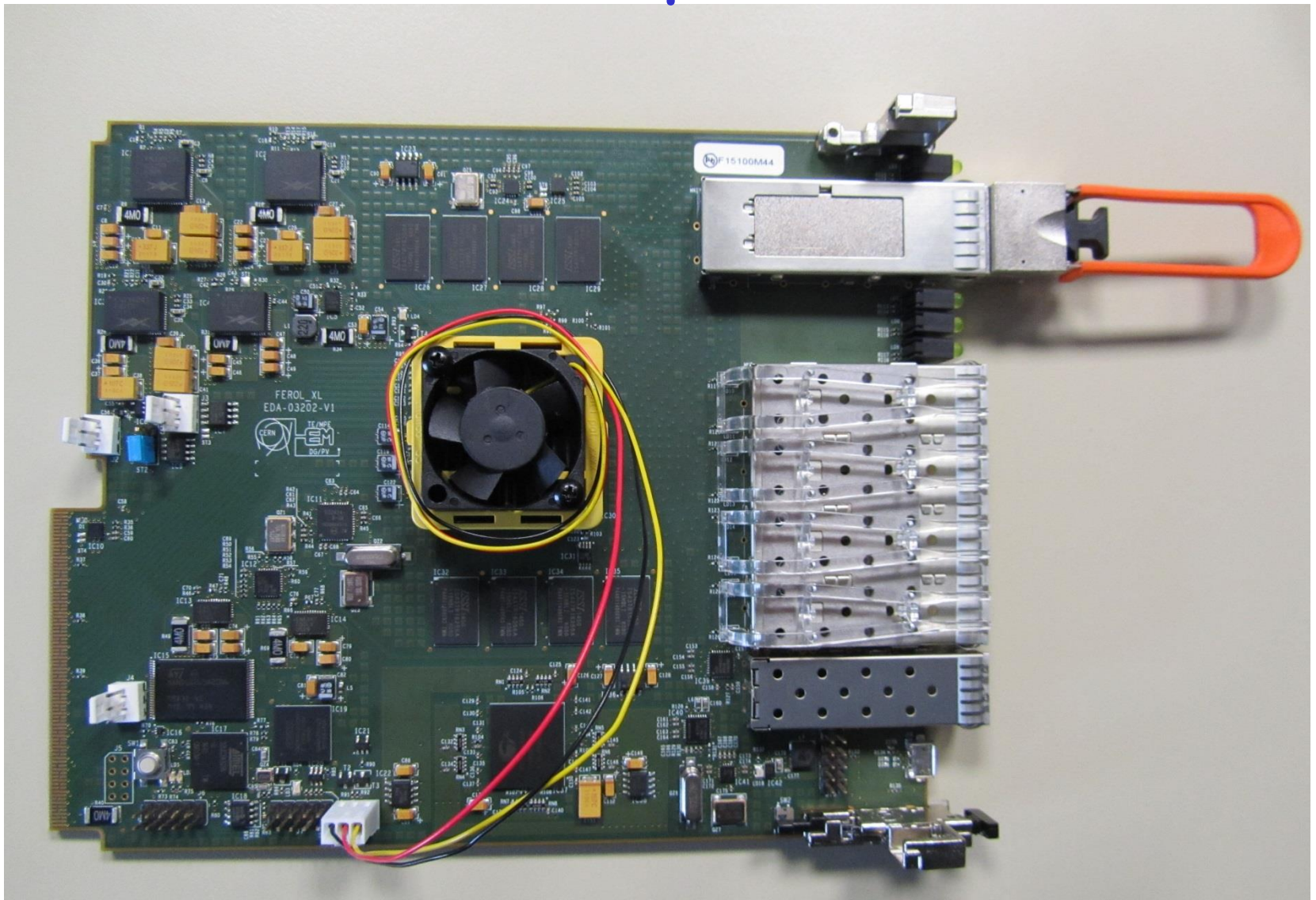








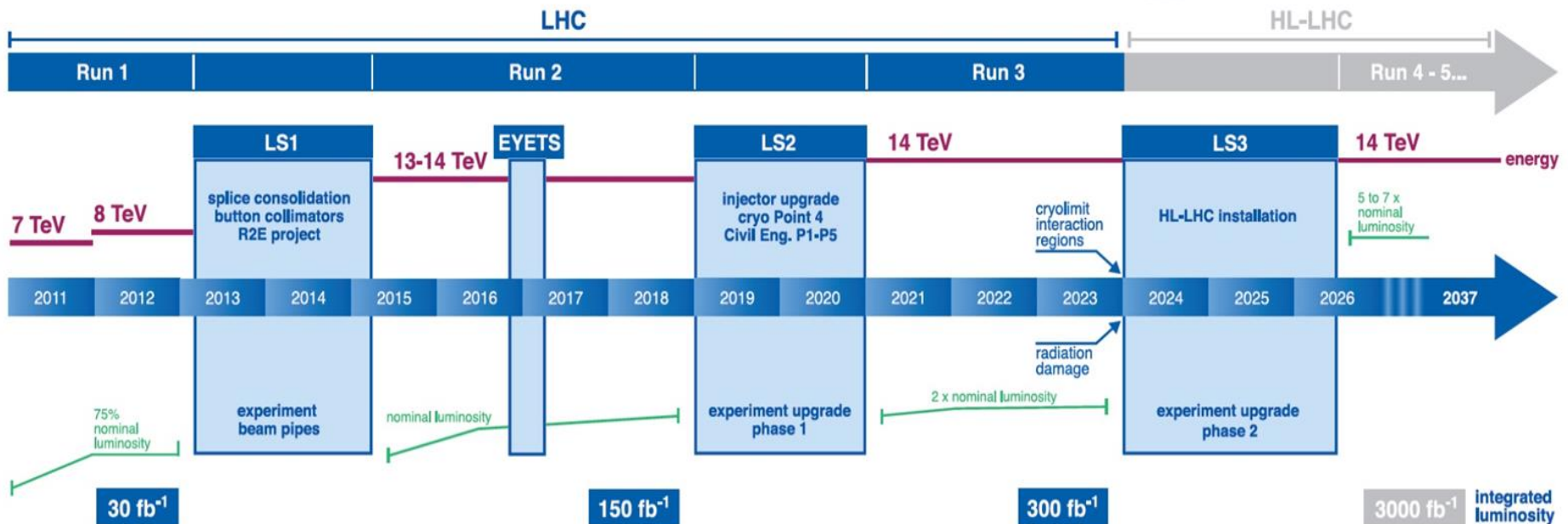
# FEROL40 picture b





# LHC operation schedule

## LHC / HL-LHC Plan





# Future developments

## Building blocks for post LS3 cDAQ

- Everything in CMS shows that the post LS3 readout systems will be based on ATCA. Hence, it is natural to think about a DAQ blade sitting in one of the hub slots of the chassis
- The overall high-level functions and final performances for such blade are :
  - Receive up to 12 data streams over SlinkExpress via the backplane
  - Today SlinkExpress is 10G, but will increase according to needs, can go up to maximum capability of ATCA backplane, i.e. 100G on fat pipes (4x25G)
  - Send data packets over TCP/IP with a matching bandwidth (i.e equiv to 12 x 100G)
  - Reception and distribution of TTC signals over the backplane
  - Collection, (pre)processing and sending of status for fast monitoring via dedicated fast link
- To reach this target, that is of course out-of-reach today 😊, we propose to go modular and proceed by steps with reduced performances (but full functionalities) and (re)-use as much as possible existing hardware and synergies from CMS subsystems and related projects



## Building blocks for post LS3 cDAQ blade

- The cDAQ blade can be split into its Data functions and its Timing/monitoring functions
  - Receive  $n$  streams of data under custom protocol (SlinkExpress)
  - Aggregate and convert the streams to TCP/IP xGbE (see what is feasible with reasonable FPGAs)
  - Receive TTC info (whatever the TTC will be)
  - Send back through same channel Fast-OR signals for trigger veto
  - Distribute TTC info to all chassis over the backplane (lines chosen to minimize perturbation on ATCA standard)
  - Collect status generated by leave cards (status set to be defined CMS wide)
  - Preprocess these status (i.e. counters, histograms, ...)
  - Sends aggregated status, monitoring info to equivalent of the FMM system today (can be TCDS but not necessarily) via dedicated link (bandwidth must allow the transfer of data for the whole chassis)
  - Past experience shows that we are always short of monitoring resources and it is increasing with the time and system knowledge



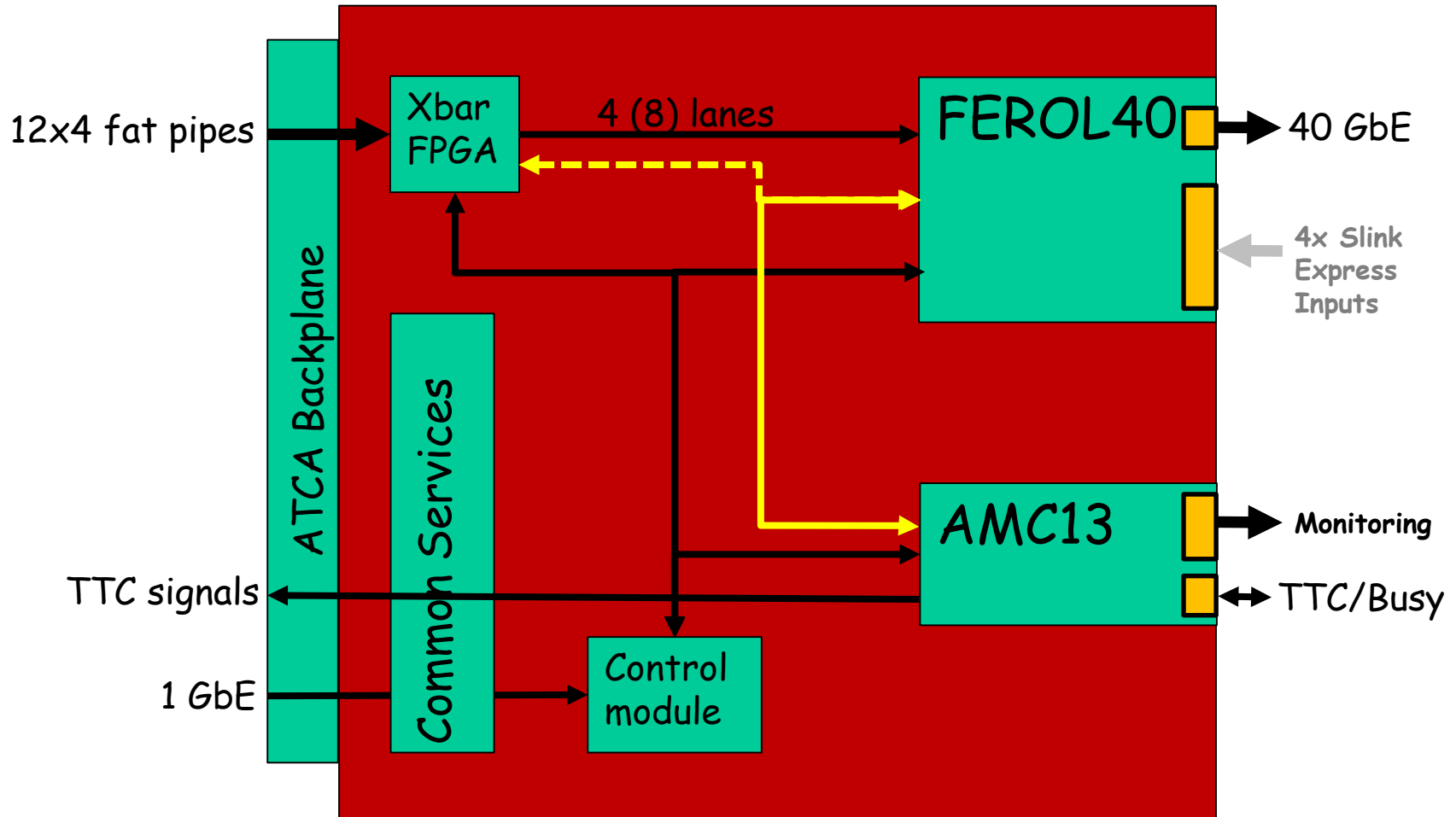


## Possible First demonstrator for a cDAQ blade

- By combining a FEROL40 and an AMC13 on a custom ATCA carrier board, we can have a functional demonstrator of a cDAQ blade
  - Limited performances for bandwidth but full functionality is achievable
  - Can be ready when first tracker proto is ready (mid 2018 ?)
- Carrier board features:
  - Provides 2 sites for FEROL40 and AMC13
  - Provides a switching device that can assign/merge dynamically backplane data streams to FEROL40 fat pipes
  - Provides backplane connectivity to Timing AMC13
  - Provides the power and services to AMCs
  - Control and management of this carrier is done via System-on-a-Module
  - For these last two items, reuse of on-going work in the "neighborhood"
- Having such demonstrator operational allows many people to work on the software stack



# Carrier board block diagram





# Next possible steps

- Once demonstrator operational, we can concentrate on :
  - a FEROL100 design ?
  - Many issues to solve like AMC connectors max speed but we have to start somewhere...
  - Start a monolithic design of the cDAQ blade ?