CERN

TE-CRG radiation tests at CHARM 2016

Irradiation test results on a Temperature Transducer prototype card using the Smartfusion2 FPGA

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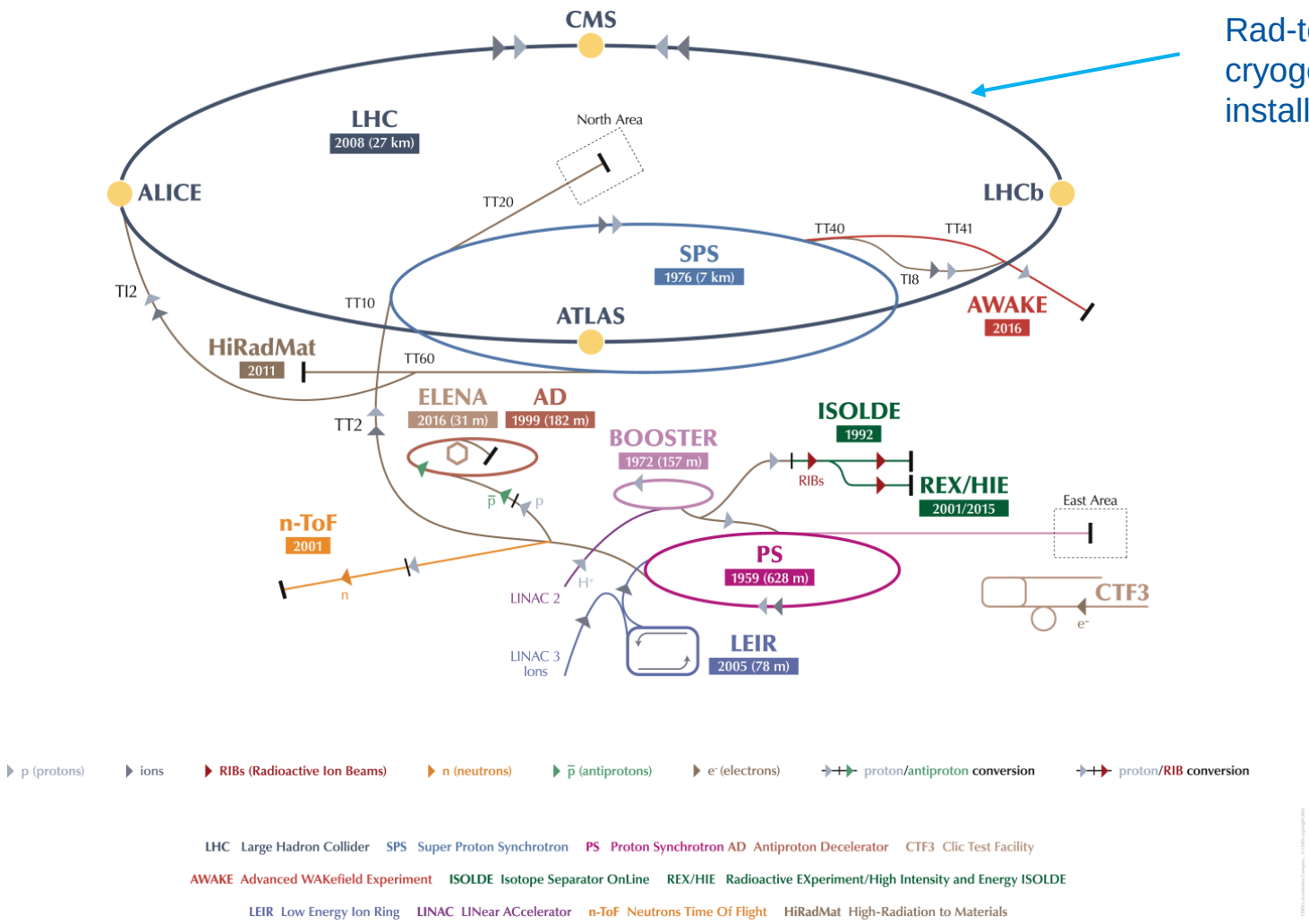
TWEPP 29/09/2016 WG: FPGA

Introduction - The CERN accelerator complex



Rad-tol electronics of the cryogenics instrumentation installed in the LHC.

Introduction - The cryogenics crate

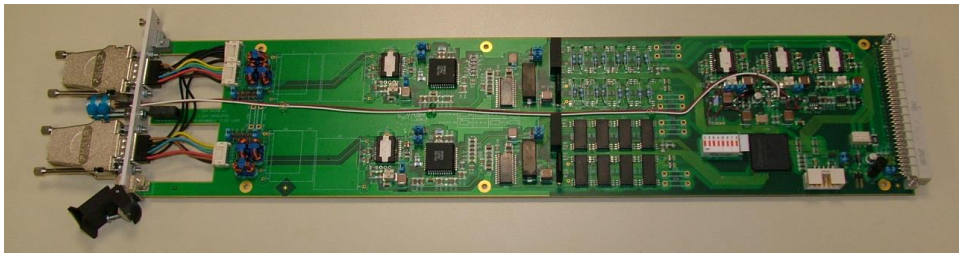
The cryogenics crate
Installed mainly in the LHC

For the LHC

800	WorldFIP crates
Active channels:	
6500	Temperature
800	Pressure
500	Liquid He level gauges
1400	Cold mass heaters
600	Beam screen heaters
1100	Mechanical Switches (I/O)
1050	WorldFIP cards (2100 channels)

- Installed in ARCs (from cell 8), shielded and protected areas
- All existing designs based on Microsemi antifuse A54SX FPGA (3 kGy)
- The rad-tol target for electronic components installed is >1 kGy (100 krad)

Generic reprogrammable insulated TT card



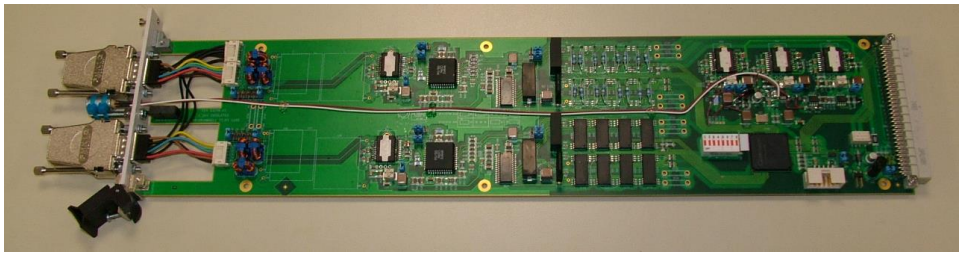
Prototype double-channel card with Smartfusion2 FPGA

Current leads require an isolated version

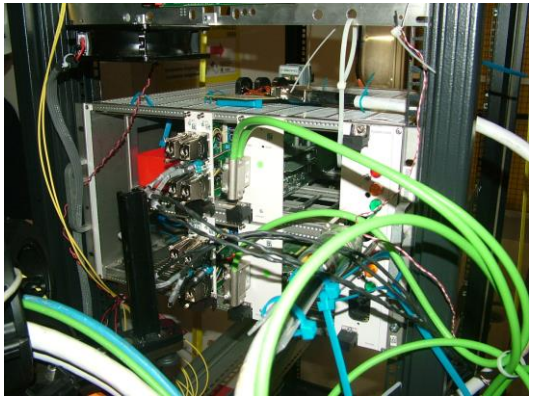
- Resistive measurements relative to precision on-board references.
- 8 x Measurements (Sensor/Reference * current flow Positive/Negative * voltage Straight/Inverse) to remove thermoelectric effects, voltage offsets and OpAmp common mode error.
- Two independent channels.

Initially, this new design was targeting non-radiation applications, but a test at CHARM was planned to explore potential use in the LHC tunnel.

FPGA code versions



Prototype double-channel card with Smartfusion2 FPGA



Crate with 4 temperature transducer cards

Supervision

FPGA: Smartfusion2
ID: M2S010T-1FGG484X417
Wafer Lot #: SKANY, Rev:2
Date code: 1526

Version considered "SEL-free"

4 cards with different FPGA code versions

- Onehot*/Safe, No TMR**
- Onehot/Safe, TMR
- Hamming 8/4***, TMR
- Hamming 8/4, TMR with with distant FFs

❖ **Using only FPGA fabric logic elements (LUT/FFs)**

*Onehot: FSM encoding with only one "1" bit per state.
**TMR: Triple Modular Redundancy on FFs only.
***Hamming 8/4: Double error detect single error correct.

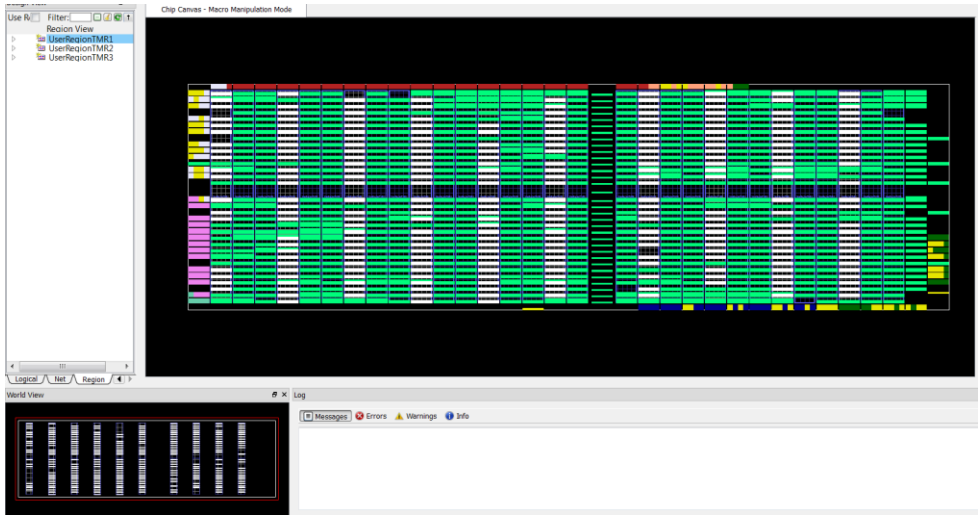
All versions offer 13-bit diagnostics per channel.

Code versions, complexity & resources

FPGA Version	4LUT	DFF	Logic element
Onehot/Safe, No TMR	3429 (28.4%)	2117 (17.5%)	3803 (31.5%)
Onehot/Safe, TMR	6871 (59.9%)	6413 (53%)	8458 (70%)
Hamming 8/4, TMR	8177 (67.7%)	6501 (53.8%)	9761 (80.8%)
Hamming 8/4, TMR with distant FFs	8177 (67.7%)	6501 (53.8%)	10680 (88.4%)

❖ **Using only FPGA fabric logic elements (LUT/FFs)**

- 10 FSMs per channel.
- FSMs will always sync, no dead-lock.
  In addition, 4 hierarchical (time) watchdogs for quick recovery.
- 15-size median filter.
- Oscillator @ 10MHz, synthesized @ 100 MHz.
- 13-bit diagnostics per channel:
  - 4 watchdogs.
  - 8 illegal FSMs or invalid data on SEU.
  - 1 ADC conversion failure.



Directives: Distance between FFs of TMR

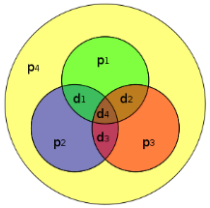
Notes on rad-tol

4 cards with different FPGA code versions

- *Onehot/Safe, No TMR**
- *Onehot/Safe, TMR*
- *Hamming 8/4**, TMR*
- *Hamming 8/4, TMR with with distant FFs*

➢ **Onehot encoding**

Original → Onehot
00 → 0001
01 → 0010
10 → 0100
11 → 1000



➢ **Hamming 8/4**: 4 bits for data, 3 data parity bits, 1 even parity bit. Double error detect single error correct on max 16 states.

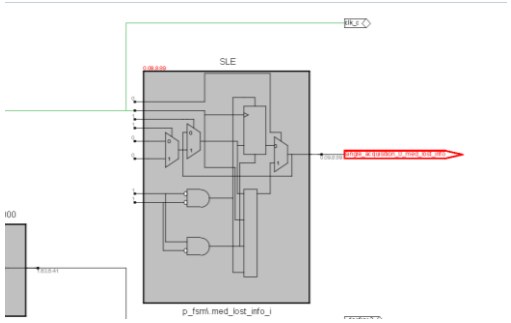
```
when others =>
...
    ParityCheck    := state(7) xor state(6) xor state(5) xor state(4) xor state(3) xor state(2) xor state(1);
    ControlBitC2   := state(7) xor state(6) xor state(5) xor state(4);
    ControlBitC1   := state(7) xor state(6)                xor state(3) xor state(2);
    ControlBitC0   := state(7)          xor state(5)       xor state(3)          xor state(1);

    if ParityCheck /= state(0) then
      if ControlBitC2 = '0' and ControlBitC1 = '0' and ControlBitC0 = '0' then
        -- single bit-error on even parity bit state(0), -> to correct
        n_state     <= state;
        n_state(0)  <= not(state(0)) ;
      else
        -- single bit-error (not in parity) at the bit position indicated -> to correct
        ErrorPositionVector     := ControlBitC2 & ControlBitC1 & ControlBitC0;
        ErrorPosition           := to_integer(unsigned(ErrorPositionVector));
        n_state                 <= state;
        n_state(ErrorPosition)  <= not(state(ErrorPosition));
      end if;
    else
      -- double bit-error, detected but NOT corrected
      n_state                                   <= ResetState;
    end if;
```

Generic "others" case for Hamming 8/4 FSM

➢ **Safe statemachines**

- "Safe" directive will only reset the FSM to the reset state when an illegal state is reached. No real implementation of the "others" case.
- An extra FF "illegalpipe" is inserted to recover from illegal states.
- The "others" case is implemented only when the "FSM explorer" is disabled. Needed for hamming 8/4.

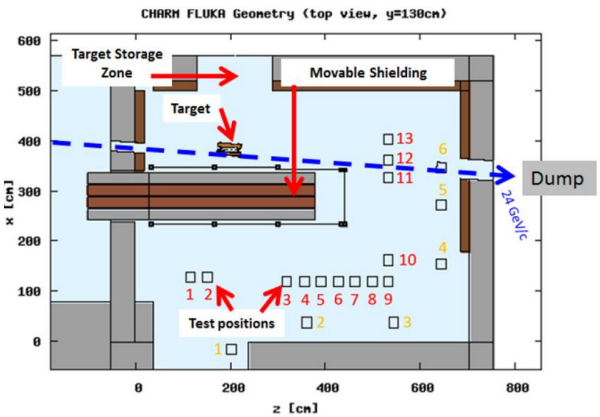


Using the "preserve" directive does not work for the "others"

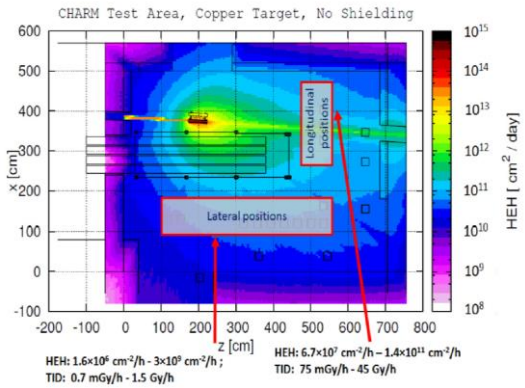
➢ **TMR: Triple Modular Redundancy**

- FFs are triplicated.
- With a single global directive.
- The "illegalpipe" FF (for the "others") was not TMR-ed.

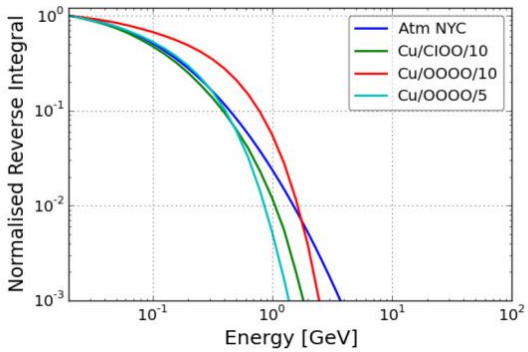
The CHARM radiation facility at CERN



The CHARM layout with test positions



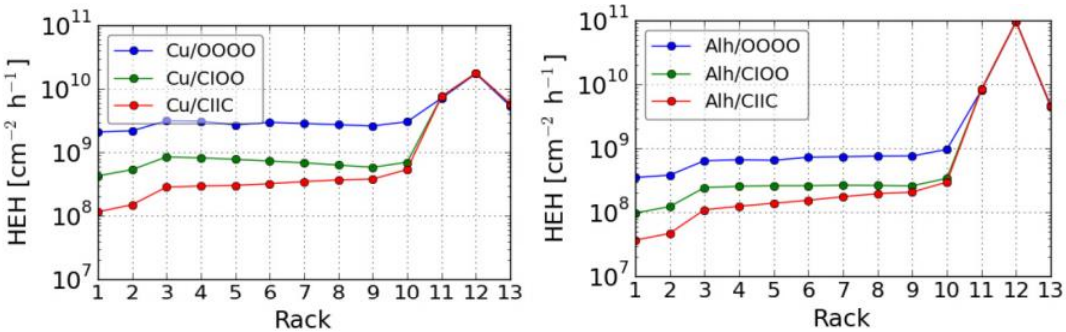
HEH of an example configuration



Test configuration simulating spectra in NYC

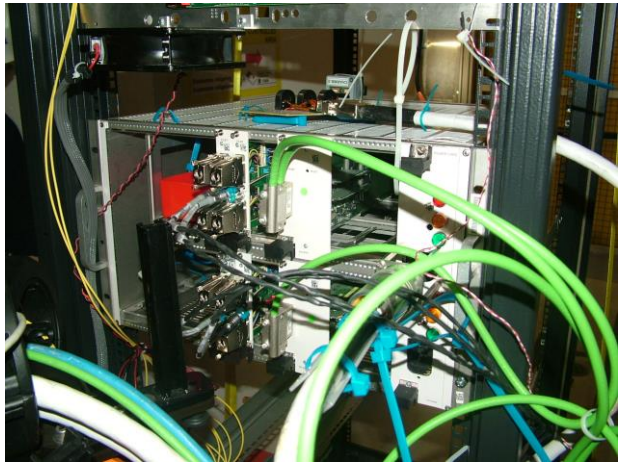
CHARM: Mixed field produced by a 24 GeV/c proton beam and a variety of targets and shield configurations. Can simulate different environments / spectra.

http://ieeexplore.ieee.org/document/7508970/

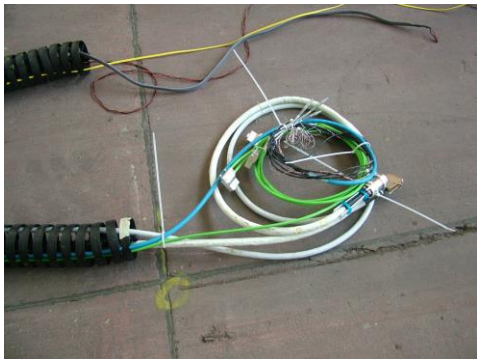


Example of HEH at different test position and configurations

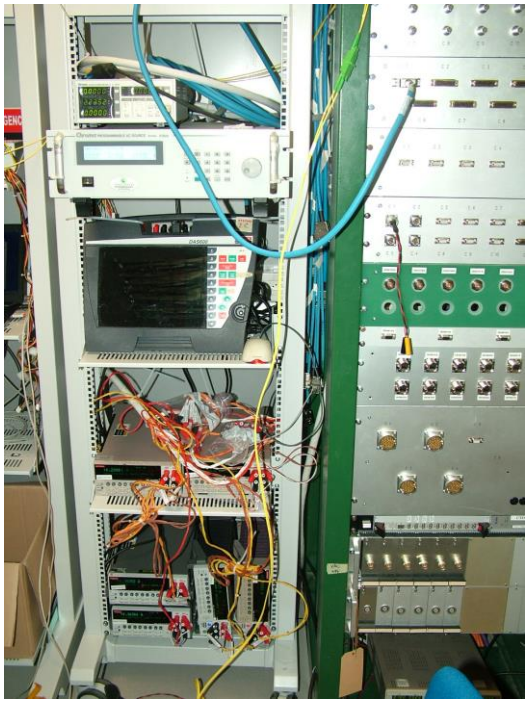
Test preparation at CHARM



Crate with 4 TT and 2 comm cards



Cabling preparation



Control room

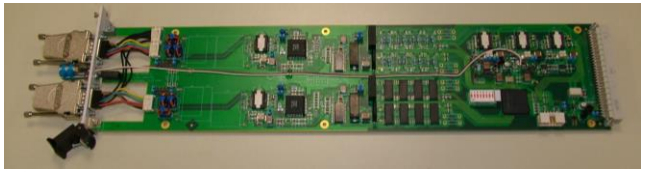
Transportation of crate inside the rad zone

Crate at position 9 (later 13)

Test plan

CHARM Pos	Start date	Stop date	Total dose (Gy)	Total 1-MeVeq Fluence (cm^{-2})	Total HEHeq Fluence (cm^{-2})
9	26/05/2016 16:08:00	01/06/2016 05:59:00	74.04	1.14×10^{12}	3.82×10^{11}
13	01/06/2016 12:47:00	13/06/2016 12:59:00	845.16	6.54×10^{12}	2.65×10^{12}
Total			928.2	7.68×10^{12}	3.03×10^{12}

Crate at position 9 (later at 13)



Prototype double-channel card with Smartfusion2 FPGA

- Rad-hard ref resistors.
- Half channels without digital isolators.

Values tracked:

- Raw data, Data accuracy, diagnostics, SEUs.
- Card power consumption & SEL.
- FPGA core 1.2V supply current.

- At position 13 the rate of ~70 Gy/day was high for the natural annealing rate of the communication card.
- After a dose of ~470 Gy, the communication card was used in intermittent mode (ON/OFF).

TID at failure: Total Integrated Dose

4 FPGA code versions
#1: Safe/Onehot, No TMR
#2: Safe/Onehot, TMR
#3: Hamming 8/4, TMR
#4: Hamming 8/4, TMR with distant FFs

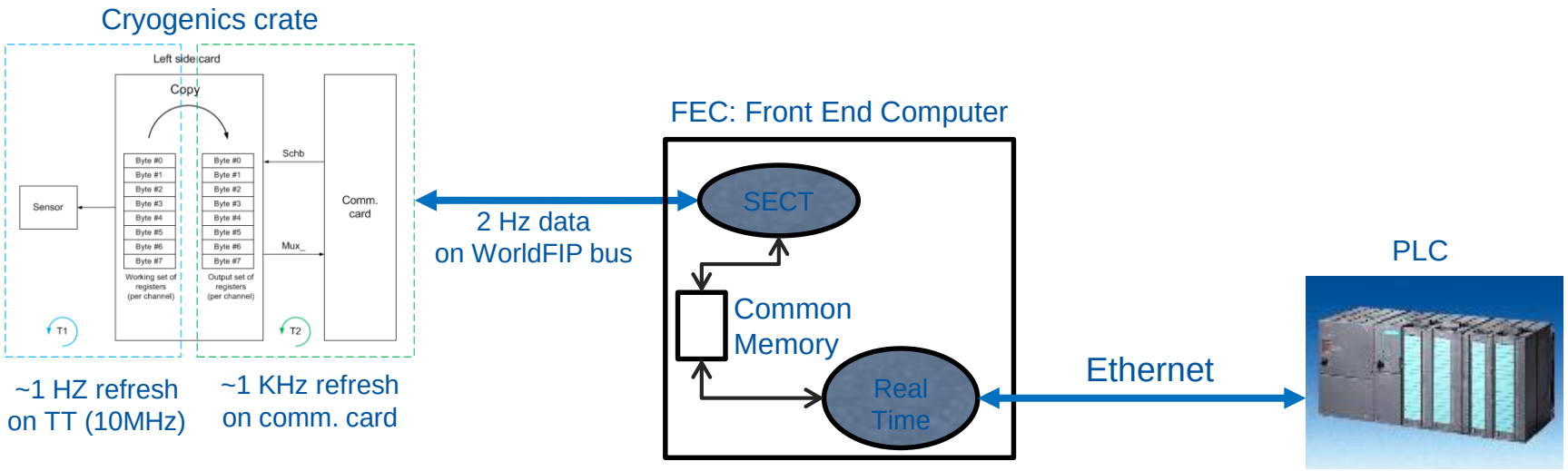
Dose at failure
#1: 725.7 Gy
#2 [749.3 821] Gy
#3: [749.3 821] Gy
#4: 826.1 Gy

After a dose of ~470 Gy communication cards in intermittent mode (ON/OFF)

For externally logged events (e.g. core current)
Dose (Gy), HEHeq Fluence (cm^{-2})
#1: 725.7 Gy, 2.42 x 10^{12} cm^{-2}
#2 [749.3] Gy, 2.5 x 10^{12} cm^{-2}
#3: [749.3] Gy, 2.5 x 10^{12} cm^{-2}
#4: 826.1 Gy, 2.74 x 10^{12} cm^{-2}

For logged events with comm. card (e.g SEU/SET)
Dose (Gy), HEHeq Fluence (cm^{-2})
#1: 725.7 Gy, 1.70 x 10^{12} cm^{-2}
#2 [749.3] Gy, 1.78 x 10^{12} cm^{-2}
#3: [749.3] Gy, 1.78 x 10^{12} cm^{-2}
#4: 749.3+ Gy, 1.78 x 10^{12} cm^{-2}

SEU/SET : Single Event Upset/Transient



4 FPGA code versions

#1: Safe/Onehot, No TMR
#2: Safe/Onehot, TMR
#3: Hamming 8/4, TMR
#4: Hamming 8/4, TMR with distant FFs

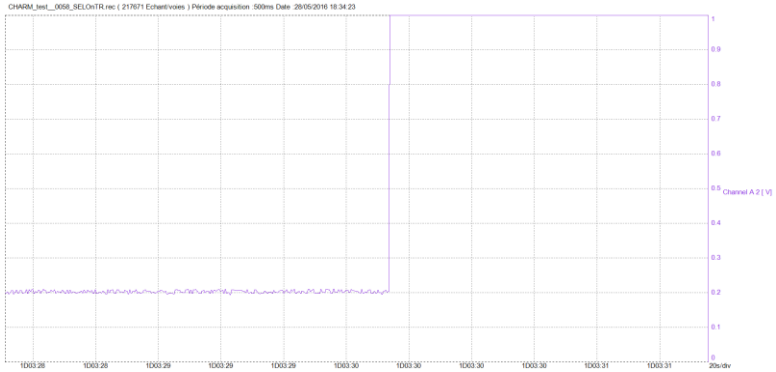
SEU/SET

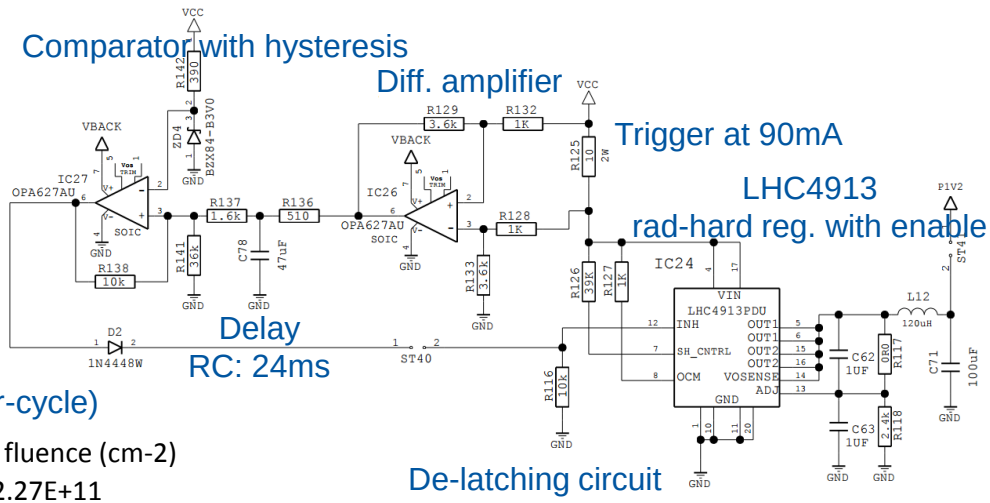
#1 → 4 (3 on single FF, 1 complex on logic)
#2 → 2 (1 reset, 1 at the non-TMRed illegalpipe most-likely)
#3 → 1 (on median logic, diagnostics only, transparent)
#4 → 1 (wdog FSM reset, diagnostics only, transparent)

Cross-sections for SEU

$\sigma_{SEU/SET\#1}$ >2.35 x 10^{-12} cm^2
$\sigma_{SEU/SET\#2}$ >1.12 x 10^{-12} cm^2
$\sigma_{SEU/SET\#3}$ >5.62 x 10^{-13} cm^2
$\sigma_{SEU/SET\#4}$ >5.62 x 10^{-13} cm^2

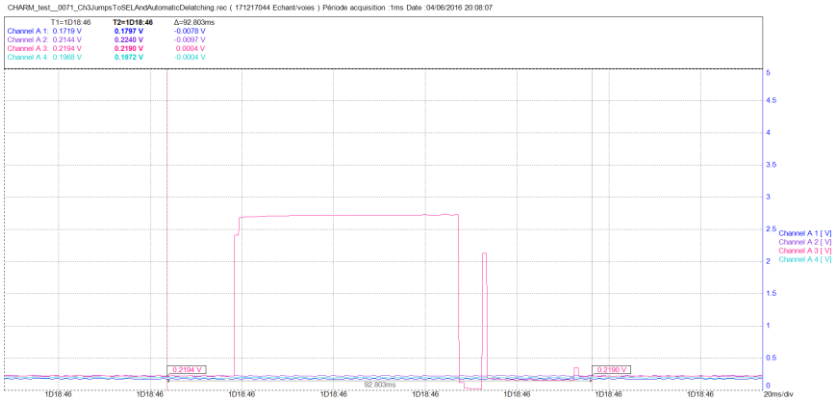
SEL: Single Event Latchup





SEL on DUT #2 de-latching circuit not active (manual power-cycle)

Time (Local)	Dose (Gy)	1-MeV neutron equ. fluence (cm-2)	HEHeq fluence (cm-2)
29/05/2016 21:34	44.01	6.79E+11	2.27E+11



SEL on DUT #3 with de-latching circuit active (recovery as designed)

Time (Local)	Dose (Gy)	1-MeV neutron equ. fluence (cm-2)	HEHeq fluence (cm-2)
06/06/2016 14:25	349.97	3.28E+12	1.247E+12

Cross-sections for SEL

Total HEHeq Fluence: 1.02×10^{13} cm^{-2}

# of events: 2

$\sigma_{SEL} > 1.96 \times 10^{-13}$

Validation of the de-latching circuit.

❖ **Microsemi did not encounter SELs with neutrons.**

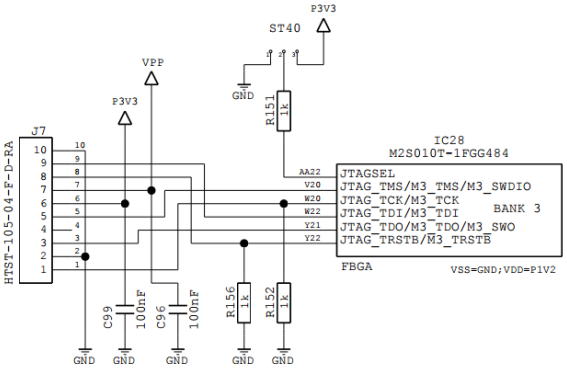
TR0020: SmartFusion2 and IGLOO2 Neutron Single Event Effects (SEE) Test Report

SEU – entering reprogramming state?

Event: The IO configuration of the DUT #1 was lost, all outputs at high-Z.

Time (Local)	Dose (Gy)	1-MeV neutron equ. fluence (cm-2)	HEHeq fluence (cm-2)
06/06/2016 23:23	381.21	3.52E+12	1.345E+12

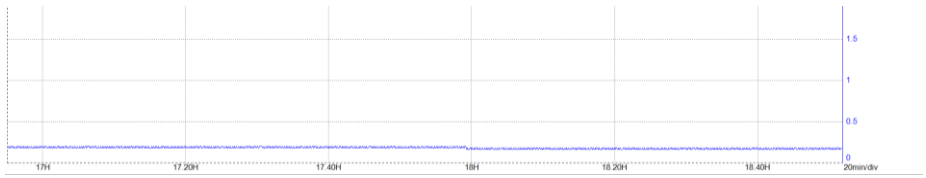
Total HEHeq Fluence: 1.02×10^{13} cm^{-2}
# of events: 1



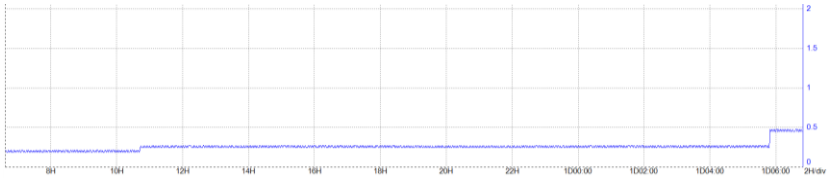
Cross-sections for this SEU event
$\sigma_{SEL} > 0.98 \times 10^{-13}$ cm^2

The PCB was updated to perform an automated power-cycle on this occurrence (by checking the voltage of a pulled-up IO output pin which is set to ‘0’.

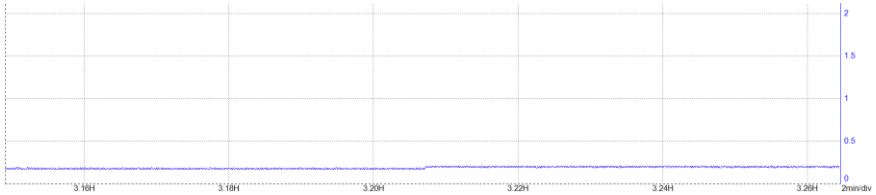
Core supply current events in FPGA #1



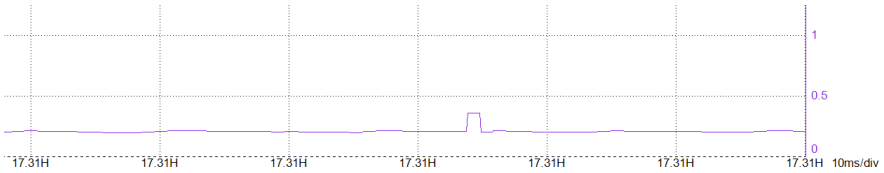
Step from 19mA to 17mA
(FPGA #1, 106.7 Gy)



From 20mA to 24mA in 6 seconds
(FPGA #1, 600.4 Gy)
Step from 26mA to 46mA
(FPGA #1, 700.1 Gy)



Step from 17mA to 19mA
(FPGA #1, 381.2 Gy)



1ms pulse 20mA to 34mA during reset SEU
(FPGA #2, 217.7 Gy)

Conclusions

- Testing at CHARM revealed cross-sections on events such as SEL and “entering programming mode”.
- SETs seem to be latched by FFs; Hamming 8/4 could cope with upsets on FSMs without resetting them.

All observed SEUs and radiation events can be transparent to the cryogenics instrumentation thanks to FPGA software architecture, automated PCB power-cycle and low/high level filtering even when using onehot/safe/non-TMR.

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