GBT-FPGA Tutorial

Informal tutorial: Questions are welcome anytime

Please interrupt !!!
Outline

• What is the GBT-FPGA?
• What is the frame structure?
• What is the relationship between GBT-link and e-links?
• Which FPGAs are supported so far?
• Which Reference board are supported so far?
• What are the typical use cases?
• What is the difference between “standard” and “Latency-optimized”?
• What constraints are required when the GBT-FPGA IP is used?
• Is it easy to switch from single to multiple GBT links?
• How many links have been already fitted in one device?
• Why do we use records in the GBT-FPGA core?
• Is it easy to migrate the GBT-FPGA core to an unsupported FPGA? (MGT core …)
• Why don’t we use the GTX wizard for Xilinx FPGAs?
• How can I check my firmware using the GBT-FPGA?
• What are the first things to check when I am facing problems running the GBT-FPGA?
• What is coming next? What is the plan for new FPGAs families?
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What is the GBT-FPGA?

- Project initiated in 2009
- Gigabit transceiver IP (@4.8Gbs) with encoding
- Targets FPGA from Altera and Xilinx
- Supported by EP-ESE-BE section at CERN
  - Sophie B. and Julian M.
- Available on SVN (latest version: 4.1.0):
  - https://svn.cern.ch/reps/ph-ese/be/GBT_fpga/tags
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What is the frame structure?

• What encoding are supported?
  • GBT: based on Reed-Salomon
    • Includes scrambling and interleaver
    • User data: 84bit
    • Can correct up to 4 consecutive symbols (4bit)
  • WideBus:
    • User data: 112bit
    • No Forward Error Correction (FEC)
    • GBTx: only upstream
    • GBT-FPGA: both direction
What is the frame structure?

“randomization” of the data to ensure a good balance of the signal

Ad-hoc encoding scheme allowing the correction of 2 symbols of 4 bits per encoder

Adding the interleaving allows having up to 16 consecutive bit errors to be decoded
What is the frame structure?

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What is the relationship between GBT-link and e-links?

• GBT-FPGA was made to communicate with a GBTx (front-end)
What is the relationship between GBT-link and e-links?

Group 4

Group 0

80 Mb/s

160 Mb/s

320 Mb/s

28/09/2016

GBT-FPGA Tutorial – TWEPP16 - J. Mendez
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<table>
<thead>
<tr>
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<th>Mode</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacturer</td>
<td>Device</td>
<td>Standard</td>
</tr>
<tr>
<td>Altera</td>
<td>Cyclone V</td>
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<td></td>
<td>Stratix V</td>
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<td></td>
<td><em>Arria V</em></td>
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<td></td>
<td>Arria 10</td>
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<tr>
<td>Xilinx</td>
<td>Virtex 6</td>
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<td>Kintex 7</td>
<td>Yes</td>
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<tr>
<td>Cyclone V GT development kit</td>
<td>Cyclone V</td>
</tr>
<tr>
<td>AMC40</td>
<td>Stratix V</td>
</tr>
<tr>
<td>Altera GX Development kit</td>
<td>Arria 10</td>
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<td>PCIe40</td>
<td>Arria 10</td>
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<td>ML605</td>
<td>Virtex 6</td>
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<td>Glib</td>
<td>Virtex 6</td>
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<td>FC7</td>
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<td>KC705</td>
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<tr>
<td>VC707</td>
<td>Virtex 7</td>
</tr>
<tr>
<td>KCU105</td>
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By default, 1 link per design
Additional reference board as third party designs (branch)
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What are the typical use cases?

• Typical link:
  • GBT-FPGA is used on back-end
  • GBTx is used on front-end

• Downstream: timing and trigger distribution (GBT) – Latency optimized
• Upstream: Data (Widebus or GBT) - Standard
What are the typical use cases?

- **GBTx emulation:**
  - GBT-FPGA is used on back-end
  - GBT-FPGA is used on front-end

- Downstream: timing and trigger distribution (GBT) – Latency optimized
- Upstream: Data (Widebus or GBT) - Standard
What are the typical use cases?

- Others (e.g.: used by accelerator)
  - GBT-FPGA is used on back-end
  - GBTx is used on front-end

- Downstream: Data (GBT) – Latency optimized
- Upstream: Measurement data (GBT or Widebus) – Latency optimized

---

**Diagram:**

- **Back end**
  - Tx: lat-opt
  - Rx: standard
  - GBT-FPGA

- **Front end**
  - Downstream (TX): lat-opt
  - Upstream (RX): lat-opt
  - GBTx
  - No BCID (no collision)
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**GBT BANK**

**Transmitter**
- **Tx PLL**
- **Tx PLL Serial clock**
- **TX_USRCLK**
- **PISO**
- **Barrel Shifter**
- **SIPO**
- **CDR**

**Receiver**
- **Barrel Shifter**
- **SIPO**
- **CDR**
- **RX_RECCLK**
- **RXFRAMECLK**
- **RX_FLAG**
- **RX_USRCLK**

**GBT FRAME**
- **Scrambler**
- **Wide-Bus Encoder**
- **GBT-Frame**
- **Gearbox Phase mon.**
- **Gearbox**
- **Barrel Shifter**
- **Pattern search**
- **BitSlip control**

**TX_FRAMECLK**
- 40MHz
- 240MHz or 120MHz

**GBT_DATA**
- 84bit
- 32bit

**WB_EXTRADATA**
- 32bit

**TX_USRCLK**
- 240MHz or 120MHz

**REFCLK**
- 240MHz or 120MHz

**TX_FRAMECLK**
- 40MHz
- 240MHz or 120MHz

**TX_USRCLK**
- 240MHz or 120MHz

**TX_FLAG**
- 20 or 40 bit

**RX_FLAG**
- 20 or 40 bit

**RX_FRAMECLK gen.**
- 240MHz or 120MHz

**RX_USRCLK**
- 240MHz or 120MHz

**RX_FLAG**
- 20 or 40 bit
What is the difference between “standard” and “Latency-optimized”?

• How to configure the transceiver for the latency-optimized mode?
  
  • **NLDC**: Non Latency Deterministic Components
    • Clock domain crossing shall be made using **register-based** modules.
    • Elastic buffer bypassed thanks to clock domain unification (also used in standard mode to simplify the design).

  • **CFD**: Clock frequency division
    • Rising edge of derived clock may lock onto any of the rising edge of the input clock.

  • **CDR**: Clock and Data recovery
    • Serial clock is **divided** by N to construct the usrclk.
    • Frame aligned using the **Rx slide / Bitslip**
    • Dual data rate implies the recovered clock can latch on both rising and falling edge of the serial clock (controlled with Rx slide / Bitslip).
What is the difference between “standard” and “Latency-optimized”?

- Why is the TX gearbox a special case?
  - DPBC: Deterministic Phase Between Clocks

Use it to scan the sampling window
What is the difference between “standard” and “Latency-optimized”?

• How the RX FrameClk (40MHz) is generated?

- RX Frameclk gen.
  - Phase align.
  - Internal PLL

  240 MHz
  RX_USRCLK

  40MHz
  RX_FRAMECLK

Header sync (from frame aligner)

RX_USRCLK

RX_FRAMECLK

Header sync

OK

X

X

X

X

X

X

X
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- Input clocks must be defined

```tcl
#*****************************************************************************
# Create Clock
#*****************************************************************************
create_clock -period 240MHz [get_ports {REF_CLOCK}]
create_clock -period 100MHz [get_ports {SYS_CLK_100MHz}]
```

- No relation between clocks

```tcl
#*****************************************************************************
# Set Clock Groups
#*****************************************************************************
set_clock_groups -asynchronous -group [get_clocks {REF_CLOCK}]
set_clock_groups -asynchronous -group [get_clocks {SYS_CLK_100MHz}]
set_clock_groups -asynchronous -group [get_clocks {*frameclk_pll_inst*outclk_0}]
set_clock_groups -asynchronous -group [get_clocks {*rxFrmClkPhAligner*outclk0}]
set_clock_groups -asynchronous -group [get_clocks {*rx_pma_clk}]
set_clock_groups -asynchronous -group [get_clocks {*tx_pma_clk}]
```
What constraints are required when the GBT-FPGA IP is used?

- Constraints for latency-optimized mode:

  - TX_FRAMECLK: 40MHz or 240MHz
  - REFCLK: 240MHz or 120MHz
  - TX_USRCLK: Encoder
  - TX_ISDATA_SEL: Scrambler
  - TX_FRAMECLK: 240MHz or 120MHz
  - GBT_DATA: 120bit
  - WB_EXTRADATA: 32bit
  - TX_RECCLK: Pattern search
  - BitSlip control
  - RX_FRAMECLK: 40MHz
  - RX_USRCLK: 240MHz or 120MHz
  - RX_RECCLK: Phase Algnr
What constraints are required when the GBT-FPGA IP is used?

• Scrambler to gearbox maximum delay constraint:

Altera:

```
# Set Maximum Delay
set_max_delay -from [get_registers {gbtExmplDsgn_inst|gbtBank[*]|scrambler[*]}] -to [get_registers {gbtExmplDsgn_inst|gbtBank[*]|txGearbox[*]}] 20.000
```

Xilinx:

```
# Set Maximum Delay
set_max_delay 20 -from [get_pins -hier -filter {NAME =~ */*/rxGearbox/*/C}] -to [get_pins -hier -filter {NAME =~ */*/descrambler/*/D}] -datapath_only
```

```
set_max_delay 20 -from [get_pins -hier -filter {NAME =~ */*/scrambler/*/C}] -to [get_pins -hier -filter {NAME =~ */*/txGearbox/*/D}] -datapath_only
```
What constraints are required when the GBT-FPGA IP is used?

• Critical warning in standard mode for Xilinx FPGA:
  • Module declared in the RX PLL constraint file cannot be found: PLL is included in the project to be compliant with latency optimized mode but not used in standard mode.

Ignore the warning in standard mode
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Is it easy to switch from single to multiple GBT links?

- Modify the GBT_Bank NUM_LINKS parameter value
  - Maximum value depends on the FPGA
  - Several GBT banks can be implemented

- 1 reference clock per bank
  - Typically configurable
  - Internal clock bonding within each bank

- Tx multi-link is usually straight forward
  - no need for specific resources

- Rx multi-link
  - Standard is usually straight forward
  - Latency optimized is more delicate:
    - Ideally one PLL per link for clock recovery would be required due to the phase difference: Lack of PLL resources (Rx Frameclk gen. cannot be shared between links)
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<tbody>
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- Number of bank per FPGA depends on the reference
- A design with 48 links was successfully validated in standard mode for the Arria 10 device (PCIe40)
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• Entity of the generic transceiver instantiation VHDL

```
entity mgt_latopt is
  generic (
    GBT_BANK_ID : integer := 1;
    NUM_LINKS : integer := 1;
    TX_OPTIMIZATION : integer range 0 to 1 := STANDARD;
    RX_OPTIMIZATION : integer range 0 to 1 := STANDARD;
    TX_ENCODING : integer range 0 to 1 := GBT_FRAME;
    RX_ENCODING : integer range 0 to 1 := GBT_FRAME;
  );
  port (  
    MGT_CLKS_I : in gbtBankMgtClks_i_R;
    MGT_CLKS_O : out gbtBankMgtClks_o_R;
  );
end entity;
```

```
type mgtCommon_i_R is
  record
    reconfReset : std_logic;
    reconf_clk : std_logic;
    reconf_avmm_addr : std_logic_vector(12 downto 0);
    reconf_avmm_read : std_logic;
    reconf_avmm_write : std_logic;
    reconf_avmm_writedata : std_logic_vector(31 downto 0);
  end record;

type mgtCommon_o_R is
  record
    reconfAvmmRead_0 : std_logic;
    reconfAvmmRead_1 : std_logic;
    reconfAvmmWaitRequest : std_logic;
  end record;
```

```
type mgt_i_R is
  record
    mgtCommon : mgtCommon_i_R;
    mgtLink : mgtLink_i_R(1 to MAX_NUMGBT_LINK);
  end record;

type mgt_o_R is
  record
    mgtCommon : mgtCommon_o_R;
    mgtLink : mgtLink_o_R(1 to MAX_NUMGBT_LINK);
  end record;
```

```
alt_ax_gbt_bank_package.vhd
```

```
alt_ax_gbt_bank_package.vhd
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gbt_bank_package.vhd
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gbt_bank_package.vhd
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Why do we use records in the GBT-FPGA core?

Xilinx Kintex 7 package (xlx_k7v7_gbt_bank_package.vhd)

```vhdl
type mgtlink_i_R is record
  rx_p : std_logic;
  rx_n : std_logic;
end record;
```

```vhdl
loopBack : std_logic_vector(2 downto 0);
```

```vhdl
tx_reset : std_logic;
rx_reset : std_logic;
```

```vhdl
rxBitSlip_enable : std_logic;
rxBitSlip_ctrl : std_logic;
rxBitSlip_nbr : std_logic_vector(GBTRX_BITSLIP_NBR_MSB downto 0);
rxBitSlip_run : std_logic;
rxBitSlip_oddRstEn : std_logic;
```

```vhdl
conf_diffCtrl : std_logic_vector(3 downto 0);
conf_postCursor : std_logic_vector(4 downto 0);
conf_preCursor : std_logic_vector(4 downto 0);
conf_txCtx : std_logic;
conf_rxCtx : std_logic;
```

```vhdl
drp_addr : std_logic_vector(8 downto 0);
drp_en : std_logic;
drp_di : std_logic_vector(15 downto 0);
drp_we : std_logic;
```

```vhdl
prbs_rxs : std_logic_vector(2 downto 0);
prbs_rxsSel : std_logic_vector(2 downto 0);
prbs_txForceErr : std_logic;
prbs_rxCntReset : std_logic;
end record;
```

Altera Arria 10 package (alt_a10_gbt_bank_package.vhd)

```vhdl
type mgtlink_i_R is record
  tx_reset : std_logic;
  rx_reset : std_logic;
end record;
```

```vhdl
loopBack : std_logic;
```

```vhdl
tx_polarity : std_logic;
rx_polarity : std_logic;
```

```vhdl
rxBitSlip_enable : std_logic;
rxBitSlip_ctrl : std_logic;
rxBitSlip_nbr : std_logic_vector(GBTRX_BITSLIP_NBR_MSB downto 0);
rxBitSlip_run : std_logic;
rxBitSlip_oddRstEn : std_logic;
end record;
```
Outline

• What is the GBT-FPGA?
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• What is the difference between “standard” and “Latency-optimized”?
• What constraints are required when the GBT-FPGA IP is used?
• Is it easy to switch from single to multiple GBT links?
• How many links have been already fitted in one device?
• Why do we use records in the GBT-FPGA core?
• *Is it easy to migrate the GBT-FPGA core to an unsupported FPGA? (MGT core ...)*
• Why don’t we use the GTX wizard for Xilinx FPGAs?
• How can I check my firmware using the GBT-FPGA?
• What are the first things to check when I am facing problems running the GBT-FPGA?
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Is it easy to migrate the GBT-FPGA core to an unsupported FPGA? (MGT core ...)

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**Top level**
- Clocks
- Reset
- Data
- Ctrl
- Status

**Device top**
- Gbt_bank
  - CLKS_I/O
  - GBT_TX_I/O
  - MGT_I/O
  - GBT_RX_I/O

**Gbtx**
- Gbt_tx
  - Data
  - Ctrl status
  - Gearbox
    - gbt_tx_gearbox_latopt
    - gbt_tx_gearbox_std

**Gbtx**
- Gbt_rx
  - Frame aligner
  - Gearbox
  - Decoder
  - Descrambler

**Multigigabit transceivers**
- multi_gigabit_transceivers
  - Ctrl status
  - Data

**Mgt std**
- Mgt_std
  - IPs
  - gbt_tx_gearbox_latopt
  - gbt_tx_gearbox_std

**Mgt latopt**
- Mgt_latopt
  - IPs
  - mgt_latopt_bitslipctrl

---

28/09/2016
Is it easy to migrate the GBT-FPGA core to an unsupported FPGA? (MGT core ...)

- Creation of the device specific top level
- Creation of the vendor_specific_package
  - Record definition
- Creation of the transceiver IP
  - Special care is required for latency optimized
- Creation of the dual ram memory IP
  - Used by the gearbox in std mode
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Why don’t we use the GTX wizard for Xilinx FPGAs?

• In Xilinx, 2 RX slide modes exist:
  • PCS: Data are shifted
  • PMA: Rx clock and data are shifted (required for latency-optimized mode)
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How can I check my firmware using the GBT-FPGA?

- Altera devices:
  - ISSP and SignalTap

ISSP configuration for Arria 10 design

SignalTap for Arria 10 development kit design
How can I check my firmware using the GBT-FPGA?

- Xilinx devices:
  - VIO and ILA

VIO for Kintex Ultrascale KCU105 design

ILA for Kintex Ultrascale KCU105 design
How can I check my firmware using the GBT-FPGA?

- Using VLDB or custom board implementing a GBTx

TWEPP 2016 [Poster H7, from Raul Martin Lesma] : The Versatile Link Board
How can I check my firmware using the GBT-FPGA?

• Configure the GBTx:
  • Tool and minimal config: https://espace.cern.ch/GBT-Project/VLDB/Control/Forms/AllItems.aspx
  • Tutorials: https://cds.cern.ch/collection/E-learning_modules
  • Tool made by Pedro Leitao
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What are the first things to check when I am facing problems running the GBT-FPGA?

• Standard:
  • All the resets must be OFF (Active High)
  • All ready signals must be ON (Active High)
  • Fix bitslip

• Latency optimized:
  • Tx_gearboxAligned (signalTap / ILA): Shift the TX PLL until gearbox phases are aligned (recommended to perform a scan)
What are the first things to check when I am facing problems running the GBT-FPGA?

• Standard:
  • GBTx must be configured
  • TX/RX polarity (GBTx serdes cannot lock when wrong polarity)
    • SFP and VTRx: inverted RX diff. pairs.

• Latency optimized:
  • TX Gearbox is aligned (phase alignment via the flag)
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What is coming next? What is the plan for new FPGAs families?

• SCA/IC : Slow control for GBT
• Testbench: simulation of the GBT and the slow control
• New FPGAs: Arria V and Virtex Ultrascale (and microsemi?)
• LpGBT

• Contributions from you are welcome

Thank you
GBT-FPGA-Support <gbt-fpga-support@cern.ch>
What is the relationship between GBT-link and e-links?

- Downstream Elink mode «x2» (80Mb/s)
What is the relationship between GBT-link and e-links?

• Downstream Elink mode «x4» (160Mb/s)

20 serial links @ 160Mbps

20 «elinks» packets of 4 bits on each 120bits frame @ 40MHz + 1 slow control link
What is the relationship between GBT-link and e-links?

- Downstream Elink mode «x4» (320Mb/s)

10 serial links @ 320Mbps

10 «elinks» packets of 8 bits on each 120bits frame @ 40MHz + 1 slow control link
Why do we use records in the GBT-FPGA core?

• What are the GBT Bank interfaces?

---

**Warning:** configuration can be made using two different ways! Do not mix these to avoid bugs.

**First way:** Specify only the GBT_BANK_ID parameters when you implement the module. In this case, the information are get from the `gbt_banks_user_setup` package (gbt_bank/your_device/xxx_xxx_gbt_bank_user_setup.vhd)

**Second way:** Specify all the parameters except the GBT_BANK_ID (its value shall be 0, default value).
Why do we use records in the GBT-FPGA core?

• How to find records definition?
  • GBT-FPGA User guide
    • 2.5. Operating the GBT-FPGA Core

• VHDL files
  • gbt_bank/core_sources/gbt_bank_package.vhd: records generic for all the devices
  • gbt_bank/<device>/xxx_xxx_gbt_bank_package.vhd: device specific records
Why do we use records in the GBT-FPGA core?

- **Transceiver IP for Altera Arria 10**

```vhdl
gxLatopt_xS: entity gx_latopt_xi.gx_latopt_xi
port map(
    -- Reconfigurator avalon MM bus
    reconfig_write(0),
    reconfig_read(0),
    reconfig_address,
    reconfig_writedata,
    reconfig_readdata,
    reconfig_waitrequest(0),
    reconfig_clk(0),
    reconfig_reset(0)
    ...
```  

- **Transceiver IP for Xilinx Kintex Ultrascale**

```vhdl
xlx_ku_mgt_std_i: xlx_ku_mgt_ip
PORT MAP (  
drpaddr_in,
    drpclk_in(0),
    drpd_in,
    drpen_in(0),
    drpwe_in(0),
    drpdo_out,
    drpdy_out(0)
    ...
```