GBT-FPGA Tutorial

FPGA Working group – TWEPP 2016

Informal tutorial:

Questions are welcome anytime

Please interrupt !!!

Outline

- What is the GBT-FPGA?
- What is the frame structure?
- What is the relationship between GBT-link and e-links?
- Which FPGAs are supported so far?
- Which Reference board are supported so far?
- What are the typical use cases ?
- What is the difference between “standard” and “Latency-optimized”?
- What constraints are required when the GBT-FPGA IP is used?
- Is it easy to switch from single to multiple GBT links?
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- Is it easy to migrate the GBT-FPGA core to an unsupported FPGA? (MGT core …)
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- How can I check my firmware using the GBT-FPGA?
- What are the first things to check when I am facing problems running the GBT-FPGA?
- What is coming next? What is the plan for new FPGAs families?

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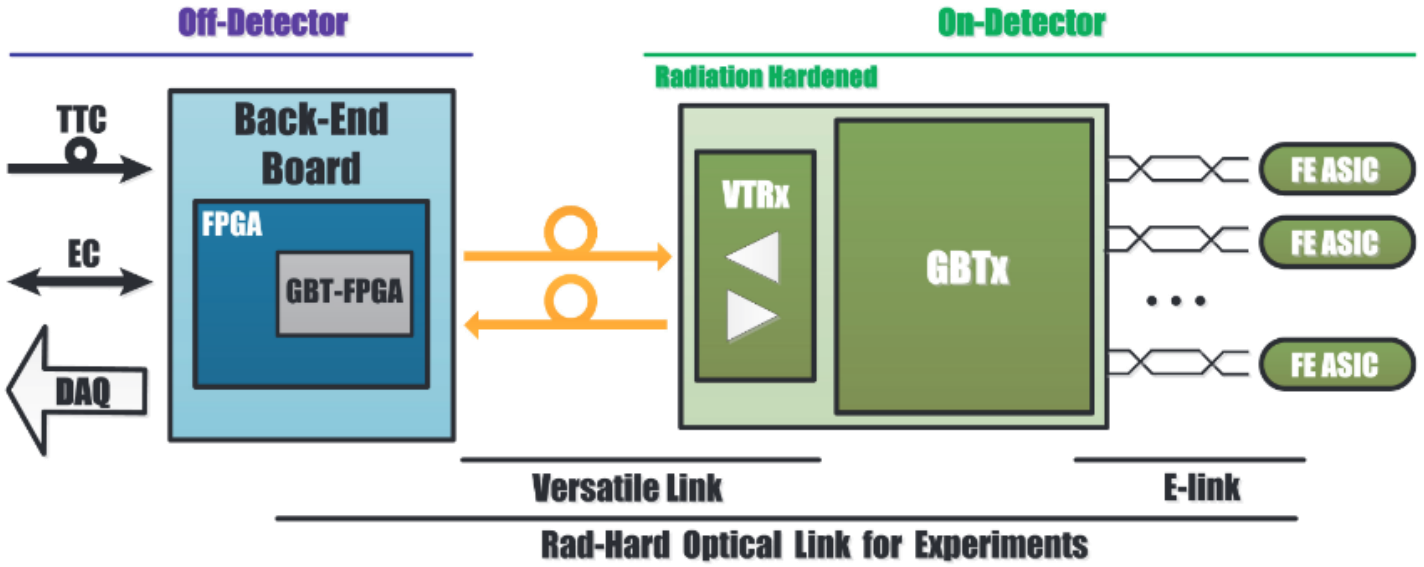
What is the GBT-FPGA?

- Project initiated in 2009
- Gigabit transceiver IP (@4.8Gbs) with encoding
- Targets FPGA from Altera and Xilinx
- Supported by EP-ESE-BE section at CERN
  - Sophie B. and Julian M.
- Available on SVN (latest version: 4.1.0):
  - https://svn.cern.ch/reps/ph-ese/be/gbt_fpga/tags



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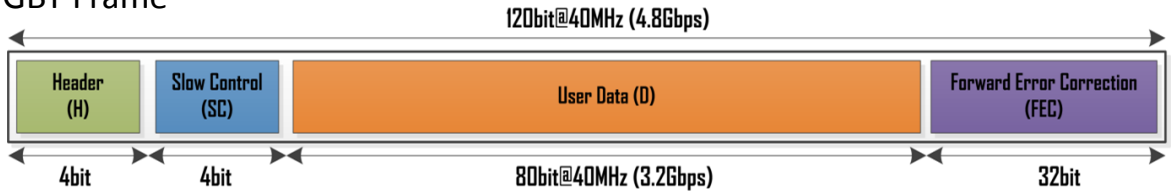
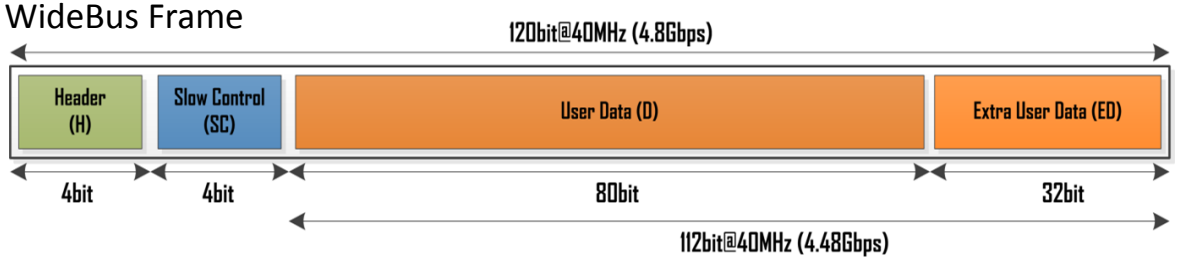
What is the frame structure?

- What encoding are supported ?
  - GBT: based on Reed-Salomon
    - Includes scrambling and interleaver
    - User data: 84bit
    - Can correct up to 4 consecutive symbols (4bit)
  - WideBus:
    - User data: 112bit
    - No Forward Error Correction (FEC)
    - GBTx: only upstream
    - GBT-FPGA: both direction

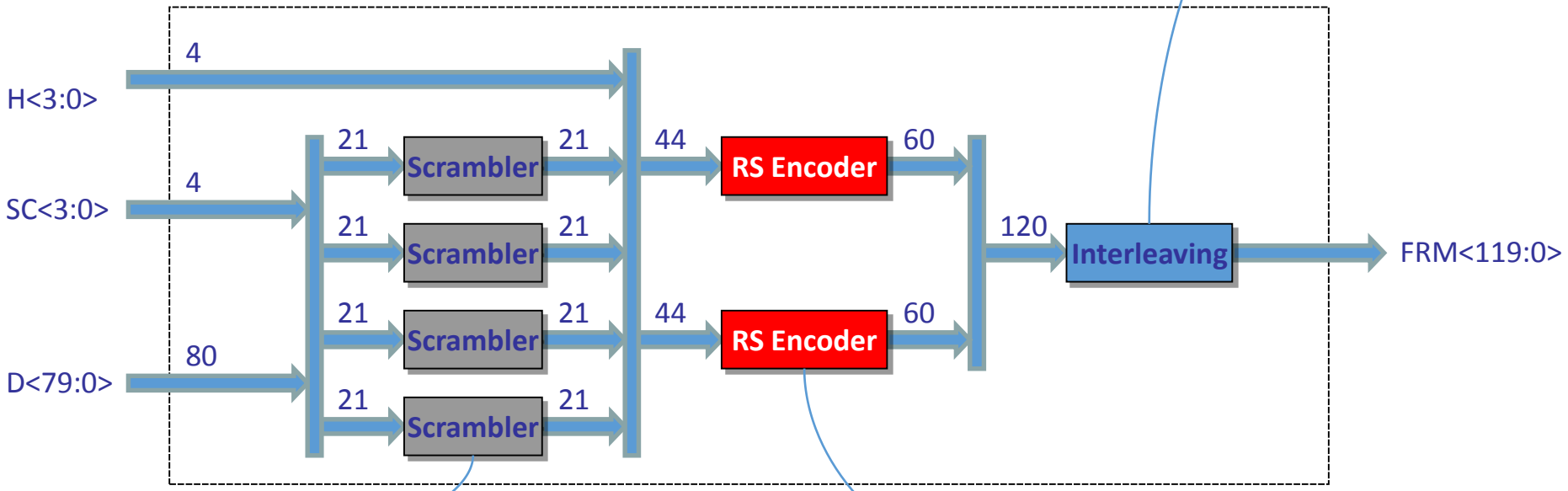
GBT Frame



WideBus Frame



What is the frame structure?

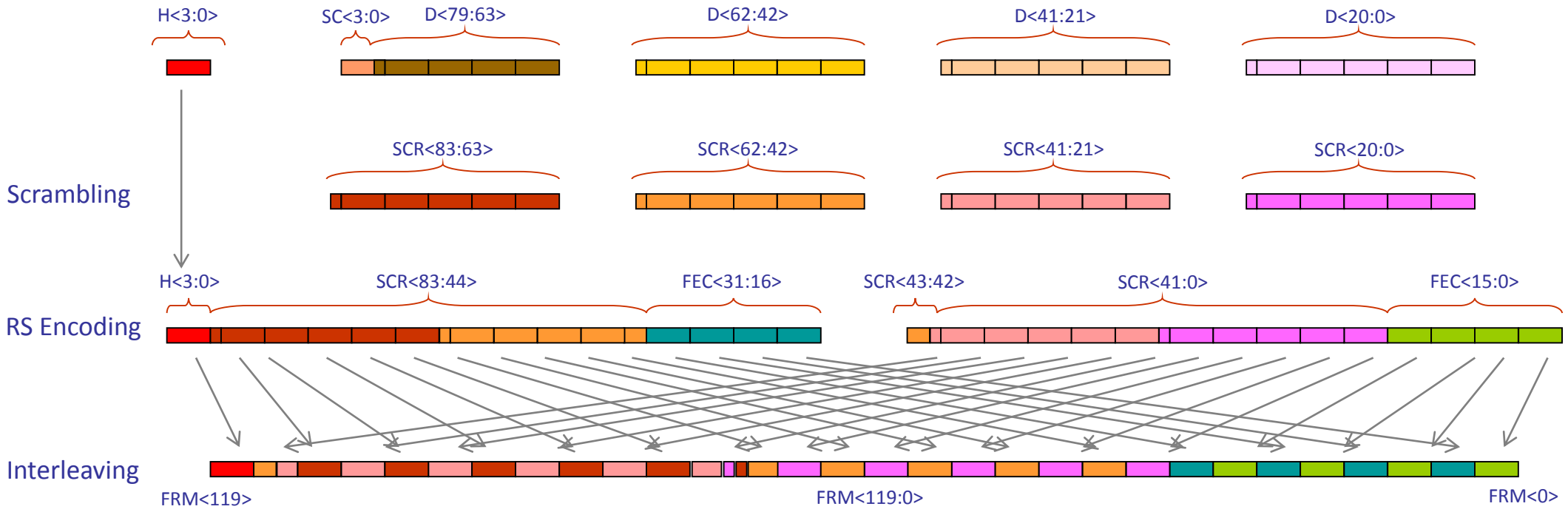


Adding the interleaving allows having up to 16 consecutive bit errors to be decoded

"randomization" of the data to ensure a good balance of the signal

Ad-hoc encoding scheme allowing the correction of 2 symbols of 4 bits per encoder

What is the frame structure?



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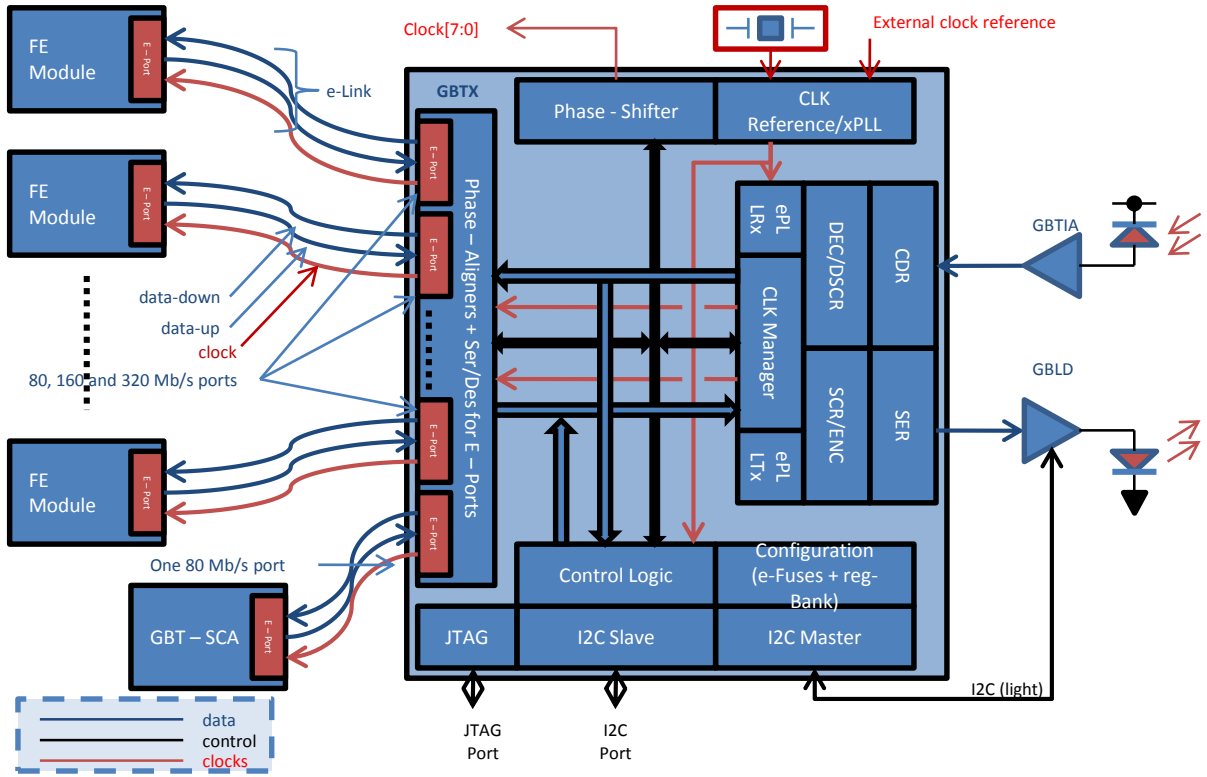
What is the relationship between GBT-link and e-links?

- GBT-FPGA was made to communicate with a GBTx (front-end)



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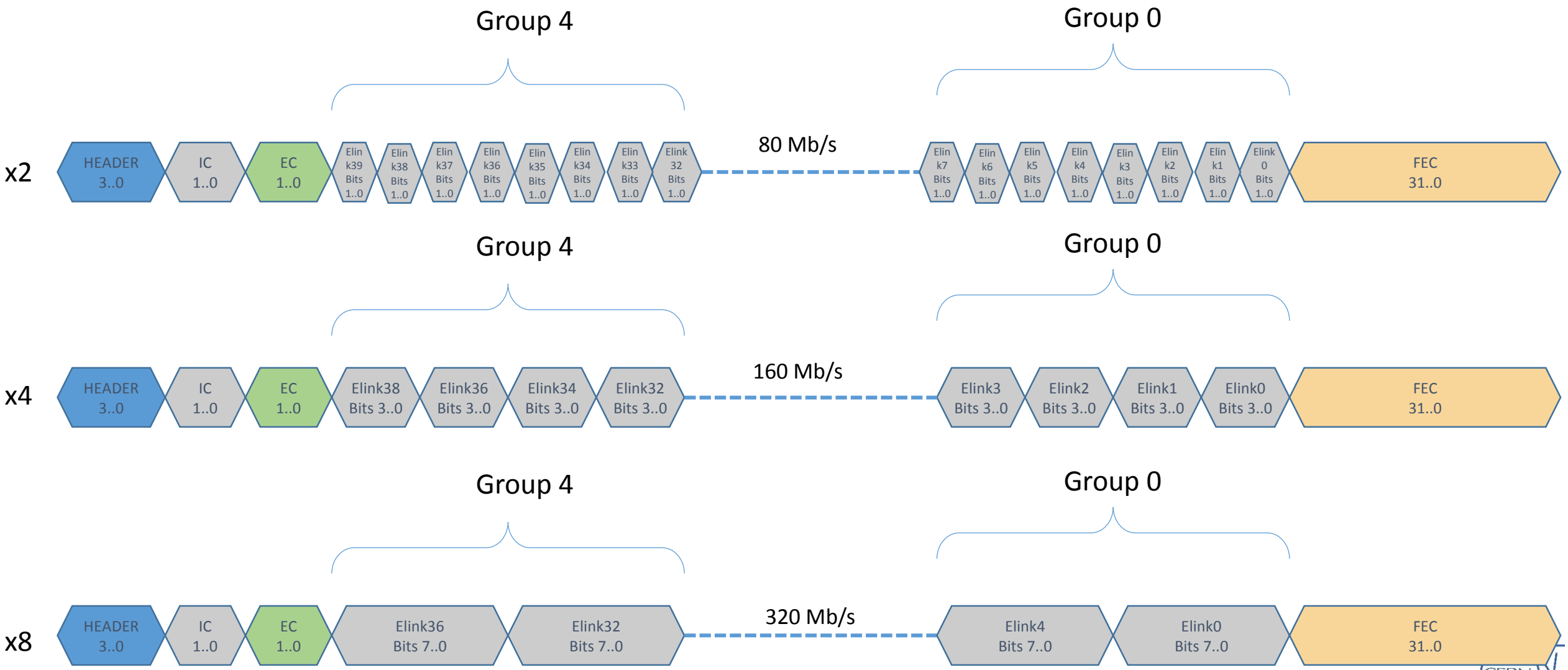

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Which FPGAs are supported so far?

FPGA		Mode		Encoding	
Manufacturer	**Device**	**Standard**	**Lat-optimized**	**GBT**	**WideBus**
Altera	Cyclone V	**Yes**	**No**	Tx/Rx	**Tx**/Rx
	Stratix V	**Yes**	**Yes**	Tx/Rx	**Tx**/Rx
	Arria V	*Yes*	*Yes*	*Tx/Rx*	***Tx**/Rx*
	Arria 10	**Yes**	**Yes**	Tx/Rx	**Tx**/Rx
Xilinx	Virtex 6	**Yes**	**Yes**	Tx/Rx	**Tx**/Rx
	Virtex 7	**Yes**	**Yes**	Tx/Rx	**Tx**/Rx
	Kintex 7	**Yes**	**Yes**	Tx/Rx	**Tx**/Rx
	Kintex Ultrascale	**Yes**	**Yes**	Tx/Rx	**Tx**/Rx

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Which Reference boards are supported so far?

	Reference	Device
Altera	Cyclone V GT development kit	Cyclone V
	AMC40	Stratix V
	Altera GX Development kit	Arria 10
	PCIe40	Arria 10
Xilinx	ML605	Virtex 6
	Glib	Virtex 6
	FC7	Kintex 7
	KC705	Kintex 7
	VC707	Virtex 7
	KCU105	Kintex Ultrascale

By default, 1 link per design

Additional reference board as third party designs (branch)

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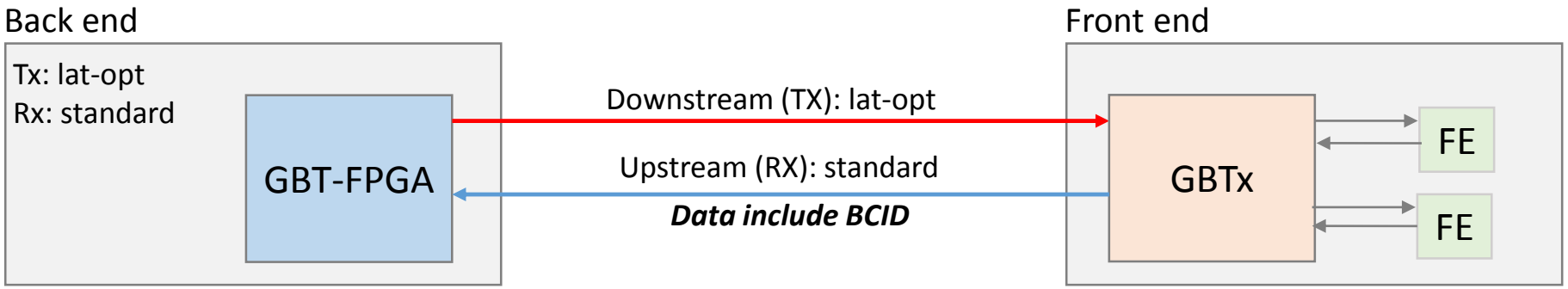
What are the typical use cases ?

- Typical link:
  - GBT-FPGA is used on back-end
  - GBTx is used on front-end

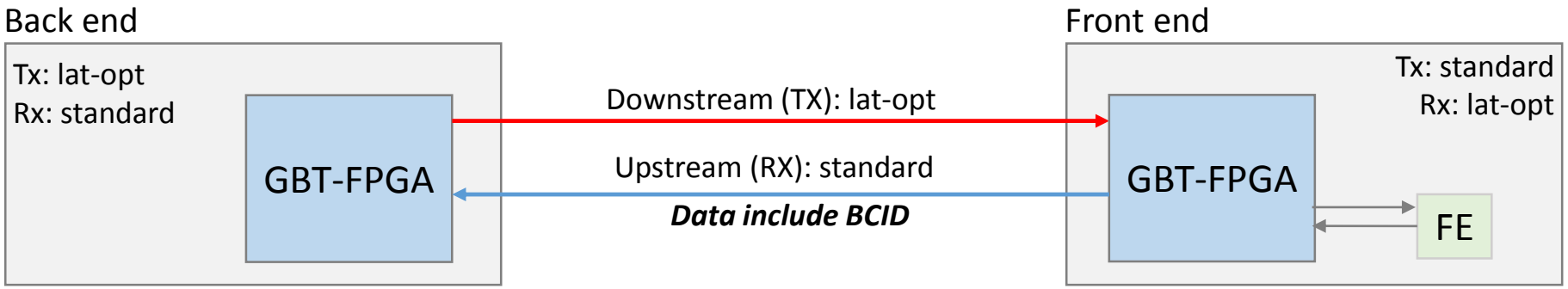
  - Downstream: timing and trigger distribution (GBT) – Latency optimized
  - Upstream: Data (Widebus or GBT) - Standard



What are the typical use cases ?

- GBTx emulation:
  - GBT-FPGA is used on back-end
  - GBT-FPGA is used on front-end

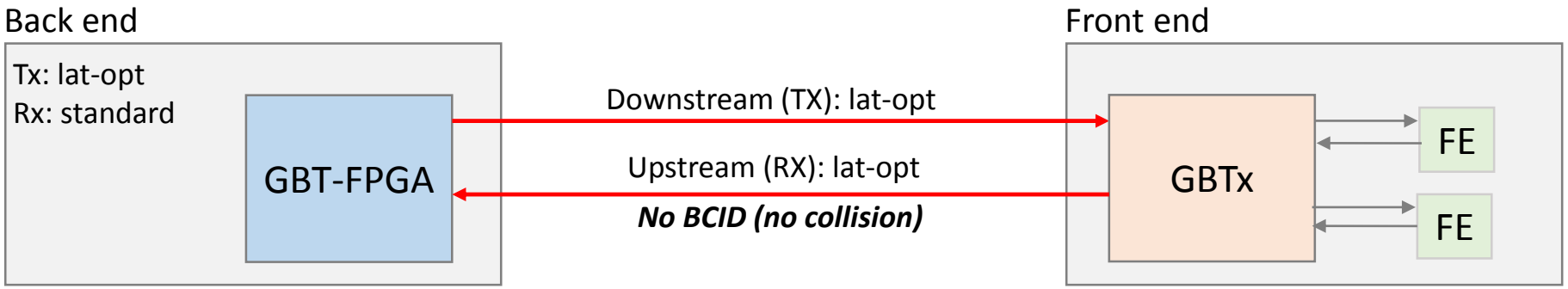
  - Downstream: timing and trigger distribution (GBT) – Latency optimized
  - Upstream: Data (Widebus or GBT) - Standard



What are the typical use cases ?

- Others (e.g.: used by accelerator)
  - GBT-FPGA is used on back-end
  - GBTx is used on front-end

  - Downstream: Data (GBT) – Latency optimized
  - Upstream: Measurement data (GBT or Widebus) – Latency optimized



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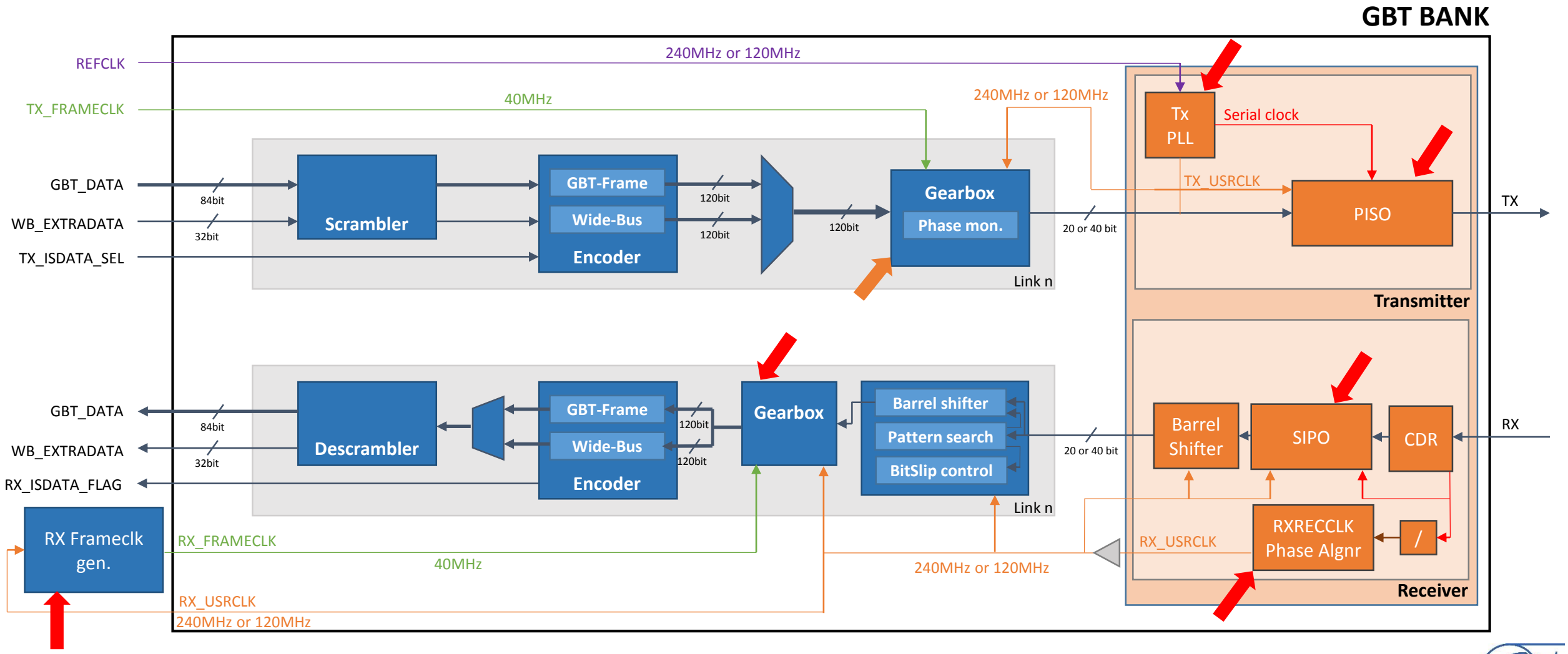
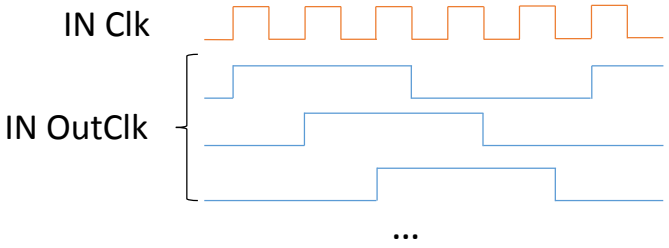


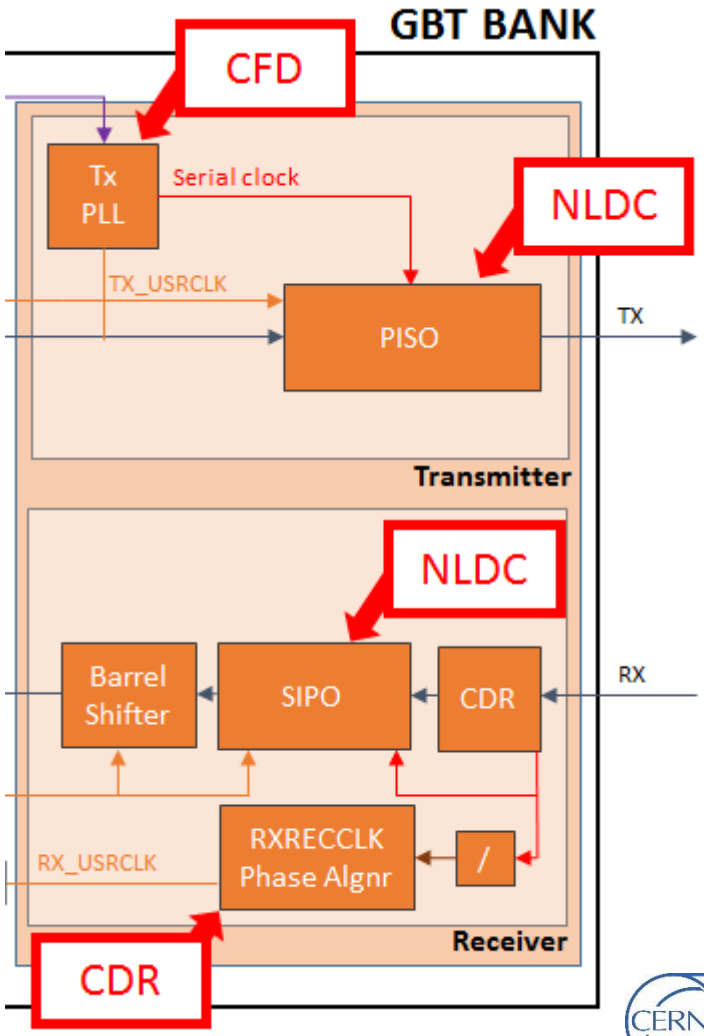
What is the difference between “standard” and “Latency-optimized”?

- How to configure the transceiver for the latency-optimized mode?
  - **NLDC**: Non Latency Deterministic Components
    - Clock domain crossing shall be made using **register-based** modules.
    - **Elastic buffer** bypassed thanks to clock domain unification (also used in standard mode to simplify the design).
  - **CFD**: Clock frequency division
    - Rising edge of derived clock may lock onto any of the rising edge of the input clock.



Managed by the Tx PLL

  - **CDR**: Clock and Data recovery
    - Serial clock is **divided** by N to construct the usrclk.
    - Frame aligned using the **Rx slide / Bitslip**
    - **Dual data rate** implies the recovered clock can latch on both rising and falling edge of the serial clock (controlled with Rx slide / Bitslip).



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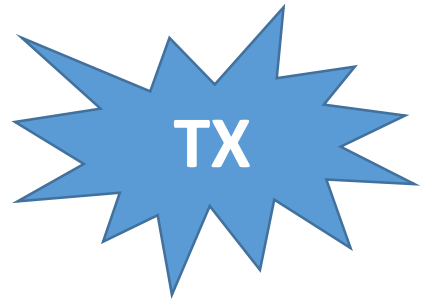
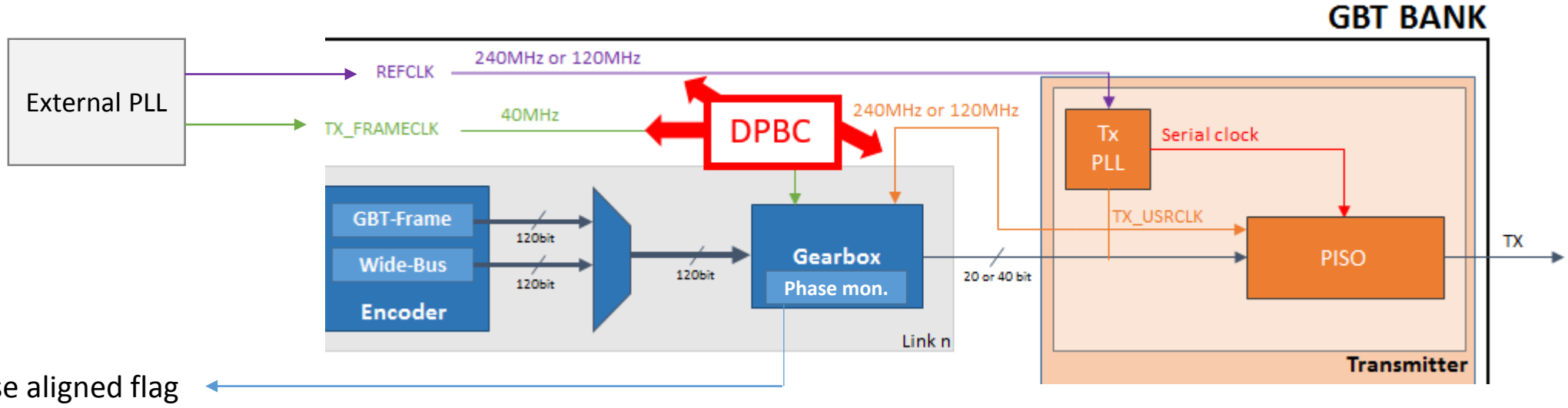


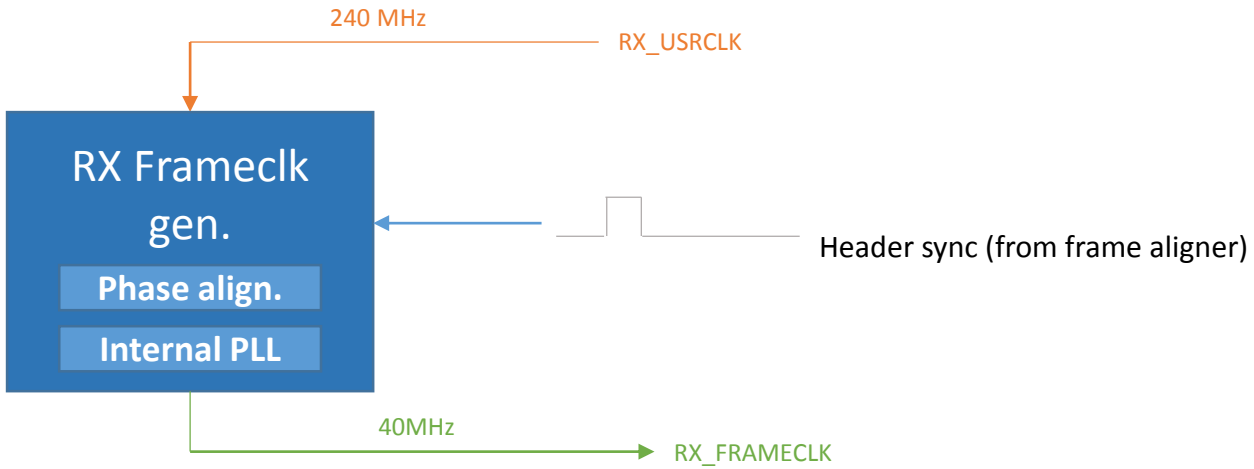
- Why is the TX gearbox a special case?
  - DPBC: Deterministic Phase Between Clocks

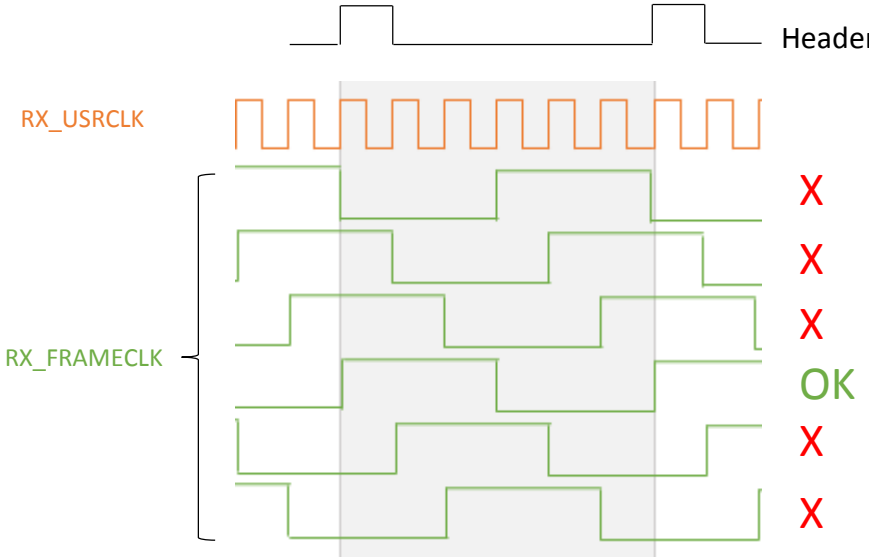


Use it to scan the sampling window

What is the difference between “standard” and “Latency-optimized”?

- How the RX FrameClk (40MHz) is generated?





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What constraints are required when the GBT-FPGA IP is used?

- Input clocks must be defined

```
#**************************************************************
# Create Clock
#**************************************************************

create_clock -period 240MHz [get_ports {REF_CLOCK}]
create_clock -period 100MHz [get_ports {SYS_CLK_100MHz}]
```

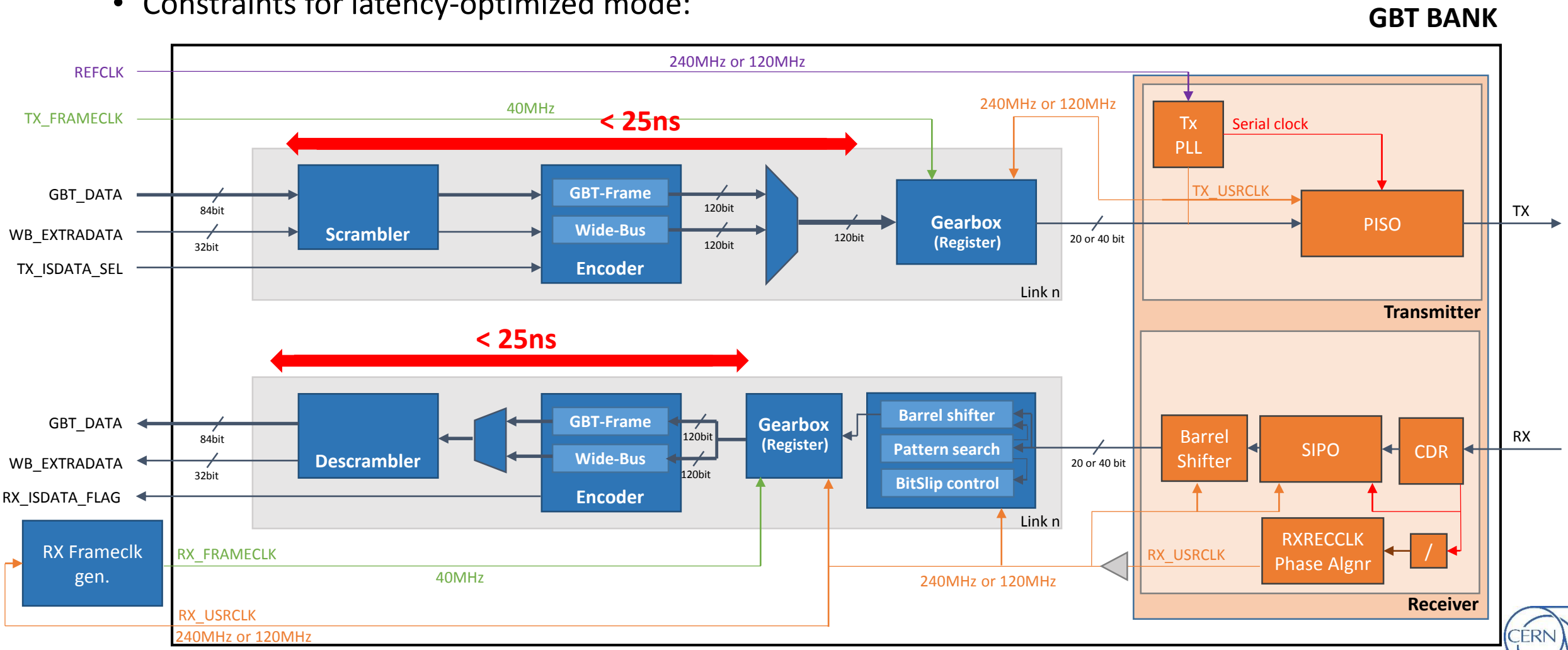
- No relation between clocks

```
#**************************************************************
# Set Clock Groups
#**************************************************************

set_clock_groups -asynchronous -group [get_clocks {REF_CLOCK}]
set_clock_groups -asynchronous -group [get_clocks {SYS_CLK_100MHz}]
set_clock_groups -asynchronous -group [get_clocks {*frameclk_pll_inst*outclk_0}]
set_clock_groups -asynchronous -group [get_clocks {*rxFrmClkPhAlgnr*outclk0}]
set_clock_groups -asynchronous -group [get_clocks {*rx_pma_clk}]
set_clock_groups -asynchronous -group [get_clocks {*tx_pma_clk}]
```

What constraints are required when the GBT-FPGA IP is used?

- Constraints for latency-optimized mode:



What constraints are required when the GBT-FPGA IP is used?

- Scrambler to gearbox maximum delay constraint:

Altera:

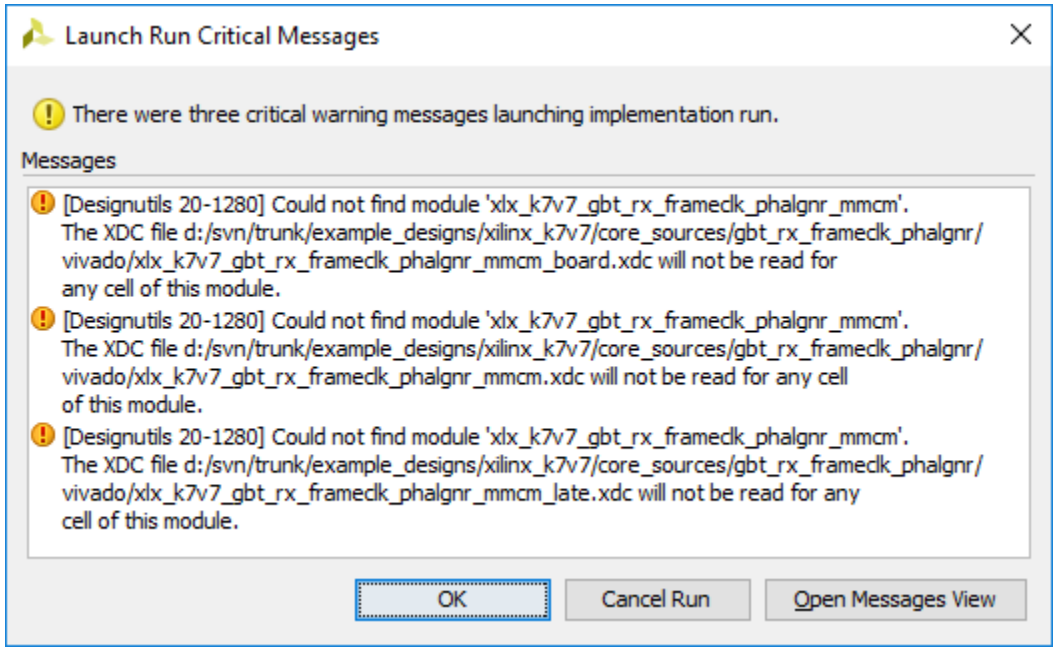
```
#**************************************************************
# Set Maximum Delay
#**************************************************************
set_max_delay -from [get_registers {gbtExmplDsgn_inst|gbtBank|*|scrambler|*}] -to [get_registers {gbtExmplDsgn_inst|gbtBank|*|txGearbox|*}] 20.000
set_max_delay -from [get_registers {gbtExmplDsgn_inst|gbtBank|*|rxGearbox|*}] -to [get_registers {gbtExmplDsgn_inst|gbtBank|*|descrambler|*}] 20.000
```

Xilinx:

```
#**************************************************************
# Set Maximum Delay
#**************************************************************
set_max_delay 20 -from [get_pins -hier -filter {NAME =~ */*/*/rxGearbox/*/C}] -to [get_pins -hier -filter {NAME =~ */*/*/descrambler/*/D}] -datapath_only
set_max_delay 20 -from [get_pins -hier -filter {NAME =~ */*/*/scrambler/*/C}] -to [get_pins -hier -filter {NAME =~ */*/*/txGearbox/*/D}] -datapath_only
```

What constraints are required when the GBT-FPGA IP is used?

- Critical warning in standard mode for Xilinx FPGA:
  - Module declared in the RX PLL constraint file cannot be found: PLL is included in the project to be compliant with latency optimized mode but not used in standard mode.



Ignore the warning in standard mode

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Is it easy to switch from single to multiple GBT links?

- Modify the GBT_Bank NUM_LINKS parameter value
  - Maximum value depends on the FPGA
  - Several GBT banks can be implemented
- 1 reference clock per bank
  - Typically configurable
  - Internal clock bonding within each bank
- Tx multi-link is usually straight forward
  - no need for specific resources
- Rx multi-link
  - Standard is usually straight forward
  - Latency optimized is more delicate:
    - Ideally one PLL per link for clock recovery would be required due to the phase difference: Lack of PLL resources (Rx Frameclk gen. cannot be shared between links)

```
--=============--
-- GBT Bank    --
--=============--
gbtBank: entity work.gbt_bank
    generic map (
        NUM_LINKS                       => 6,
        TX_OPTIMIZATION                 => STANDARD,
        RX_OPTIMIZATION                 => STANDARD,
        TX_ENCODING                     => GBT_FRAME,
        RX_ENCODING                     => GBT_FRAME
    )
    port map (
        CLKS_I                          => to_gbtBank_clks,
        CLKS_O                          => from_gbtBank_clks,
        ------------------------------------------------
        GBT_TX_I                        => to_gbtBank_gbtTx,
        GBT_TX_O                        => from_gbtBank_gbtTx,
        ------------------------------------------------
        MGT_I                           => to_gbtBank_mgt,
        MGT_O                           => from_gbtBank_mgt,
        ------------------------------------------------
        GBT_RX_I                        => to_gbtBank_gbtRx,
        GBT_RX_O                        => from_gbtBank_gbtRx
    );
```

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How many links have been already fitted in one device?

FPGA		Bank
Manufacturer	**Device**	**Max. of links / bank**
Altera	Cyclone V	3 links
	Stratix V	6 links
	Arria V	*6* links
	Arria 10	6 links
Xilinx	Virtex 6	4 links
	Virtex 7	4 links
	Kintex 7	4 links
	Kintex Ultrascale	4 links

- Number of bank per FPGA depends on the reference
- A design with 48 links was successfully validated in standard mode for the Arria 10 device (PCIe40)

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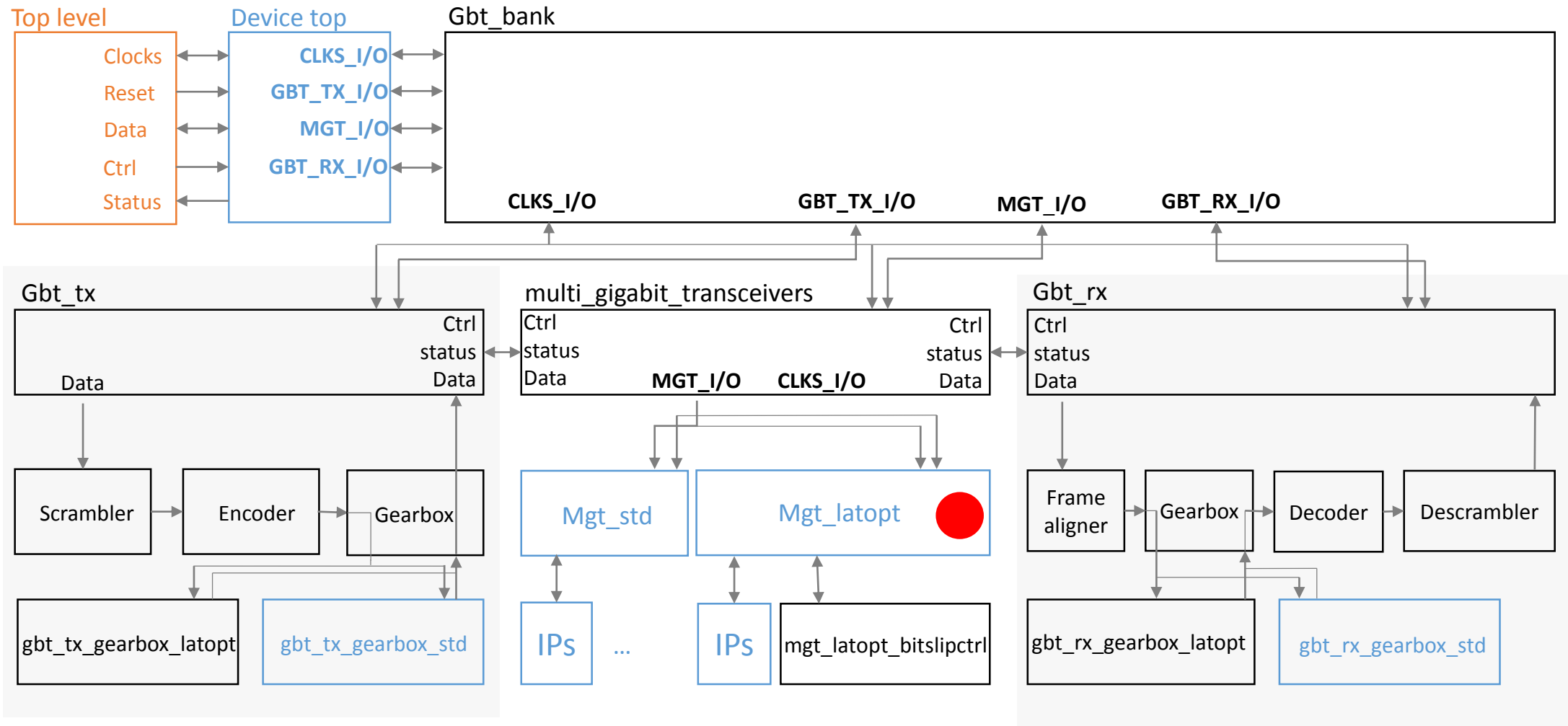
Why do we use records in the GBT-FPGA core?



Why do we use records in the GBT-FPGA core?

- Entity of the generic transceiver instantiation VHDL

```
--================================================================================--
--############################    Entity    ################################--
--================================================================================--

entity mgt_latopt is
   generic (
      GBT_BANK_ID           : integer := 1;
        NUM_LINKS           : integer := 1;
        TX_OPTIMIZATION     : integer range 0 to 1 := STANDARD;
        RX_OPTIMIZATION     : integer range 0 to 1 := STANDARD;
        TX_ENCODING         : integer range 0 to 1 := GBT_FRAME;
        RX_ENCODING         : integer range 0 to 1 := GBT_FRAME
   );
   port (

      --================--
      -- Clocks scheme --
      --================--

      MGT_CLKS_I            : in  gbtBankMgtClks_i_R;
      MGT_CLKS_O            : out gbtBankMgtClks_o_R;

      --==========--
      -- MGT I/O --
      --==========--

      MGT_I                 : in  mgt_i_R;
      MGT_O                 : out mgt_o_R;
```

alt_ax_gbt_bank_package.vhd

```
type mgtCommon_i_R is
record
      -- Reconfigurator
      reconf_reset              : std_logic;
      reconf_clk                : std_logic;
      reconf_avmm_addr          : std_logic_vector(12 downto 0);
      reconf_avmm_read          : std_logic;
      reconf_avmm_write         : std_logic;
      reconf_avmm_writedata     : std_logic_vector(31 downto 0);
end record;

type mgtCommon_o_R is
record
      -- Reconfigurator
      reconf_avmm_readdata      : std_logic_vector(31 downto 0);
      reconf_avmm_waitrequest   : std_logic;
end record;
```

gbt_bank_package.vhd

```
--====================================--
-- Multi Gigabit Transceivers (MGT) --
--====================================--

type mgt_i_R is
record
   mgtCommon        : mgtCommon_i_R;
   mgtLink          : mgtLink_i_R_A(1 to MAX_NUM_GBT_LINK);
end record;

type mgt_o_R is
record
   mgtCommon        : mgtCommon_o_R;
   mgtLink          : mgtLink_o_R_A(1 to MAX_NUM_GBT_LINK);
end record;
```

Why do we use records in the GBT-FPGA core?

Xilinx Kintex 7 package (xlx_k7v7_gbt_bank_package.vhd)

```
type mgtLink_i_R is
record
    rx_p                : std_logic;
    rx_n                : std_logic;
    --------------------
    loopBack            : std_logic_vector( 2 downto 0);
    --------------------
    tx_reset            : std_logic;
    rx_reset            : std_logic;
    --------------------
    rxBitSlip_enable    : std_logic;
    rxBitSlip_ctrl      : std_logic;
    rxBitSlip_nbr       : std_logic_vector(GBTRX_BITSLIP_NBR_MSB downto 0);
    rxBitSlip_run       : std_logic;
    rxBitSlip_oddRstEn  : std_logic;
    --------------------
    conf_diffCtrl       : std_logic_vector( 3 downto 0);
    conf_postCursor     : std_logic_vector( 4 downto 0);
    conf_preCursor      : std_logic_vector( 4 downto 0);
    conf_txPol          : std_logic;
    conf_rxPol          : std_logic;
    --------------------
    drp_addr            : std_logic_vector( 8 downto 0);
    drp_en              : std_logic;
    drp_di              : std_logic_vector(15 downto 0);
    drp_we              : std_logic;
    --------------------
    prbs_txSel          : std_logic_vector( 2 downto 0);
    prbs_rxSel          : std_logic_vector( 2 downto 0);
    prbs_txForceErr     : std_logic;
    prbs_rxCntReset     : std_logic;
end record;
```

Altera Arria 10 package (alt_a10_gbt_bank_package.vhd)

```
type mgtLink_i_R is
record
    tx_reset            : std_logic;
    rx_reset            : std_logic;
    ------------------------
    rxSerialData        : std_logic;
    ------------------------
    loopBack            : std_logic;
    ------------------------
    tx_polarity         : std_logic;
    rx_polarity         : std_logic;
    ------------------------
    rxBitSlip_enable    : std_logic;
    rxBitSlip_ctrl      : std_logic;
    rxBitSlip_nbr       : std_logic_vector(GBTRX_BITSLIP_NBR_MSB downto 0);
    rxBitSlip_run       : std_logic;
    rxBitSlip_oddRstEn  : std_logic;
end record;
```

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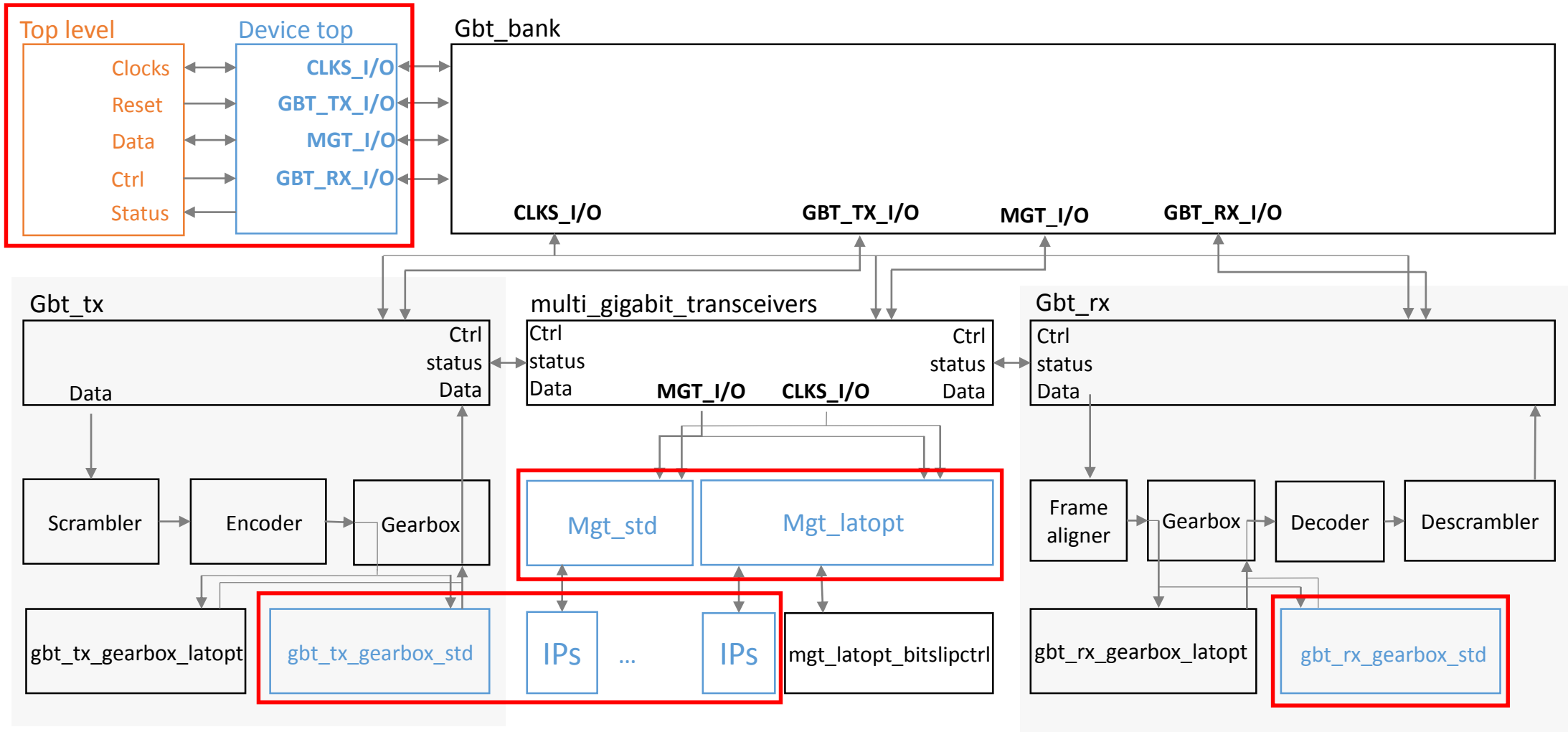
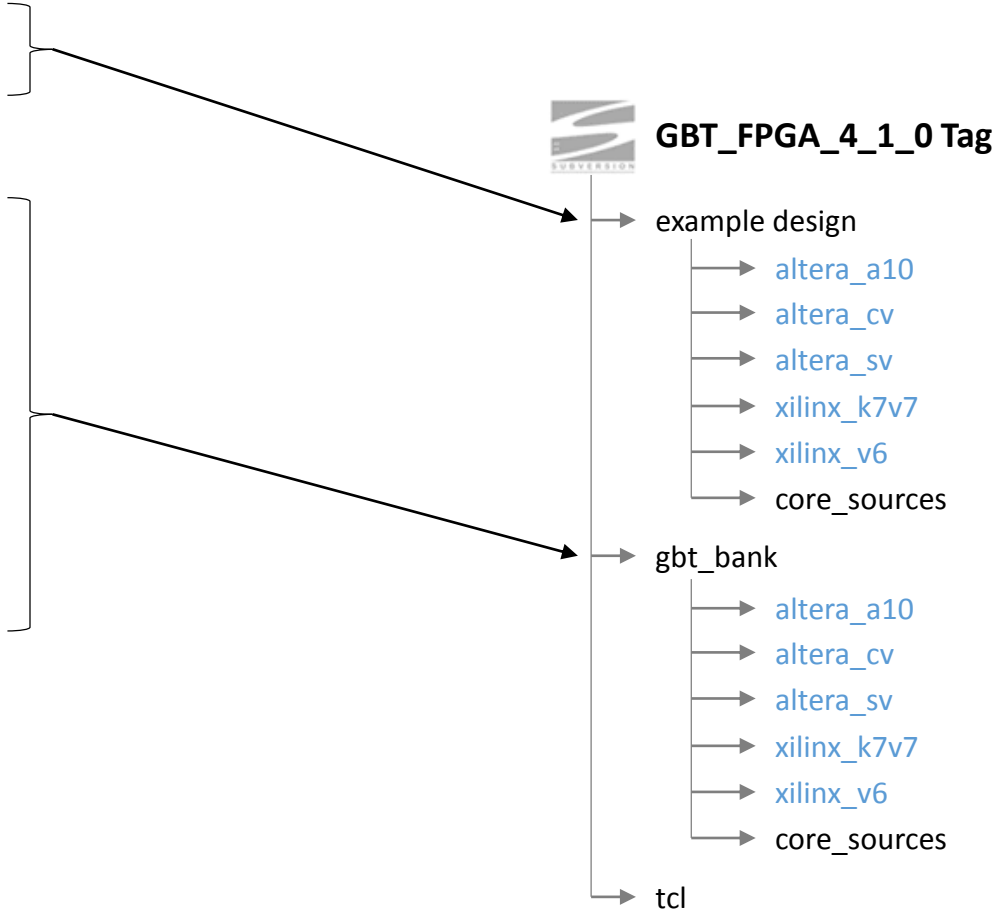
Is it easy to migrate the GBT-FPGA core to an unsupported FPGA? (MGT core …)



Is it easy to migrate the GBT-FPGA core to an unsupported FPGA? (MGT core …)

- Creation of the device specific top level

- Creation of the vendor_specific_package
  - Record definition
- Creation of the transceiver IP
  - Special care is required for latency optimized
- Creation of the dual ram memory IP
  - Used by the gearbox in std mode



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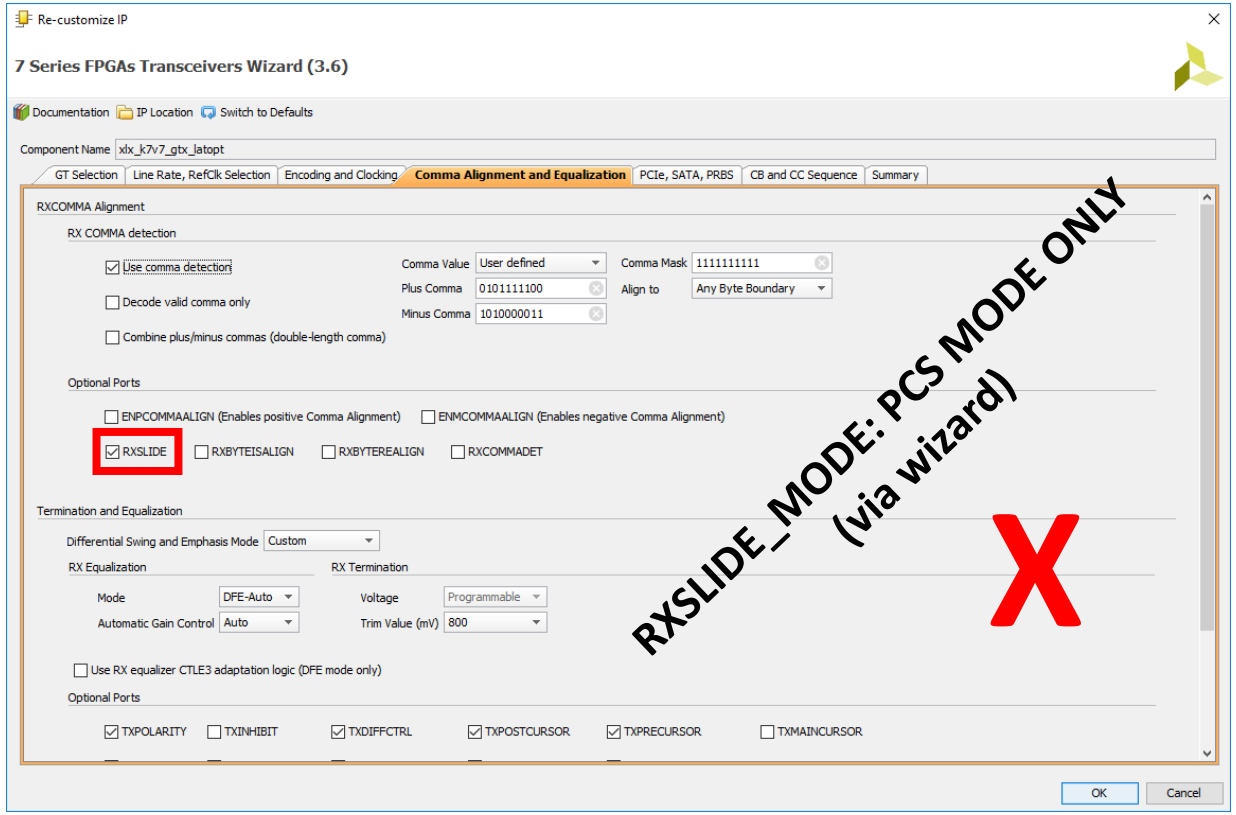
Why don’t we use the GTX wizard for Xilinx FPGAs?

- In Xilinx, 2 RX slide modes exist:
  - PCS: Data are shifted
  - PMA: Rx clock and data are shifted (**required for latency-optimized mode**)



xlx_k7v7_mgt_ip_gt.vhd

```
gtxe2_i :GTXE2_CHANNEL
generic map
(
    --_____________________ Simulation-Only Attributes _____________________

    SIM_RECEIVER_DETECT_PASS    =>      ("TRUE"),
    SIM_RESET_SPEEDUP           =>      (GT_SIM_GTRESET_SPEEDUP),
    SIM_TX_EIDLE_DRIVE_LEVEL    =>      ("X"),
    SIM_CPLLREFCLK_SEL          =>      (SIM_CPLLREFCLK_SEL),
    SIM_VERSION                 =>      ("4.0"),


  ------------------RX Byte and Word Alignment Attributes---------------
    ALIGN_COMMA_DOUBLE                      =>      ("FALSE"),
    ALIGN_COMMA_ENABLE                      =>      ("1111111111"),
    ALIGN_COMMA_WORD                        =>      (1),
    ALIGN_MCOMMA_DET                        =>      ("TRUE"),
    ALIGN_MCOMMA_VALUE                      =>      ("1010000011"),
    ALIGN_PCOMMA_DET                        =>      ("TRUE"),
    ALIGN_PCOMMA_VALUE                      =>      ("0101111100"),
    SHOW_REALIGN_COMMA                      =>      ("FALSE"),
    RXSLIDE_AUTO_WAIT                       =>      (7),
    RXSLIDE_MODE                            =>      ("PMA"),
    RX_SIG_VALID_DLY                        =>      (10),
    ...
```

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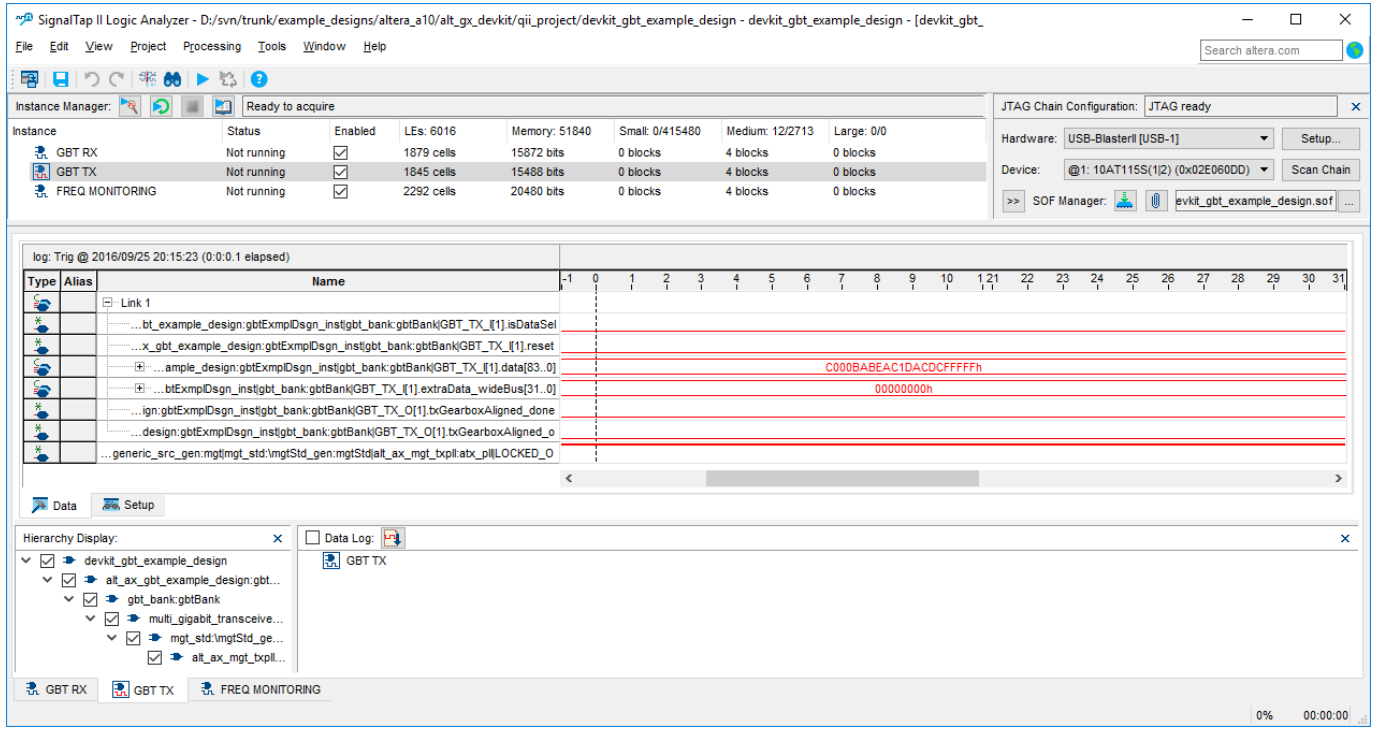
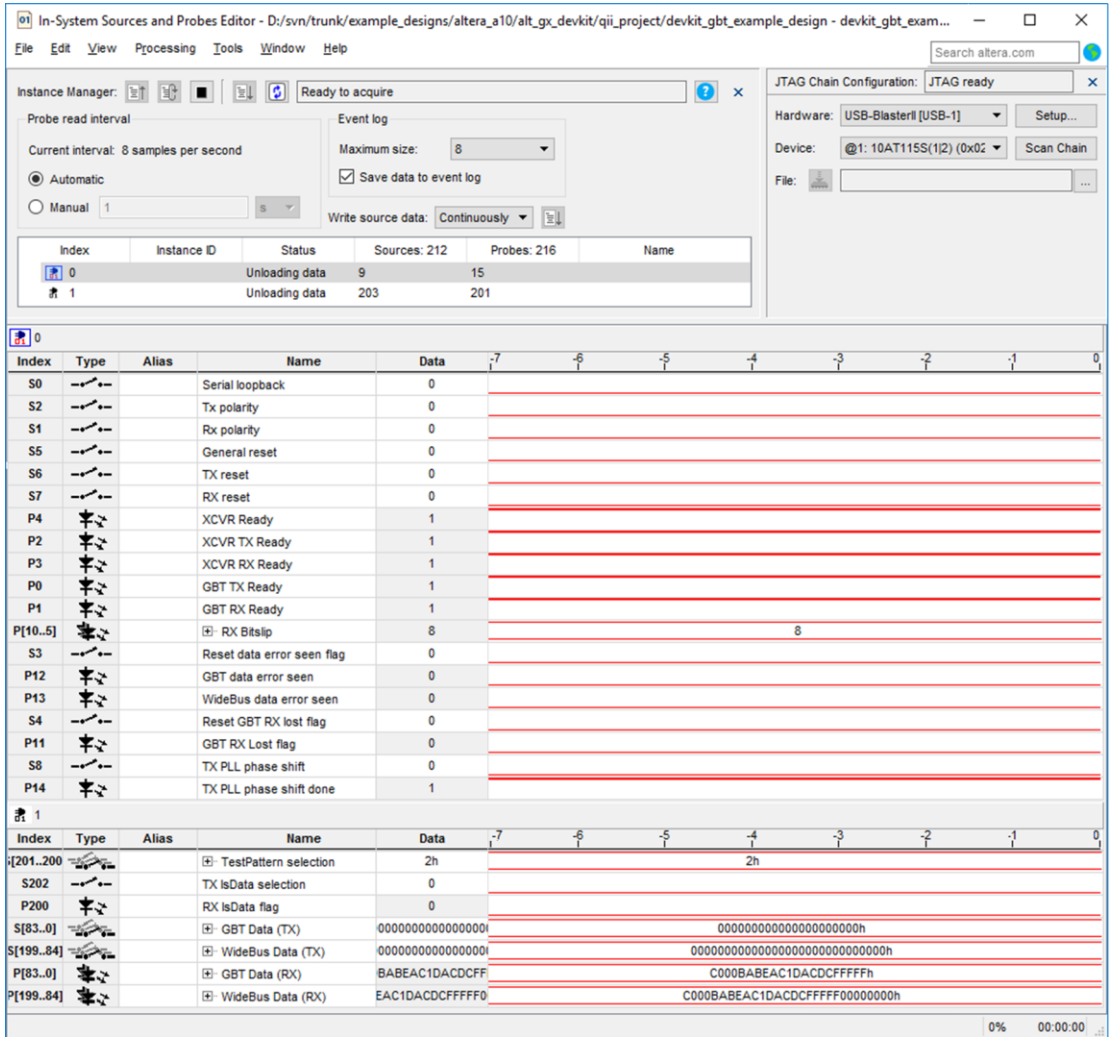
How can I check my firmware using the GBT-FPGA?

- Altera devices:
  - ISSP and SignalTap

Signaltap for Arria 10 development kit design



ISSP configuration for Arria 10 design



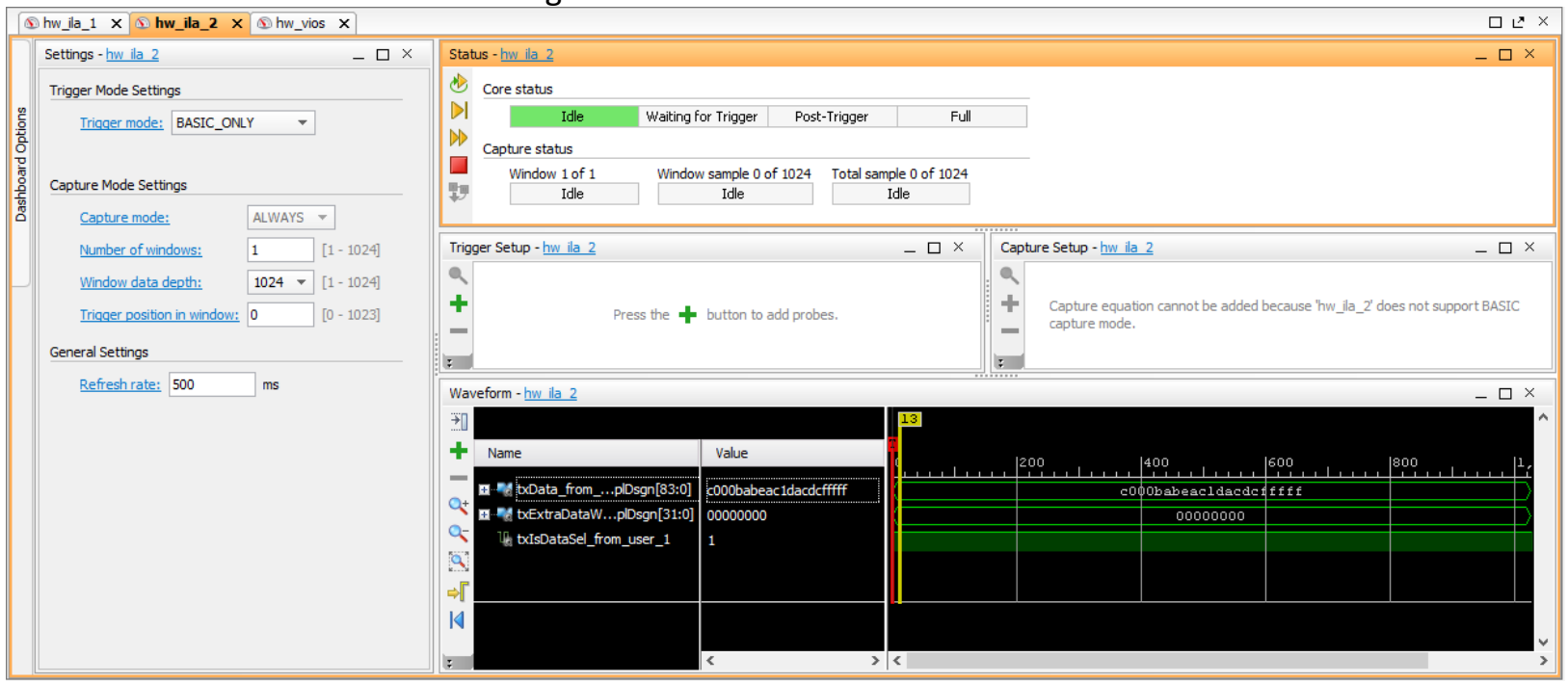
How can I check my firmware using the GBT-FPGA?

- Xilinx devices:
  - VIO and ILA

VIO for Kintex Ultrascale KCU105 design

Name	Value	Activity	Direction
testPatterSel_from_user[1:0]	[H] 3		Output
loopBack_from_user[2:0]	[H] 0		Output
latOptGbtBankRx_from_gbtExmplDsgn			Input
latOptGbtBankTx_from_gbtExmplDsgn			Input
generalReset_from_user	0		Output
manualResetRx_from_user	0		Output
manualResetTx_from_user	0		Output
mgtReady_from_gbtExmplDsgn			Input
gbtRxReady_from_gbtExmplDsgn			Input
rxWordClkReady_from_gbtExmplDsgn			Input
txFrameClkPllLocked_from_gbtExmplDsgn			Input
rxFrameClkReady_from_gbtExmplDsgn			Input
rxBitSlipNbr_from_gbtExmplDsgn[5:0]	[H] 17		Input
txIsDataSel_from_user	1		Output
rxIsData_from_gbtExmplDsgn			Input
resetDataErrorSeenFlag_from_user	0		Output
rxDataErrorSeen_from_gbtExmplDsgn			Input
rxExtrDataWidebusErSeen_from_gbtExmplDsgn			Input
resetGbtRxReadyLostFlag_from_user	0		Output
gbtRxReadyLostFlag_from_gbtExmplDsgn			Input
clkMuxSel_from_user	0		Output

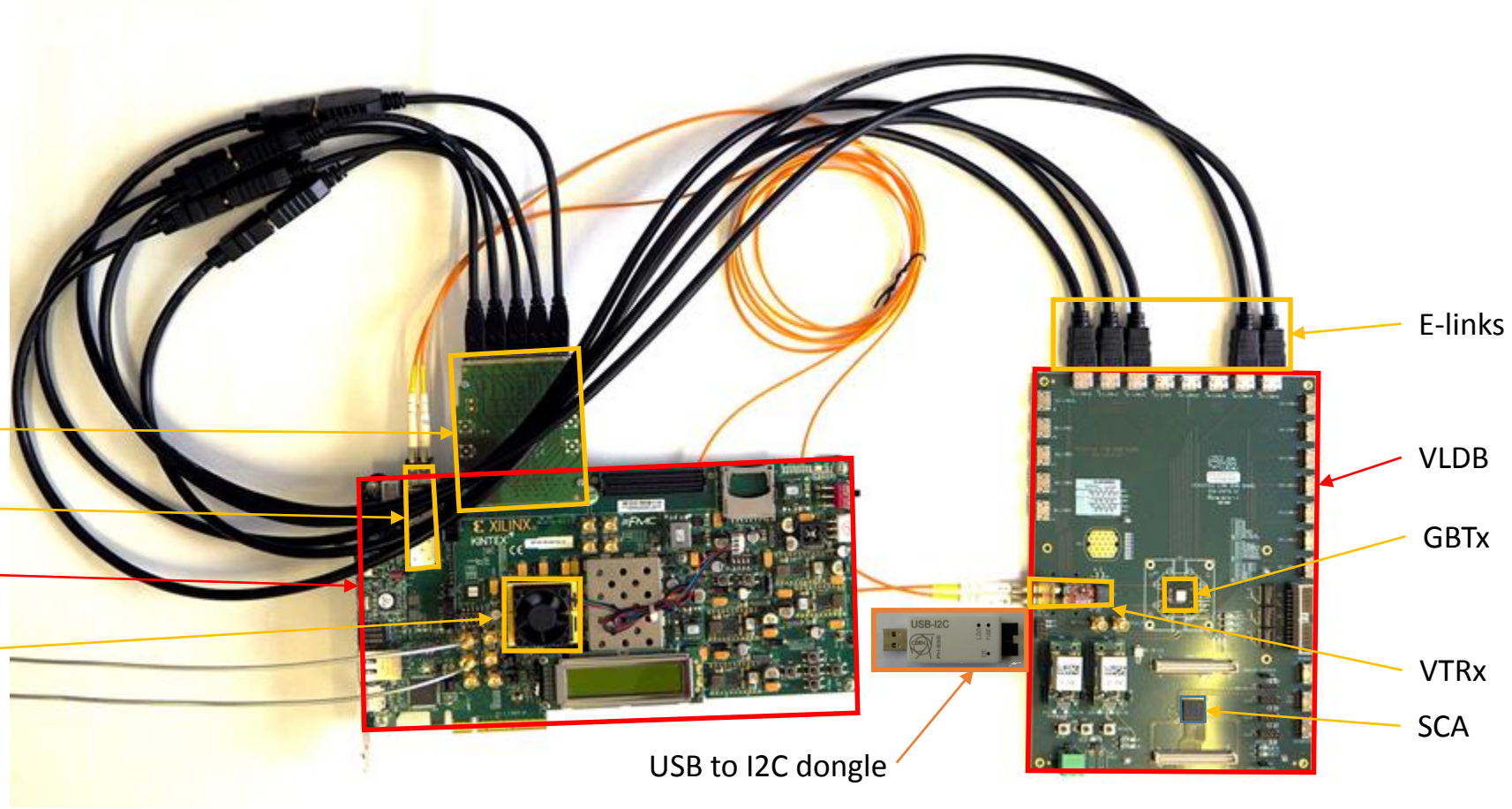
ILA for Kintex Ultrascale KCU105 design



How can I check my firmware using the GBT-FPGA?

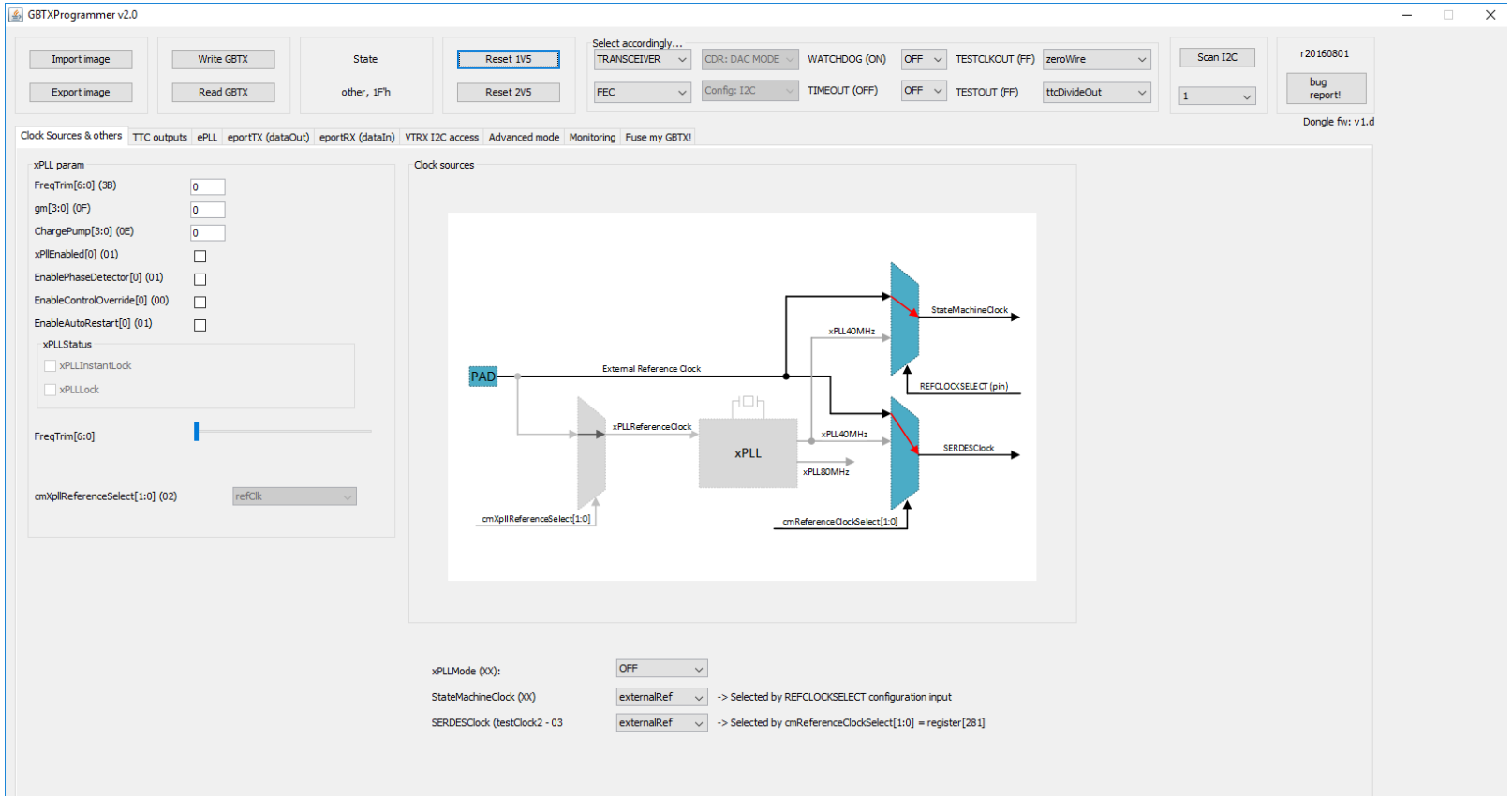
- Using VLDB or custom board implementing a GBTx

TWEPP 2016 [Poster H7, from Raul Martin Lesma] : The Versatile Link Board



How can I check my firmware using the GBT-FPGA?

- Configure the GBTx:
  - Tool and minimal config: https://espace.cern.ch/GBT-Project/VLDB/Control/Forms/AllItems.aspx
  - Tutorials: https://cds.cern.ch/collection/E-learning modules
  - Tool made by Pedro Leitao



Via I2C dongle

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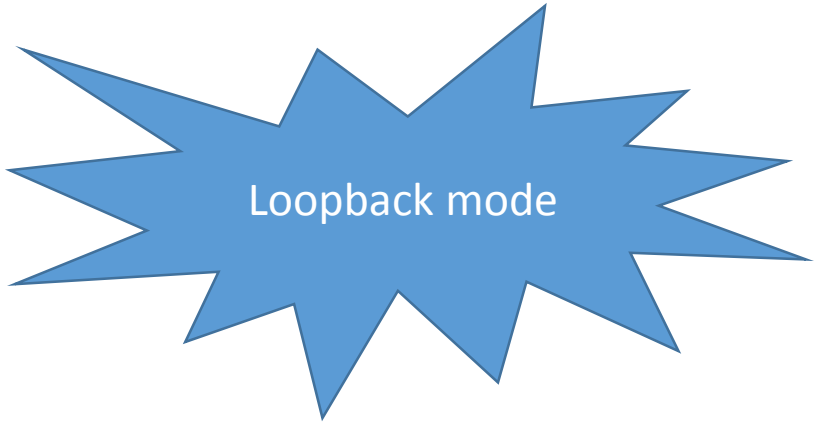
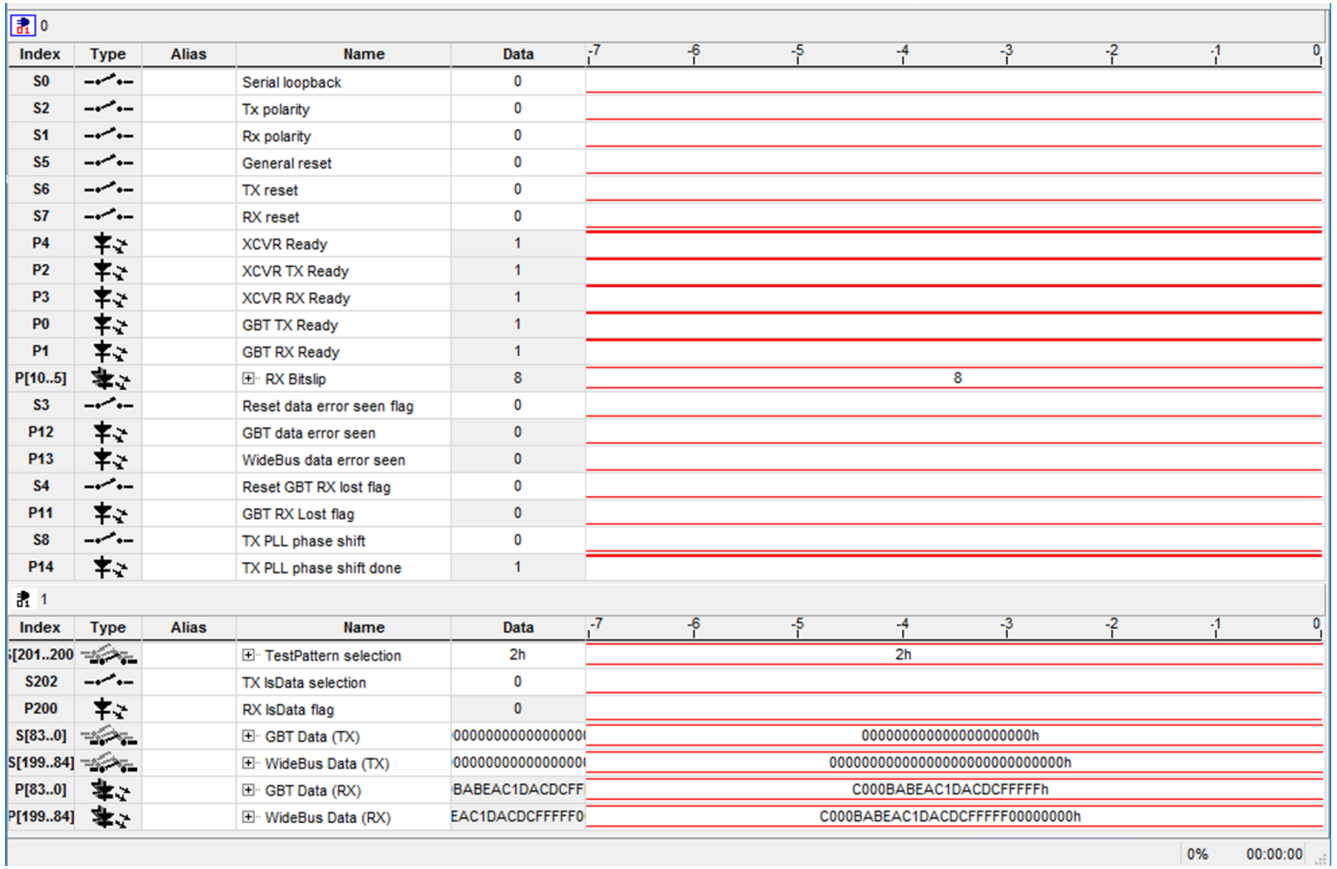
What are the first things to check when I am facing problems running the GBT-FPGA?

- Standard:
  - All the resets must be OFF (Active High)
  - All ready signals must be ON (Active High)
  - Fix bitslip
- Latency optimized:
  - Tx_gearboxAligned (signalTap / ILA): Shift the TX PLL until gearbox phases are aligned (recommended to perform a scan)





0

Index	Type	Alias	Name	Data
S0			Serial loopback	0
S2			Tx polarity	0
S1			Rx polarity	0
S5			General reset	0
S6			TX reset	0
S7			RX reset	0
P4			XCVR Ready	1
P2			XCVR TX Ready	1
P3			XCVR RX Ready	1
P0			GBT TX Ready	1
P1			GBT RX Ready	1
P[10..5]			RX Bitslip	8
S3			Reset data error seen flag	0
P12			GBT data error seen	0
P13			WideBus data error seen	0
S4			Reset GBT RX lost flag	0
P11			GBT RX Lost flag	0
S8			TX PLL phase shift	0
P14			TX PLL phase shift done	1

1

Index	Type	Alias	Name	Data
S[201..200]			TestPattern selection	2h
S202			TX IsData selection	0
P200			RX IsData flag	0
S[83..0]			GBT Data (TX)	00000000000000000000
S[199..84]			WideBus Data (TX)	00000000000000000000
P[83..0]			GBT Data (RX)	BABEAC1DACDCFF
P[199..84]			WideBus Data (RX)	EAC1DACDCFFFFF0

-7 -6 -5 -4 -3 -2 -1 0

8

2h

00000000000000000000h

00000000000000000000000000h

C000BABEAC1DACDCFFFFFh

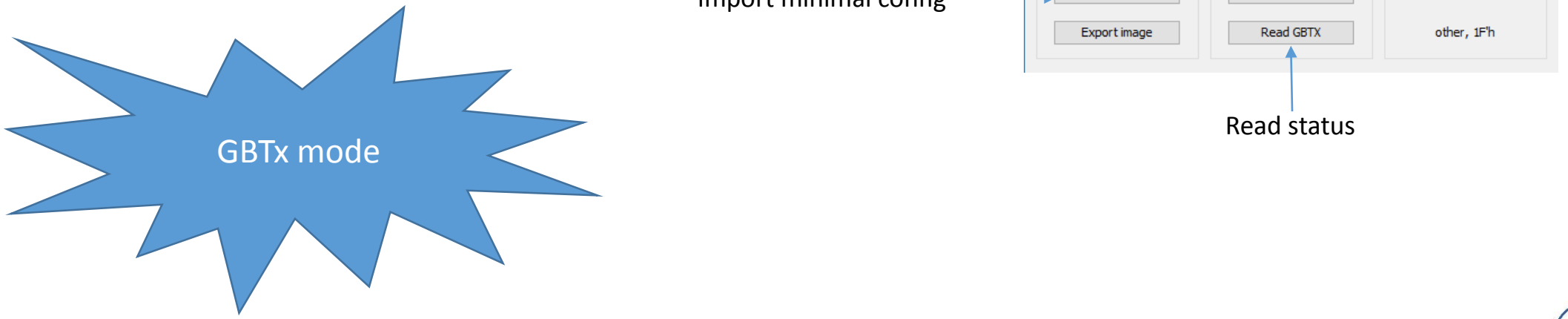
C000BABEAC1DACDCFFFFF00000000h

0% 00:00:00

What are the first things to check when I am facing problems running the GBT-FPGA?

- Standard:
  - GBTx must be configured
  - TX/RX polarity (GBTx serdes cannot lock when wrong polarity)
    - SFP and VTRx: inverted RX diff. pairs.

- Latency optimized:
  - TX Gearbox is aligned (phase alignment via the flag)



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What is coming next? What is the plan for new FPGAs families?

- SCA/IC : Slow control for GBT
- Testbench: simulation of the GBT and the slow control
- New FPGAs: Arria V and Virtex Ultrascale (and microsemi?)
- LpGBT

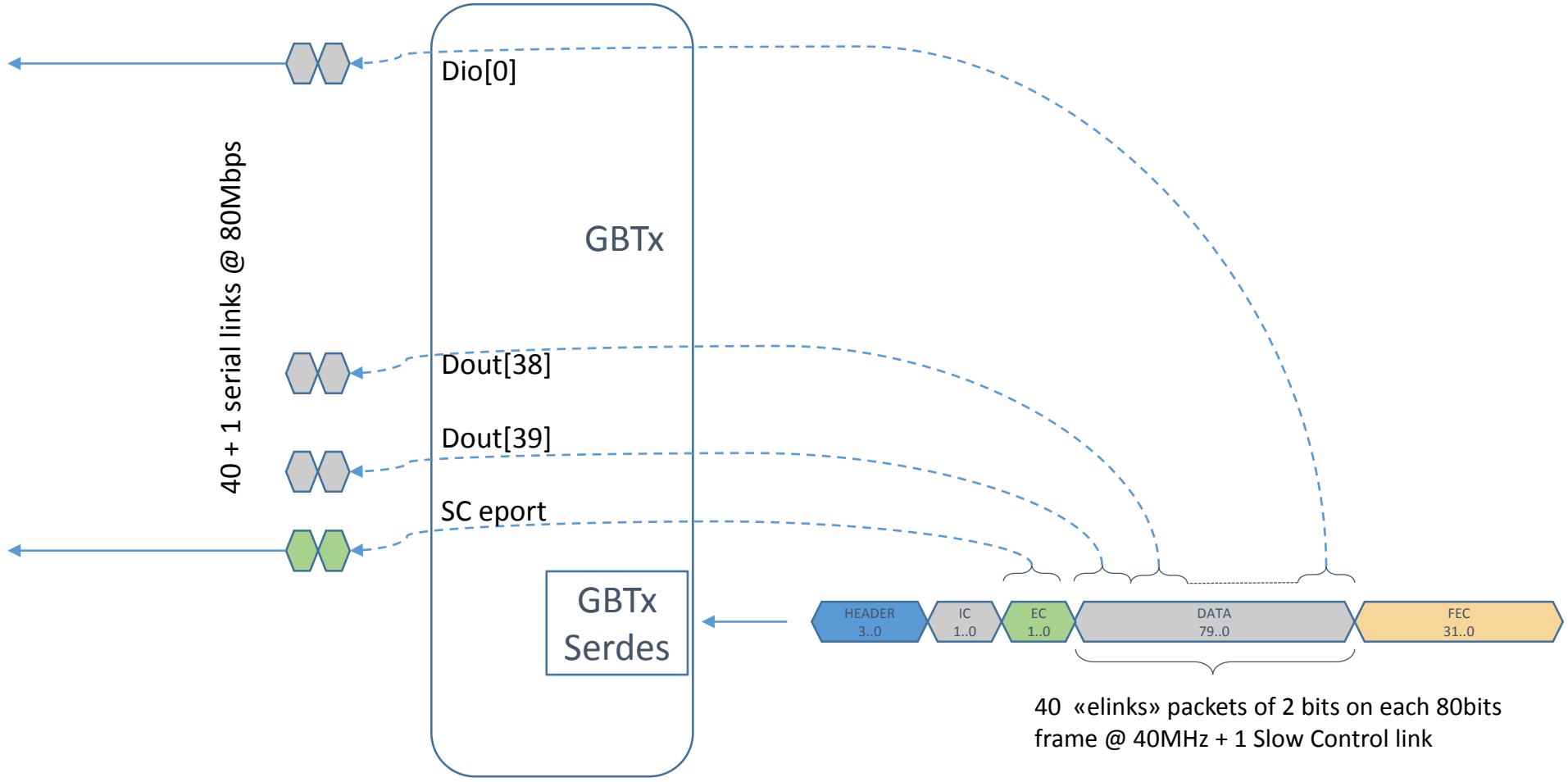
- Contributions from you are welcome

Thank you

GBT-FPGA-Support <gbt-fpga-support@cern.ch>

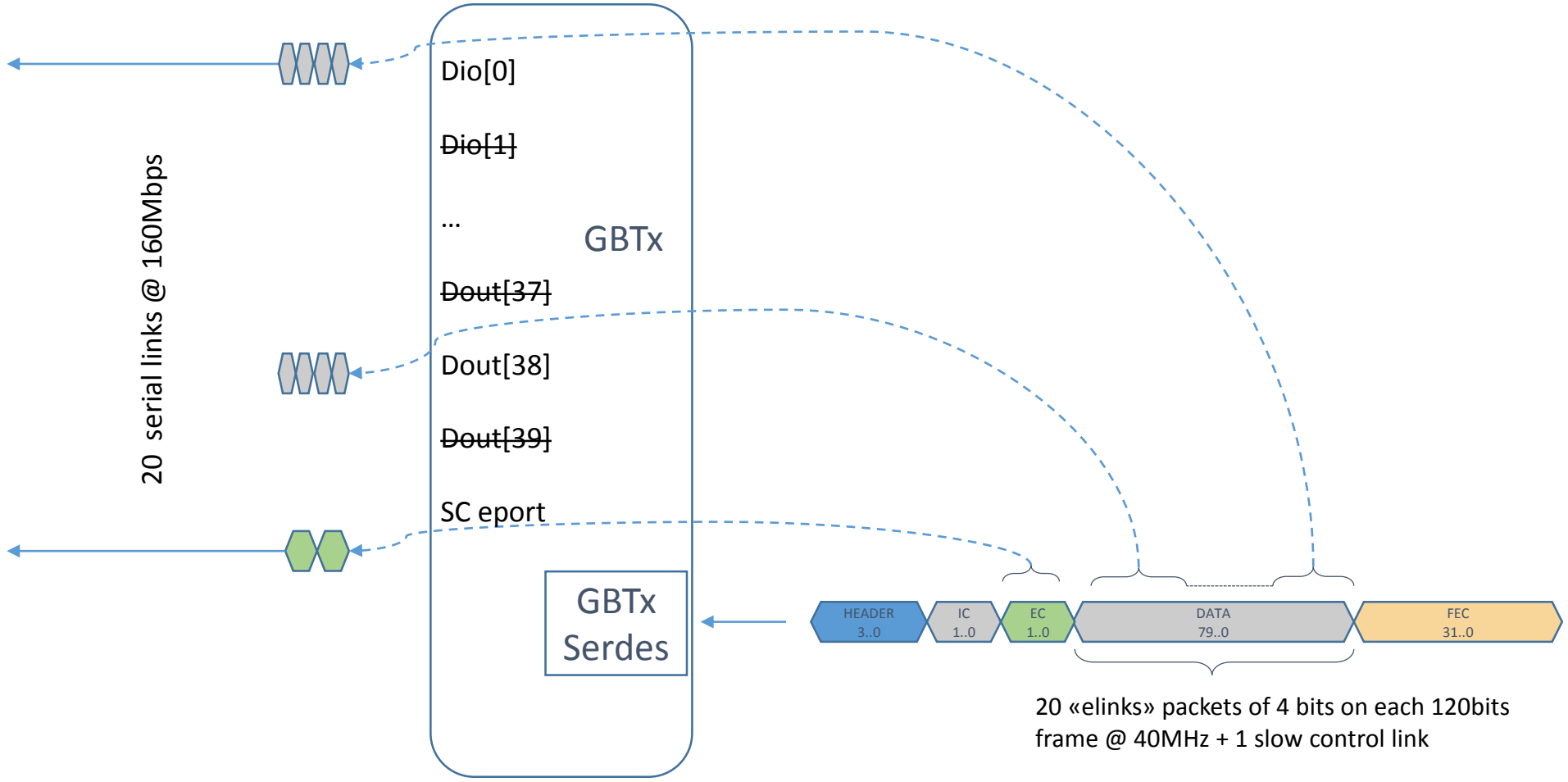
What is the relationship between GBT-link and e-links?

- Downstream Elink mode «x2» (80Mb/s)



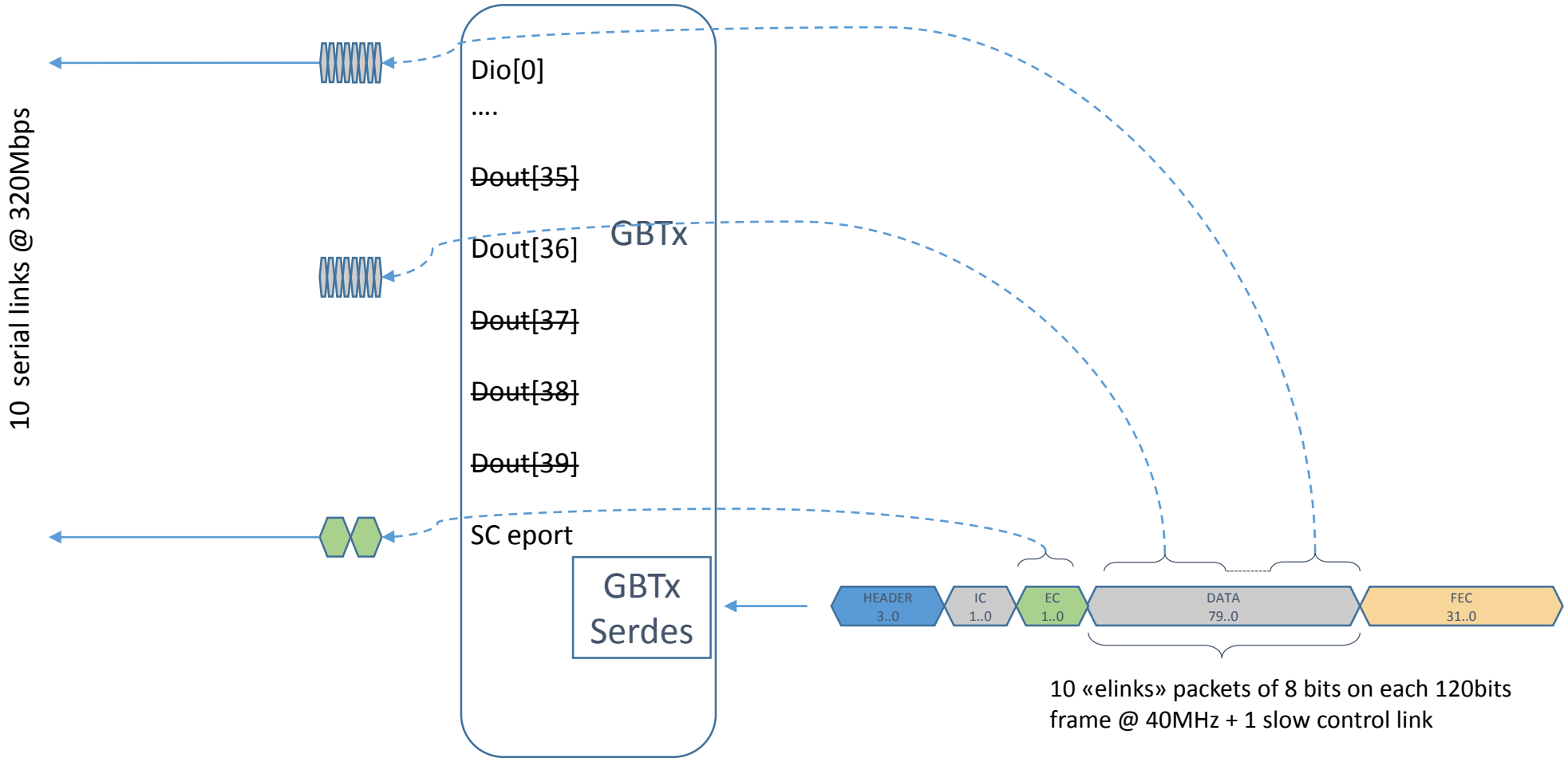
What is the relationship between GBT-link and e-links?

- Downstream Elink mode «x4» (160Mb/s)



What is the relationship between GBT-link and e-links?

- Downstream Elink mode «x4» (320Mb/s)



Why do we use records in the GBT-FPGA core?

- What are the GBT Bank interfaces ?

Warning: configuration can be made using two different ways ! Do not mix these to avoid bugs.

First way: Specify only the GBT_BANK_ID parameters when you implement the module. In this case, the information are get from the ***gbt_banks_user_setup*** package (gbt_bank/your_device/xxx_xxx_gbt_bank_user_setup.vhd)

Second way: Specify all the parameters **except** the GBT_BANK_ID (its value shall be 0, default value).

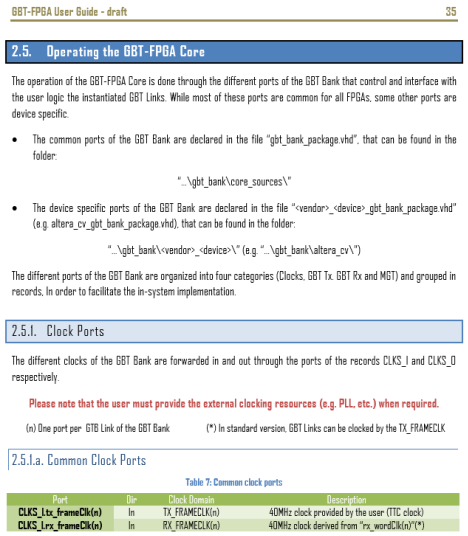
Configuration

Records

```
--=================================================================================================--
--#########################################   Entity   ##############################################--
--=================================================================================================--

entity gbt_bank is
   generic (
      GBT_BANK_ID                               : integer := 0;
      NUM_LINKS                                 : integer := 1;
      TX_OPTIMIZATION                           : integer range 0 to 1 := STANDARD;
      RX_OPTIMIZATION                           : integer range 0 to 1 := STANDARD;
      TX_ENCODING                               : integer range 0 to 1 := GBT_FRAME;
      RX_ENCODING                               : integer range 0 to 1 := GBT_FRAME
   );
   port (

      --========--
      -- Clocks --
      --========--

      CLKS_I                                    : in  gbtBankClks_i_R;
      CLKS_O                                    : out gbtBankClks_o_R;

      --========--
      -- GBT TX --
      --========--

      GBT_TX_I                                  : in  gbtTx_i_R_A       (1 to NUM_LINKS);
      GBT_TX_O                                  : out gbtTx_o_R_A       (1 to NUM_LINKS);

      --====================================--
      -- Multi Gigabit Transceivers (MGT) --
      --====================================--

      MGT_I                                     : in  mgt_i_R;
      MGT_O                                     : out mgt_o_R;

      --========--
      -- GBT RX --
      --========--

      GBT_RX_I                                  : in  gbtRx_i_R_A       (1 to NUM_LINKS);
      GBT_RX_O                                  : out gbtRx_o_R_A       (1 to NUM_LINKS)

   );
end gbt_bank;
```

Why do we use records in the GBT-FPGA core?

- How to find records definition?
  - GBT-FPGA User guide
    - 2.5. Operating the GBT-FPGA Core
  - VHDL files
    - gbt_bank/core_sources/gbt_bank_package.vhd: records generic for all the devices
    - gbt_bank/<device>/xxx_xxx_gbt_bank_package.vhd: device specific records



GBT-FPGA User Guide - draft 35

2.5. Operating the GBT-FPGA Core

The operation of the GBT-FPGA Core is done through the different ports of the GBT Bank that control and interface with the user logic the instantiated GBT Links. While most of these ports are common for all FPGAs, some other ports are device specific.

- The common ports of the GBT Bank are declared in the file "gbt_bank_package.vhd", that can be found in the folder:

  "...\gbt_bank\core_sources\"

- The device specific ports of the GBT Bank are declared in the file "<vendor>_<device>_gbt_bank_package.vhd" (e.g. altera_cv_gbt_bank_package.vhd), that can be found in the folder:

  "...\gbt_bank\<vendor>_<device>\" (e.g. "...\gbt_bank\altera_cv\")

The different ports of the GBT Bank are organized into four categories (Clocks, GBT Tx, GBT Rx and MGT) and grouped in records, In order to facilitate the in-system implementation.

2.5.1. Clock Ports

The different clocks of the GBT Bank are forwarded in and out through the ports of the records CLKS_I and CLKS_O respectively.

Please note that the user must provide the external clocking resources (e.g. PLL, etc.) when required.

(n) One port per GTB Link of the GBT Bank (*) In standard version, GBT Links can be clocked by the TX_FRAMECLK

2.5.1.a. Common Clock Ports

Table 7: Common clock ports

Port	Dir	Clock Domain	Description
CLKS_Ltx_frameClk(n)	In	TX_FRAMECLK(n)	40MHz clock provided by the user (TTC clock)
CLKS_Lrx_frameClk(n)	In	RX_FRAMECLK(n)	40MHz clock derived from "rx_wordClk(n)"(*)

```
--================================================================================================--
--#################################   Package Declaration   ########################################--
--================================================================================================--

package gbt_bank_package is

   --================================ Record Declarations ================================--

   --================--
   -- Clocks scheme --
   --================--

   type gbtBankClks_i_R is
   record
      tx_frameClk                           : std_logic_vector(1 to MAX_NUM_GBT_LINK);
      rx_frameClk                           : std_logic_vector(1 to MAX_NUM_GBT_LINK);
      ------------------------------------------
      mgt_clks                              : gbtBankMgtClks_i_R;
   end record;

   type gbtBankClks_o_R is
   record
      mgt_clks                              : gbtBankMgtClks_o_R;
   end record;

   --=========--
   -- GBT Tx --
   --=========--

   type gbtTx_i_R is
   record
      reset                                 : std_logic;
      ------------------------------------------
      isDataSel                             : std_logic;
      ------------------------------------------
      data                                  : std_logic_vector(83 downto 0);
      extraData_wideBus                     : std_logic_vector(31 downto 0);
   end record;
```

Why do we use records in the GBT-FPGA core?

- Transceiver IP for Altera Arria 10

```
gxLatOpt_x5: entity gx_latopt_x1.gx_latopt_x1
    port map(

        -- Reconfigurator avalon MM bus
        reconfig_write(0)          => MGT_I.mgtCommon.reconf_avmm_write,
        reconfig_read(0)           => MGT_I.mgtCommon.reconf_avmm_read,
        reconfig_address           => MGT_I.mgtCommon.reconf_avmm_addr(9 downto 0),
        reconfig_writedata         => MGT_I.mgtCommon.reconf_avmm_writedata,
        reconfig_readdata          => MGT_O.mgtCommon.reconf_avmm_readdata,
        reconfig_waitrequest(0)    => MGT_O.mgtCommon.reconf_avmm_waitrequest,
        reconfig_clk(0)            => MGT_I.mgtCommon.reconf_clk,
        reconfig_reset(0)          => MGT_I.mgtCommon.reconf_reset,
        …
```

- Transceiver IP for Xilinx Kintex Ultrascale

```
xlx_ku_mgt_std_i: xlx_ku_mgt_ip
   PORT MAP (
      drpaddr_in                   => MGT_I.mgtLink(i).drp_addr,
      drpclk_in(0)                 => MGT_CLKS_I.drpClk,
      drpdi_in                     => MGT_I.mgtLink(i).drp_di,
      drpen_in(0)                  => MGT_I.mgtLink(i).drp_en,
      drpwe_in(0)                  => MGT_I.mgtLink(i).drp_we,
      drpdo_out                    => MGT_O.mgtLink(i).drp_do,
      drprdy_out(0)                => MGT_O.mgtLink(i).drp_rdy,
      …
```