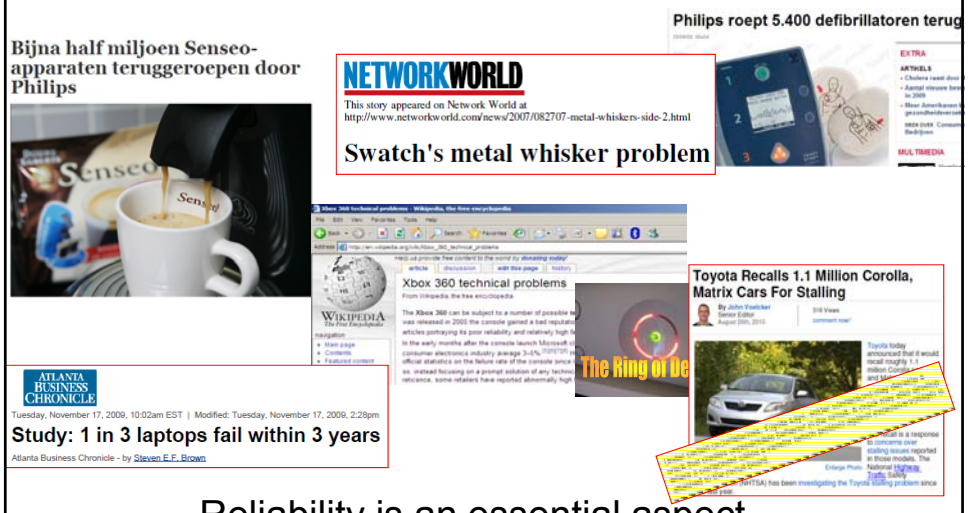
RELIABILITY AND FAILURE MECHANISMS OF INTEGRATED CIRCUITS AND DEVICES

GUIDO GROESENEKEN (IMEC, K.U.LEUVEN)
EMAIL: GUIDO.GROESENEKEN@IMEC.BE

IS RELIABILITY IMPORTANT ?

Some famous examples of the consequences of insufficient reliability

IS RELIABILITY IMPORTANT ?



Reliability is an essential aspect of all products and technologies

imec © IMEC 2016 3

IS RELIABILITY IMPORTANT ?

Reliability is an essential aspect of all products and technologies

imec © IMEC 2016 4

OUTLINE

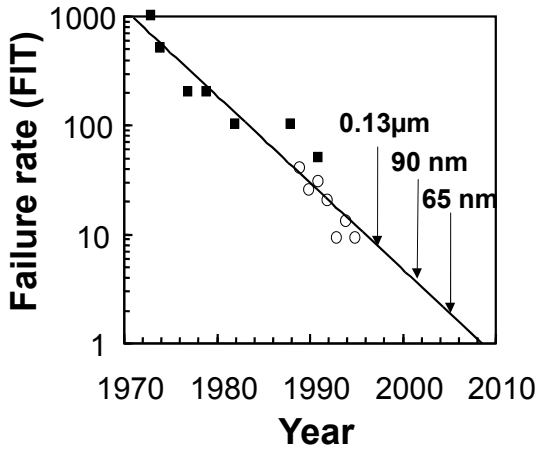
1. Introduction
2. Basic reliability concepts
3. Time-dependent Dielectric Breakdown (TDDB)
4. Hot carrier degradation
5. Bias-Temperature Instability (NBTI)

WHY IS RELIABILITY IMPORTANT ?

Reliability is becoming a major bottleneck in the further downscaling of VLSI technologies

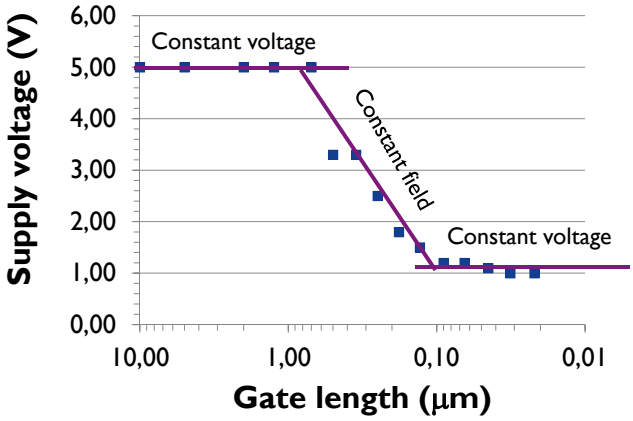
- Increasing fields and current densities
- Increasing power density and chip temperatures
- Increasing number of interfaces
- Increasing process complexity
- Introduction of new materials (high k, low k, Cu, metal gate)
- Increasing failure rate requirements

MARKET CONTINUOUSLY DEMANDS FOR HIGHER RELIABILITY LEVELS



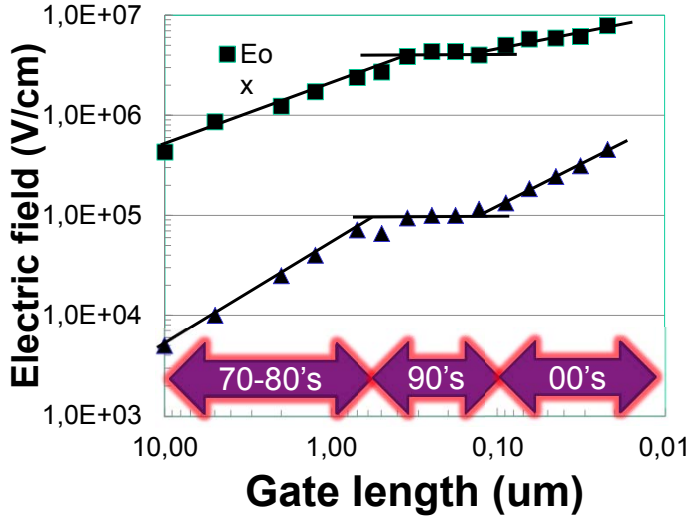
Maximum failure rate and defect density requirements are continuously increasing

Power supply voltage evolution



Power supply voltage is saturating at about 1V due to non-scaling of subthreshold slope

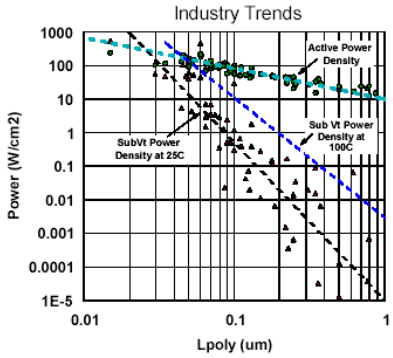
ELECTRIC FIELDS IN OXIDE AND IN SILICON STARTED TO INCREASE AGAIN !

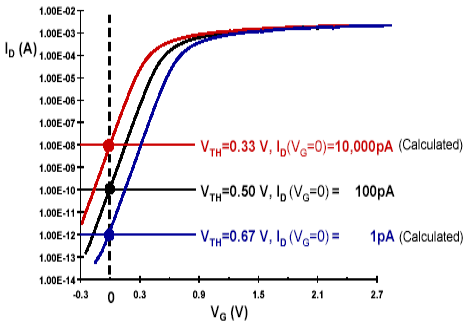


Third scaling period: renewed constant voltage scaling due to non-scaling subthreshold slope will have new implications on reliability !

 9

POWER DENSITY INCREASES





Power density will soon be dominated by static power !

D. Cox, IRPS Tutorial 2004

Dynamic :

$$P_{dyn} = \alpha \cdot V_{dd} \cdot V_{swing} \cdot C_{eff} \cdot f$$

Static :

$$P_{stat} = V_{dd} \cdot I_{leak}$$

Almost all reliability problems are accelerated by Temperature !

 10

TECHNOLOGY TRENDS

Performance requirements push intrinsic reliability of materials to the limit

- Gate oxide fields > 5MV/cm
- Interconnect current densities > $5x10^5$ A/cm^2

New materials introduced

- 70's: Si, Al, SiO_2 (oxides), Si_3N_4 (nitrides)
- 80-90's: Ti-silicide, Co-silicide, W, TiN, Al-Cu
- 2000: high k gate dielectrics (Hf-oxide, Zr-oxide, Ta-oxide), low k dielectrics, Cu metallization
- 2010: Ge, III-V, CNT, graphene ???

imec

HUGE RELIABILITY CHALLENGES AHEAD OF US !

- **high k gate dielectrics for logic and memory applications (HfO_2, HfSiON, Al2O3, etc.)**
- **metal gates (TaN, TiN, RuO, etc.)**
- **ferroelectric materials (PZT, BST, etc.)**
- **phase change materials, Resistive RAM materials**
- **nanodevices (MuGFET, Finfet, Ge, III-V devices, TFET's, CNT, nanowires, graphene devices)**
- **low k dielectrics/barrier materials/airgaps**
- **Cu metallization, CNT interconnects, Cu contacts, ….**

Unknown reliability behavior and/or new failure mechanisms !

Speed of introduction exceeds capabilities to explore reliability performance

imec

MAIN ON-CHIP RELIABILITY FAILURE MECHANISMS

1) Time-dependent dielectric breakdown
2) Hot carrier degradation
3) Bias-Temperature Instability
4) Electromigration
5) Stress voiding
6) Interconnect dielectric breakdown/ stability
7) Electrostatic Discharge sensitivity

imec

MAIN OFF-CHIP RELIABILITY FAILURE MECHANISMS

1) Creep
2) Fatigue
3) Stiction
4) Corrosion
5) Electromigration
6) Charging

Reliability needs a broad field of disciplines and expertises going from device physics, material science, surface chemistry, electrical and physical characterisation

imec

OUTLINE

1. Introduction
2. Basic reliability concepts
3. Time-dependent Dielectric Breakdown (TDDB)
4. Hot carrier degradation
5. Bias-Temperature Instability (NBTI)

 15

DEFINITIONS

Reliability = **probability** that an item will
- perform a **required function**
- under **stated conditions**
- for a **stated period of time**

probability: probabilistic models/statistical methods
- random variables, sample populations
- density functions (p.d.f., c.d.f.)
- mean time, median time-to-failure, failure rate

required function: includes definition of failure
- specification of satisfactory operation

stated conditions: total physical environment
- mechanical, thermal, environmental, electrical conditions

stated period of time: concept of lifetime
- required lifetime depends on application: telecom, consumer, space, automotive

 16

DEFINITIONS

Failure = termination of the ability of an item to perform a **required function** (within previously specified limits)

Failure mechanism = the physical, electrical, chemical, thermal or any other ***process*** which leads to a failure.

Examples:

Devices	**Interconnects**	**Packages**
hot carrier injection	electromigration	humidity/corrosion
NBTI	stress migration	moisture penetration
Gate oxide breakdown	low k dielectric BD	die cracking
		bond wire fracture

DEFINITIONS

Failure mode = consequence of the mechanism through which the failure occurs

or

that characteristic of the device for which it has been named a failure

Examples:

Devices/interconnects	*Circuits*
internal short or open	shift in access time
threshold voltage shift	power supply current increase
parametric variation	functional failure
Junction/gate leakage	stuck-at fault

DEFINITIONS

Intrinsic failures:

- inherent in the design and materials used
- managed by insuring that they occur beyond useful life of a product, by limiting loads that drive the failure mechanisms (e.g. maximum field, maximum current density, thermal management)

Extrinsic failures:

- due to process or manufacturing defects or to misapplications such as overload, EOS, ESD etc.
- managed by improving manufacturing process, reducing defect density
- usually product reliability is determined by extrinsic failures

imec 19

RELIABILITY AND FAILURE FUNCTIONS

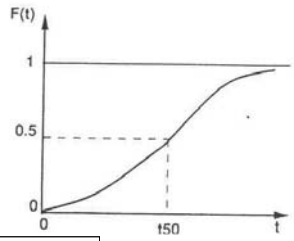
Random variable x: **time t**

a) Cumulative Failure Function: F(t)

$t < 0 \quad \rightarrow \quad F(t) = 0$

$0 \le t \le t' \quad \rightarrow \quad 0 \le F(t) \le F(t')$

$t \rightarrow \infty \quad \rightarrow \quad F(t) \rightarrow 1$

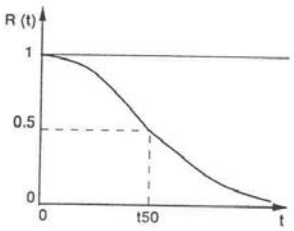


F(t) = probability that a device will fail at or before time t
= **percentage of failures at time t**

b) Reliability function: R(t)

R(t) = Probability that a device will survive to time t without failure
= **percentage of good devices at time t**

$R(t) = 1 - F(t)$



imec 20

RELIABILITY AND FAILURE FUNCTIONS

c) Failure density function: f(t) : = p.d.f.

f(t)dt = probability that an item will fail between time t and t + dt

$$f(t) = \frac{dF(t)}{dt} = -\frac{dR(t)}{dt}$$

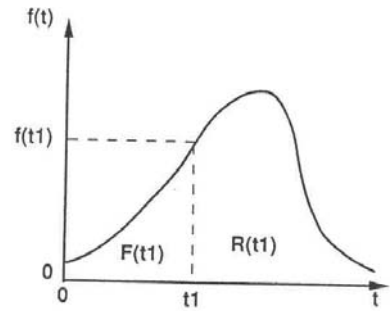
$$F(t_1) = \int_0^{t_1} f(t)dt$$

$$R(t_1) = 1 - \int_0^{t_1} f(t)dt = \int_{t_1}^{\infty} f(t)dt$$

d) Mean time to failure: MTTF

MTTF = mean value to the p.d.f.

$$MTTF = \int_0^{\infty} tf(t)dt$$



e) Median time to failure: MTF

MTF = median value to the p.d.f. f(t)
MTF = time when F(t) = 50% = t_{50}

RELIABILITY AND FAILURE FUNCTIONS

f) Failure rate

-instantaneous failure rate or hazard rate:

$$\lambda_i(t) = \lim_{\Delta t \to 0} \frac{F(t+\Delta t) - F(t)}{R(t) \times \Delta t}$$

$$= \frac{1}{R(t)} \times \frac{dF(t)}{dt}$$

fraction of failures in a time period (t, t+Δt) of those units that were good at the beginning of this period, divided by the period Δt

λ_I (t) = probability that a device will fail in the time interval (t, t+Δt), given that it has survived at time t

- cumulative failure rate = average hazard rate

$$\lambda_c(t) = \frac{1}{t}\int_0^t \lambda_i(t)dt$$

$$H(t) = \int_0^t \lambda_i(t)dt = \text{cumulative hazard function}$$

Units of failure rate: **# Failures/(devices x hours)**
Failure unit: **1 FIT = 1 failure/10^9 device hours** = 8.76 ppm/year

HAZARD RATE AND BATHTUB CURVE

If hazard rate λ_I (t) is **Decreasing** / **Constant** / **increasing** With time **Infant mortality** / **Useful life** / **Wear-out**

Bath tub curve = sum of 3 curves

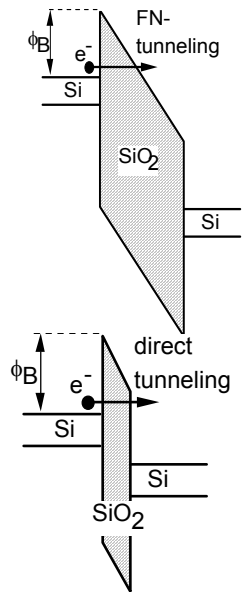
1) ***quality failures***: weaker parts (**manufacturing defects)** are getting removed from the population
2) ***stress related failures****:* failures occur occasionally at a constant rate
3) ***wear-out failures****:* accumulated damage takes its toll, devices start to fail with increasing frequency

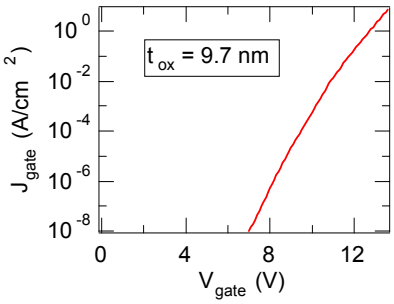
OUTLINE

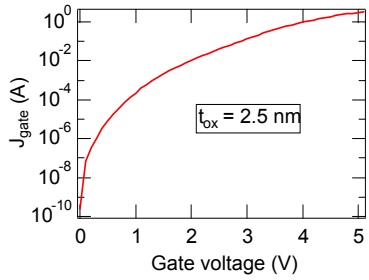
1. Introduction
2. Basic reliability concepts
3. Time-dependent Dielectric Breakdown (TDDB)
   - Basics
   - Statistics
   - Acceleration model
   - Impact on circuits
4. Hot carrier degradation
5. Bias-Temperature Instability (NBTI)

imec 24

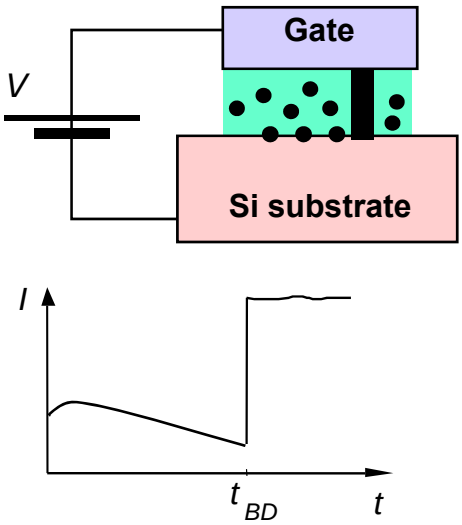
TUNNELING BASICS



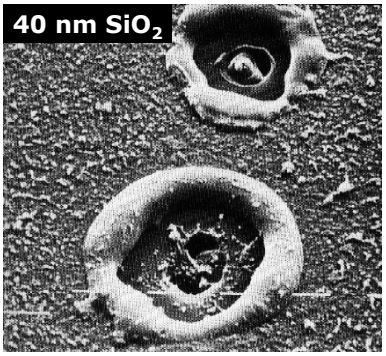




(GIST OF) GATE OXIDE BREAKDOWN



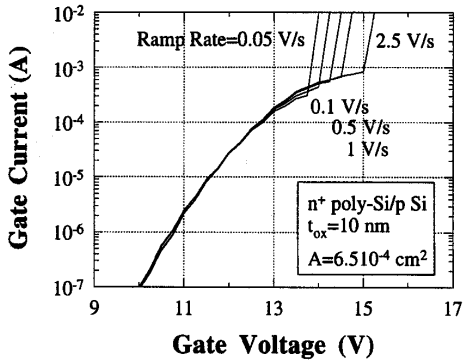
D. R. Wolters, Ph.D. Thesis, 1985



Gate oxide breakdown = catastrophic failure

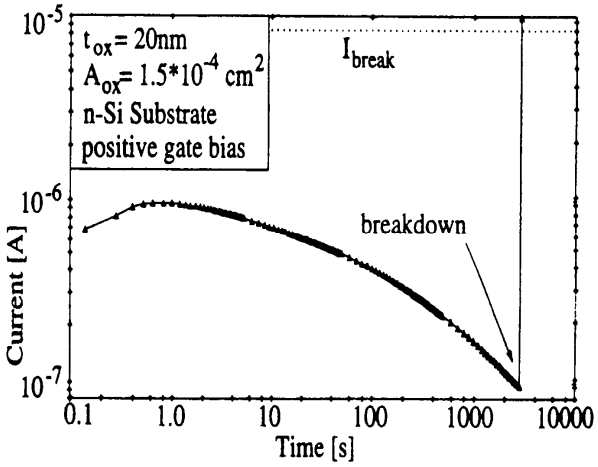
imec © IMEC 2016 26

RAMPED VOLTAGE TEST



- Apply a fast **voltage ramp** (typically 1-100V/s) and measure current
- **Breakdown voltage** is defined as the gate voltage at which a sudden current increase occurs
- Fixed **trigger current** is set (100uA to 5mA)
- Sensitive to series resistance effects !

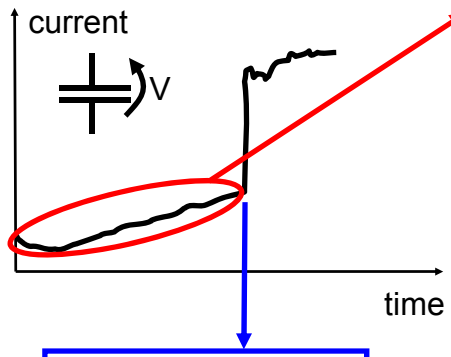
CONSTANT VOLTAGE STRESS



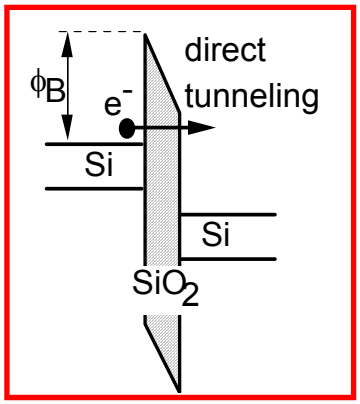
Oxide breakdown is a time-dependent phenomenon

TDDB = Time dependent Dielectric Breakdown

CONSTANT VOLTAGE STRESS (CVS)



Oxide degradation =



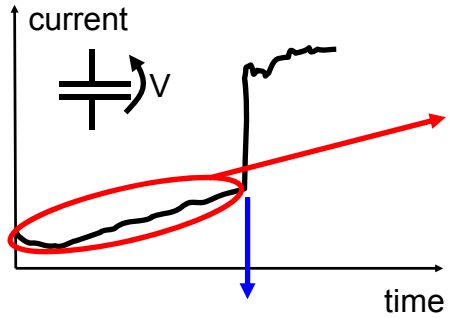
Dielectric breakdown =

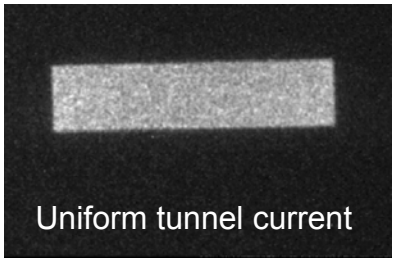
(sudden) loss of the insulating property

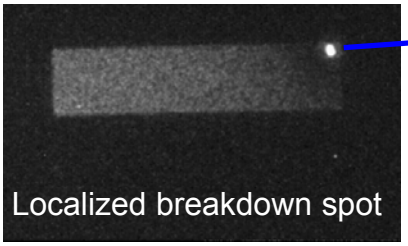
+

current change as a consequence of degradation

CVS SEEN BY THE EMISSION MICROSCOPE



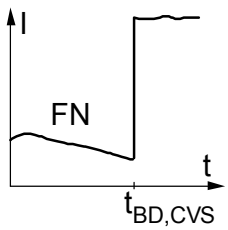


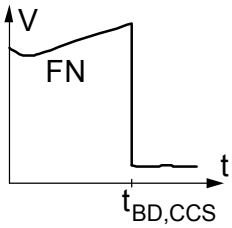


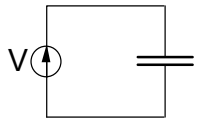
SPOT

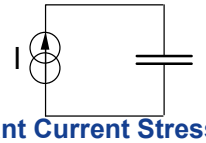
Breakdown is a localized event

TDDB: CVS AND CCS









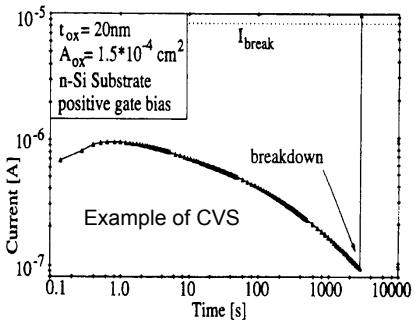
Constant Voltage Stress (CVS)

- average field is constant
- current increase: net positive charge; current decrease : net negative charge
- at fixed Vg: tbd decrease with thinner oxides

Constant Current Stress (CCS)

- net positive charge => decrease of average field (and voltage)
- net negative charge => increase applied voltage
- at fixed J: tbd increases witn thinner oxides

CHARGE-TO-BREAKDOWN



Degradation scales with charge fluence: for higher currents, lower t_{BD}

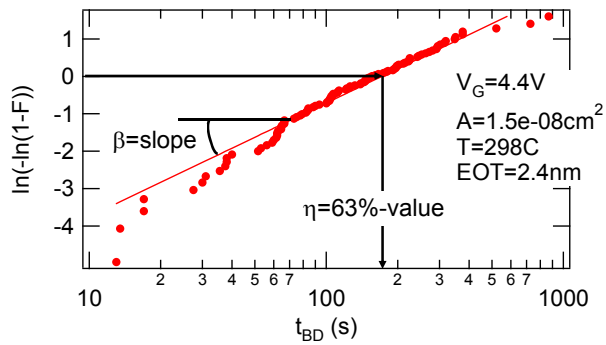
Charge - to - breakdown :

$$Q_{BD} = \int_0^{t_{BD}} J_n.dt' \quad \text{or} \quad \text{for CCS :} \quad Q_{BD} = J_n.t_{BD}$$

Q_{BD} is one of the main BD figure-of-merits of a technology: typically between 1-100 C/cm^2

When oxide thickness scales down: Q_{bd}-value becomes less relevant

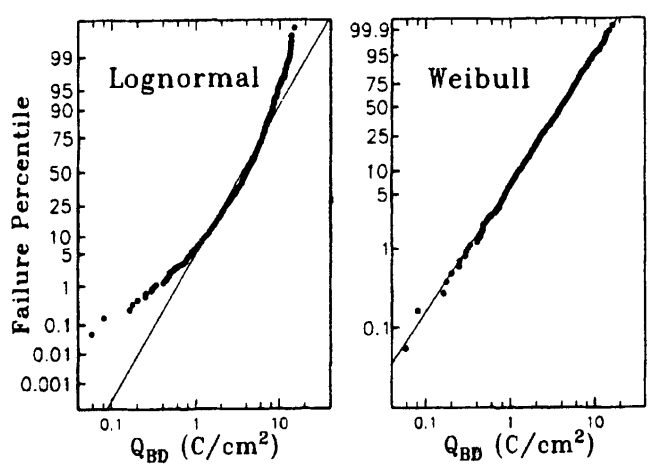
TIME-TO-BREAKDOWN = STATISTICALLY DISTRIBUTED PARAMETER



- Time-to-breakdown is Weibull distributed
- Monomodal Weibull distribution is described as:

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right] \Rightarrow \ln(-\ln(1-F)) = \beta \ln(t) - \beta \ln(\eta)$$

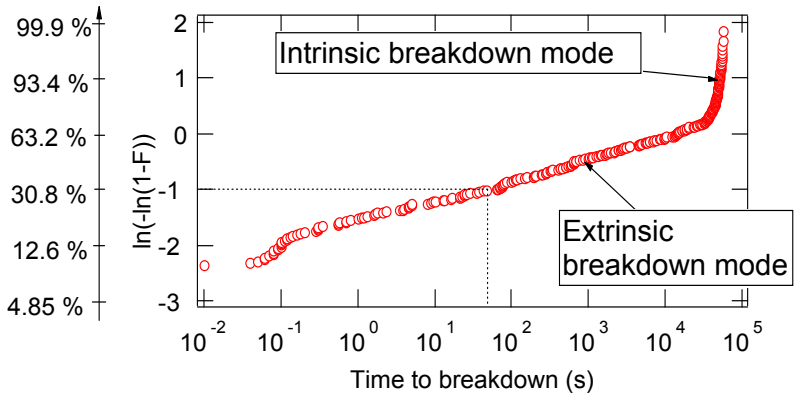
BREAKDOWN STATISTICS



Oxide breakdown (t_{BD}, Q_{BD}) is Weibull distributed

Extrapolation towards low percentile from lognormal distribution yield overoptimistic results !

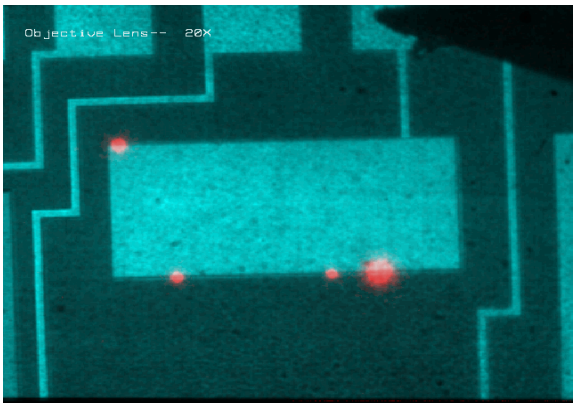
TWO BREAKDOWN MODES



Intrinsic BD = caused by electrical stress-induced defect generation (creation of neutral electron traps)

Extrinsic BD = caused by process-induced imperfections (impurities, roughness, thinning, pinholes,structural weakness)

EXTRINSIC BREAKDOWN



Example of extrinsic breakdown

- Process-induced damage at the gate isolation edge causes multiple breakdowns after continued stress

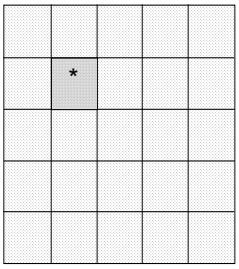
EXTRINSIC RELIABILITY

Influencing factors:

- substrate quality (epi vs Cz substrates)
- crystalline defects in the silicon: stacking faults !
- wafer cleaning procedures
- oxidation procedures (wet, dry, post-oxidation anneal)
- purity of chemicals
- cleanliness of oxidation furnace
- metal contamination (e.g. heating elements in furnace)
- mobile ion contamination (Na)
- photolithographic related defects
- mechanical stress buildup
- post-oxidation processing: e.g. plasma induced damage

 37

AREA DEPENDENCE OF TBD



$\overline{t_{BD,small}} > \overline{t_{BD,large}}$

For $A_1 > A_2$: series rule applies:

$$F_{A_1}(t) = 1 - \prod_n (1 - F_{A_2}(t)) \qquad \text{with } n = \frac{A_1}{A_2}$$

$$\ln(1 - F_{A_1}(t)) = \sum_n \ln(1 - F_{A_2}(t)) = n \times \ln(1 - F_{A_2}(t))$$

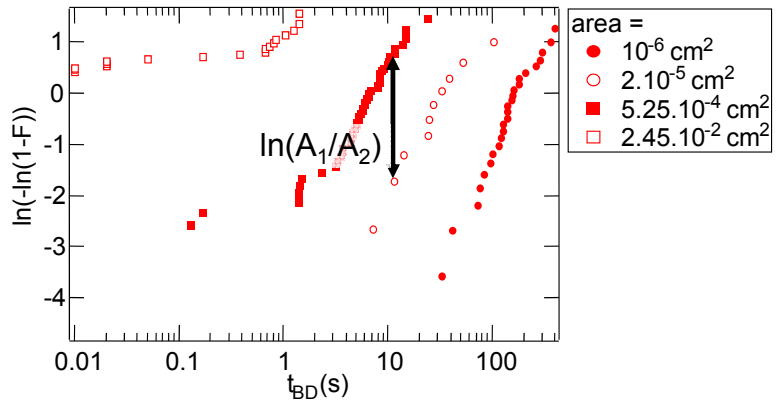
$$\boxed{\ln(-\ln(1 - F_{A_1}(t))) = \ln\left(\frac{A_1}{A_2}\right) + \ln(-\ln(1 - F_{A_2}(t)))}$$

The area effect: changing from A_1 to A2: distribution shift vertically over a distance $\ln(A_1 / A_2)$

The area dependence of breakdown: schematically

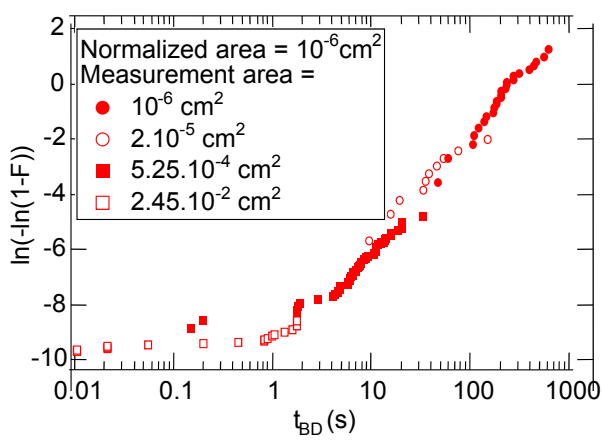
 38

THE AREA SCALING EFFECT



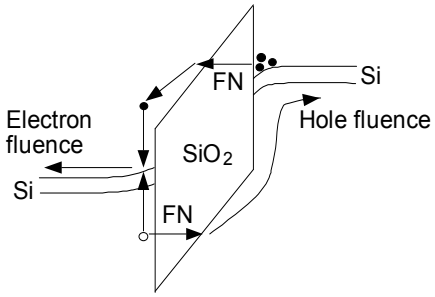
- Changing from A_1 to A_2 gives a vertical shift of $\ln(A_1/A_2)$
- For Weibull: $\eta_1=\eta_2(A_2/A_1)^{1/\beta}$
- Scaling of η is β-dependent
- Extrinsic breakdown can only be measured if gate area is large

THE AREA SCALING EFFECT



- Normalization of the breakdown distribution to a reference area is always possible
- Depending on test structure area different parts of the distribution are measured
- Allows to extract Weibull slope with higher accuracy

BREAKDOWN MODEL



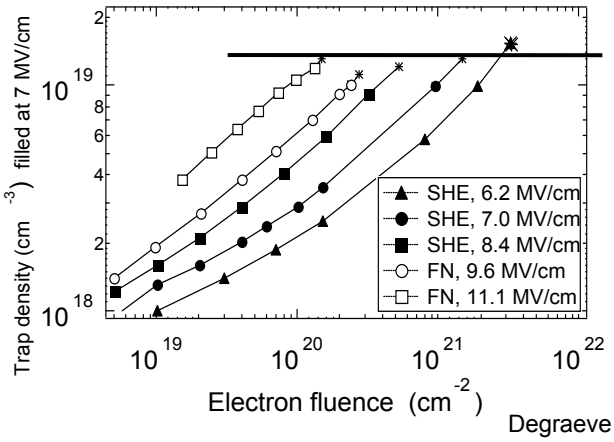
Breakdown model :

- electrons are tunneling
- gain energy in the oxide conduction band
- at anode: energy is transferred to holes

1) anode hole injection model: holes tunnel back and generate traps
2) hydrogen release model: H is released and moves through the oxide, generate traps

At critical trap density: breakdown occurs !

OXIDE DEGRADATION



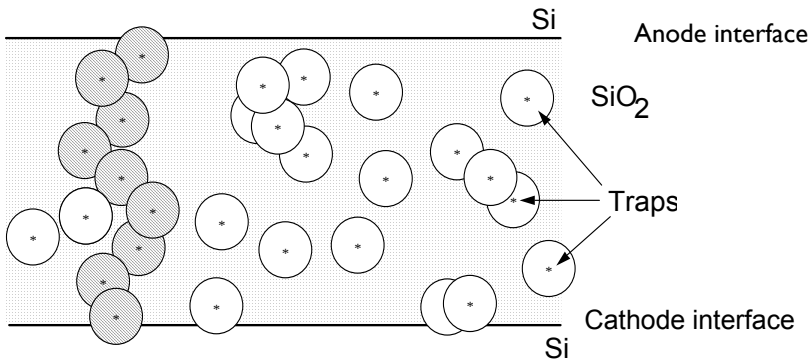
NBD = critical defect density

Decreases with Tox !

Degraeve et al, TED, p. 904 1998

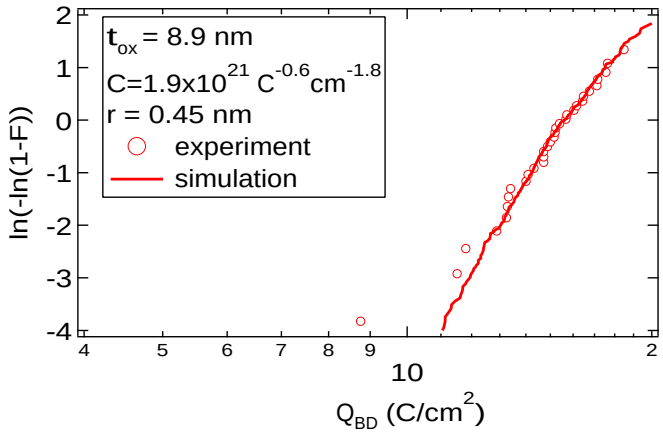
Breakdown occurs when a critical density of neutral electron traps is reached

PERCOLATION MODEL



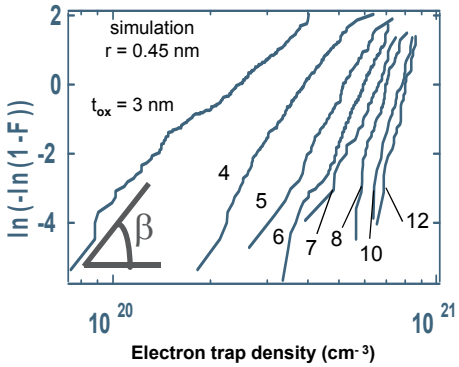
Electron traps are randomly generated in the oxide
Trap is characterized by a sphere with constant radius r
Breakdown when conducting path is formed from anode to cathode
Critical trap density = total number of traps / testvolume

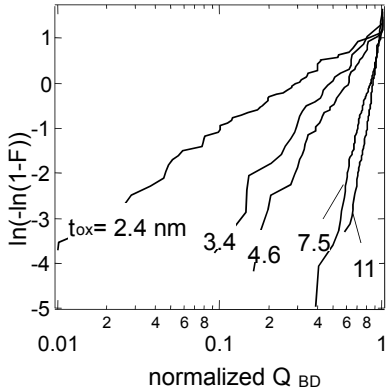
STATISTICAL MODELLING OF BREAKDOWN



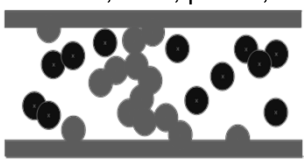
Simulation fits experimental Q_{BD}-distribution very well

STATISTICAL MODELING OF BREAKDOWN



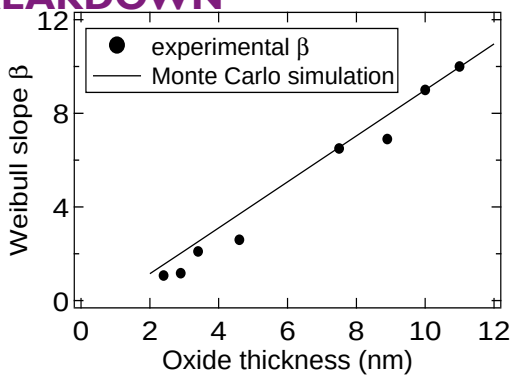


Degraeve et al, TED, p. 904, 1998



Statistics of percolation model explains decreasing Weibull slope (larger spread of t_{BD}) for decreasing oxide thickness

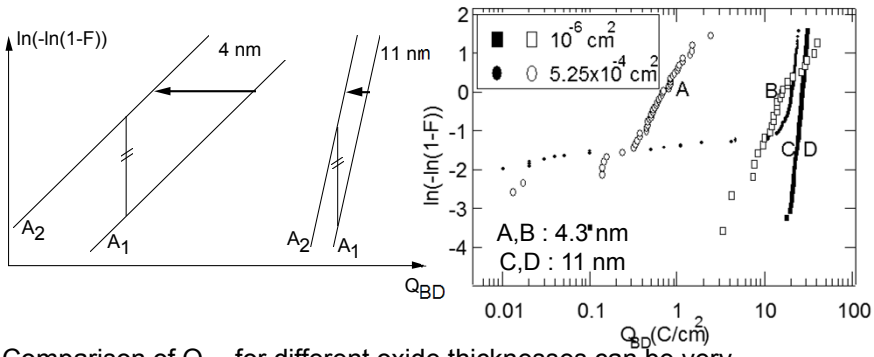
STATISTICAL MODELING OF BREAKDOWN



Degraeve et al, TED, p. 904, 1998

The decrease of the Weibull slope ß for thin oxides is an **intrinsic statistical property** of the degradation mechanism

CHANGE IN AREA DEPENDENCE



Comparison of Q_{BD} for different oxide thicknesses can be very misleading !!

Thick oxide: large Weibull slope : small area dependence

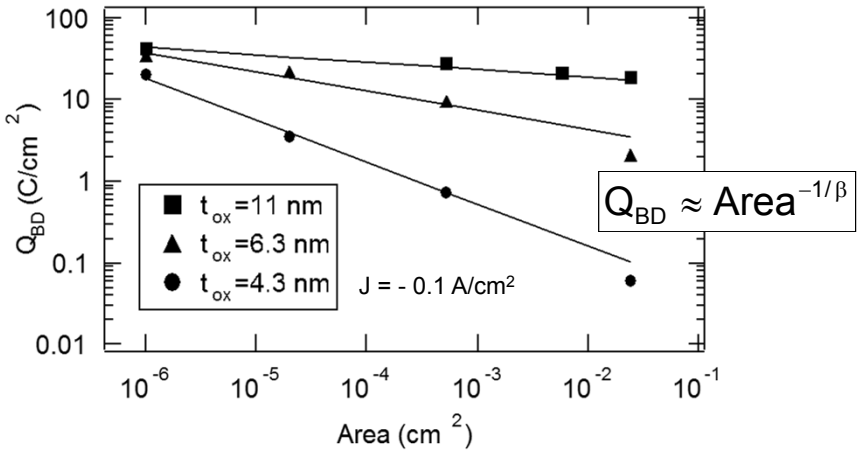
Thin oxide: small Weibull slope: large area dependence

$$Q_{BD,1} = Q_{BD,2}\left(\frac{A_2}{A_1}\right)^{\frac{1}{\beta}}$$

Nigam et al. IRPS 1998

 47

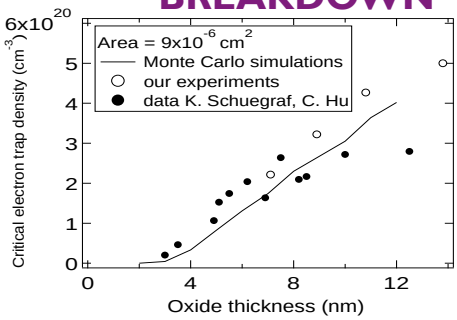
AREA DEPENDENCE OF Q_{BD}



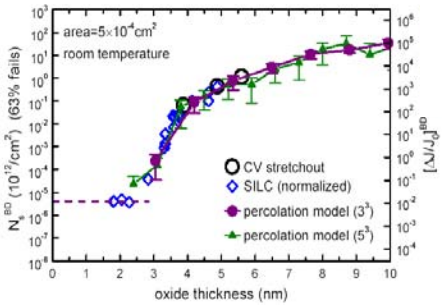
Between 10^{-6} and 0.1 cm^2 lifetime drops with **3-4 orders of magnitude** for 4 nm oxides, only **factor of 2** for 11 nm oxides

 48

STATISTICAL MODELING OF BREAKDOWN



Degraeve et al., TED 1998



Stathis et al., JAP, 1999

Critical electron trap density (N_{BD}) is reduced with oxide thickness scaling, wich is also explained by percolation model

Trap size: 0.9 nm diameter (IMEC) to 2.5 nm (IBM)

imec © IMEC 2016 49

FIELD ACCELERATION MODELS

E-model

$$t_{BD} \approx \tau_0 . \exp(-\gamma \cdot E_{ox})$$

Breakdown is not fluence driven

Based on Thermochemical model

Worst case ?

1/E-model

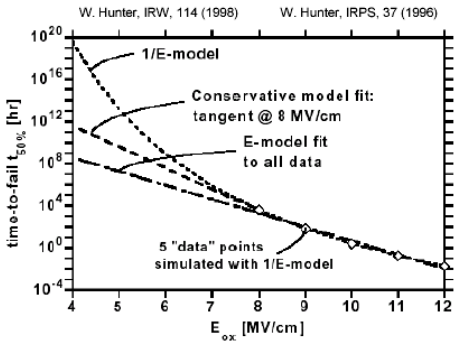
$$t_{BD} \approx \tau_0 . \exp\left(\frac{G}{E_{ox}}\right)$$

Breakdown is fluence driven

Based on Anode hole injection

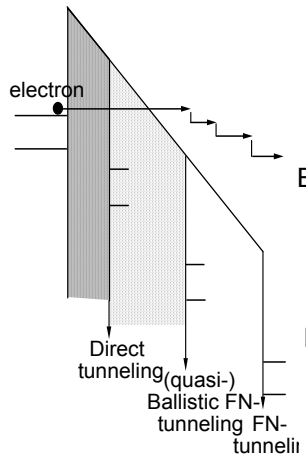
Very optimistic- 1/E probably not valid at lower voltages

W. Hunter, IRW, 114 (1998) W. Hunter, IRPS, 37 (1996)



50

IMPACT OF SCALING ON ACCELERATION MODEL



Decreasing t_{ox}:

FN tunneling

⇩

Ballistic tunneling

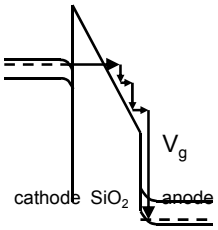
⇩

Direct tunneling

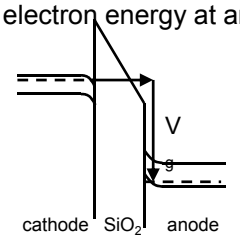
E_{ox}-dependence

⇩

V_g-dependence



Thick oxide: E_{ox} determines electron energy at anode



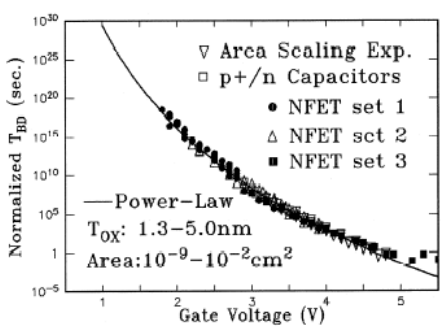
Electron energy at the anode determines oxide degradation and breakdown

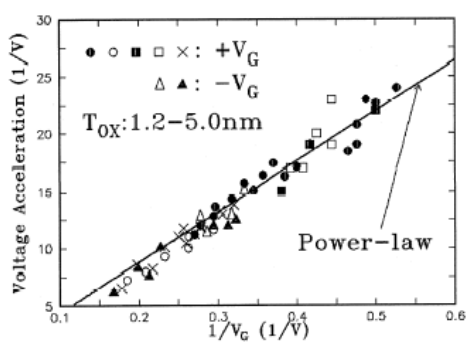
Thin oxide: V_G determines electron energy at anode

VOLTAGE ACCELERATION MODEL

Power law model
- acceleration increases at low Vg
- power factor n ~ 44

$$t_{BD} \approx Vg^{-n}$$





E. Hu et al, TED p 2244, 2002

PRINCIPLE OF EXTRAPOLATION TO SPECIFIED CONDITIONS

63% TBD at test structure, test voltage and test temperature

Temperature acceleration **NO** Arrhenius-law
Use spec. T = test T to avoid acceleration issue

63% TBD at test structure, test voltage and spec. temperature

Voltage acceleration to operating voltage
Use power law $t_{BD} \sim V_G^n$

63% TBD at test structure, operating voltage and spec. T

Area scaling law to total gate oxide area on chip

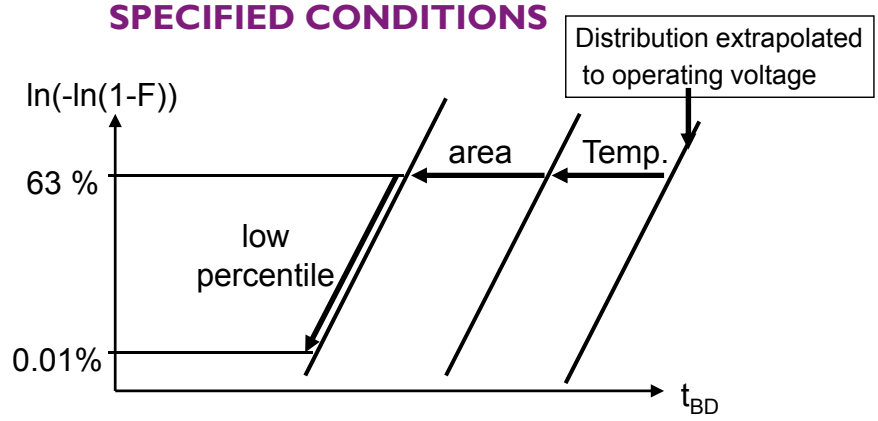
63% TBD at spec. area, operating voltage and spec. T

Weibull distribution

low percentile TBD at spec. area, operating voltage and spec. T

 53

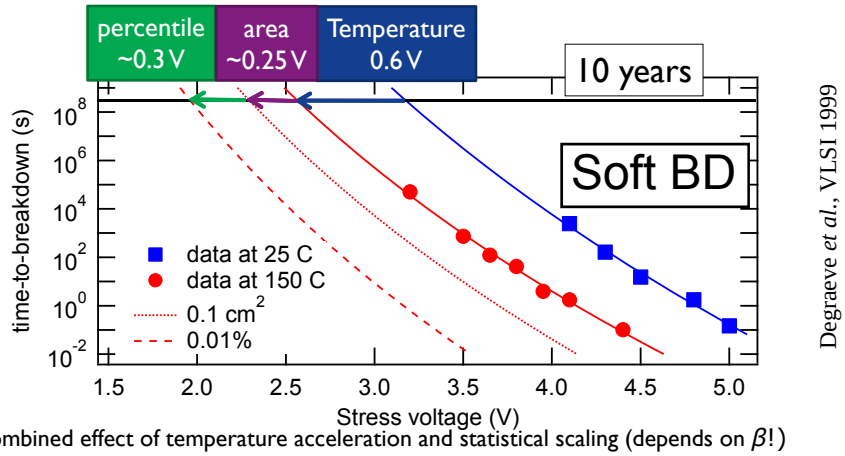
PRINCIPLE OF EXTRAPOLATION TO SPECIFIED CONDITIONS



- Spec : 0.01% failures at 0.1 cm2 after 10 years
- DC operation at operation voltage and temperature
- Area scaling and percentile scaling require correct Weibull slope β

 54

DETERMINATION OF THE MAXIMUM APPLICABLE GATE VOLTAGE



Degraeve *et al.*, VLSI 1999

Combined effect of temperature acceleration and statistical scaling (depends on β!)

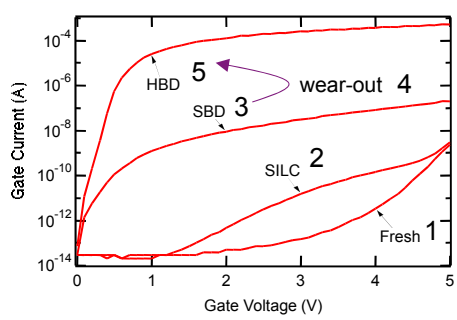
This extrapolation is only valid for soft breakdown

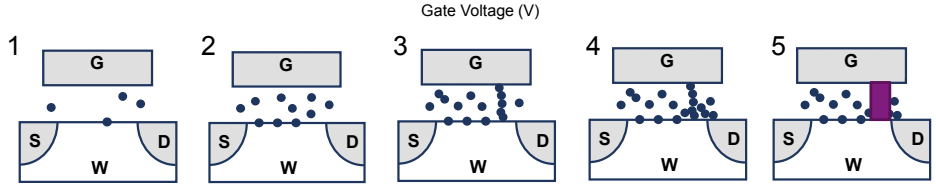
Voltage power-law more accurate than exponential also in high-k

Wu & Suñe, TED 2009

imec © IMEC 2016 55

PHASES OF GATE OXIDE BREAKDOWN

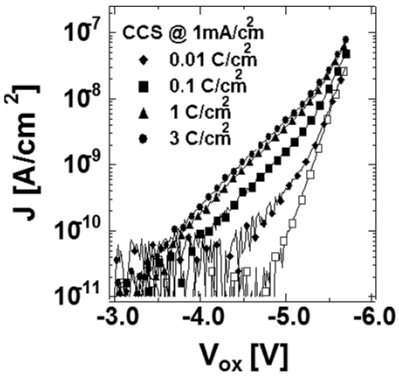


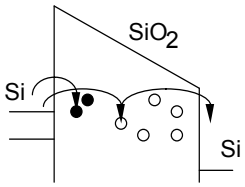


Electrical stress = Additional gate oxide leakage paths (TDDB)

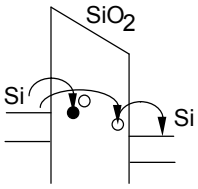
imec © IMEC 2016 56

STRESS-INDUCED LEAKAGE CURRENT





Thick oxide (>8nm): transient dominant



Thin oxide (<8nm): steady-state dominant

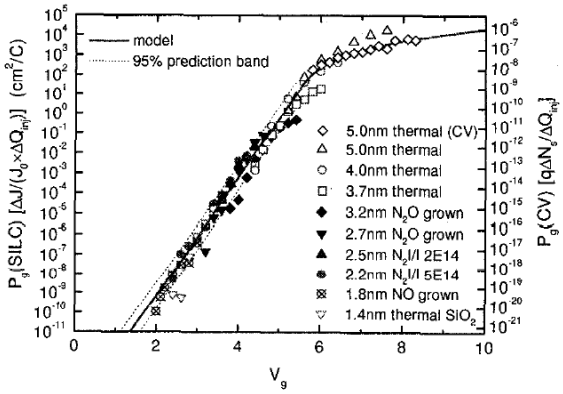
SILC: macroscopically uniform over the area

- tunneling mechanism = trap assisted tunneling

imec © IMEC 2016 57

TWO COMPENSATING EVOLUTIONS IN ULTRA-THIN OXIDE SILC

(trap generation rate)



(Stathis et al, IEDM 1998)

Effect 1: trap generation rate drastically drops (figure)

- Less conductive paths through the oxide

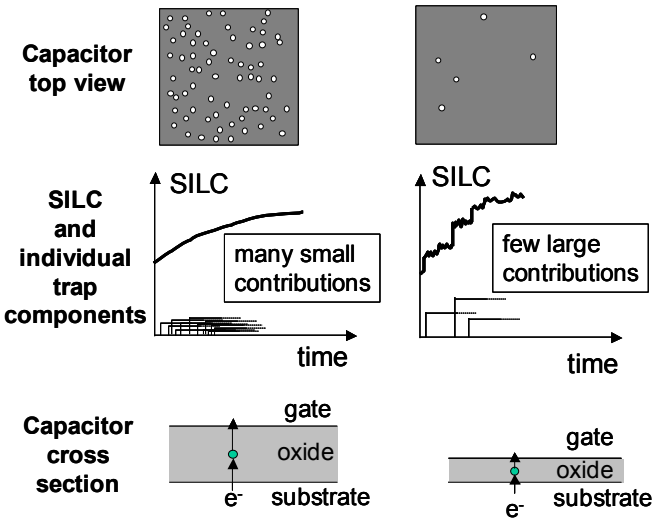
Effect 2: conductivity per trap increases drastically

- Tunnel distance decreases and current rises exponentially
- Each trap contributes more to the total SILC

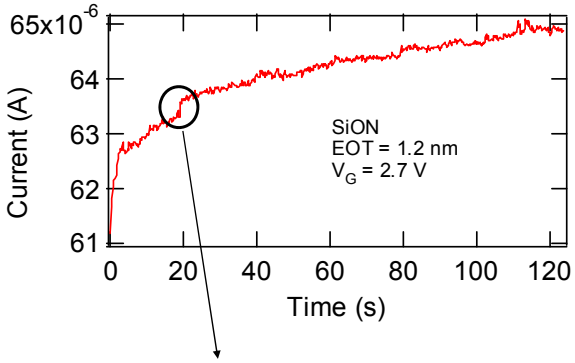
imec © IMEC 2016 58

THE CHANGING APPEARANCE OF SILC

Thick / large capacitor thin / small capacitor

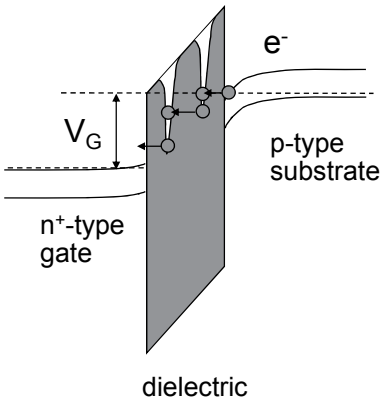


DISCRETE SILC EVENTS IN VERY THIN LAYERS

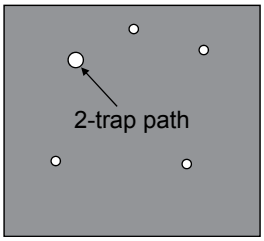


Abrupt current increase of about 250nA
= creation of single trap conduction path
= 'discrete' SILC event
This is NOT a breakdown

TWO-TRAP CONDUCTION PATH



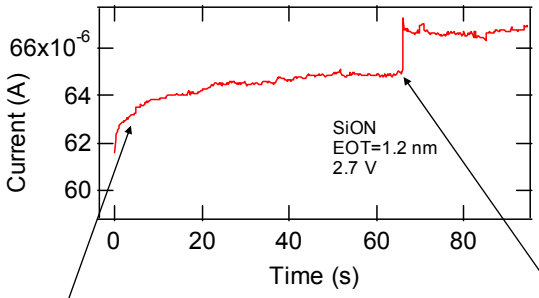
capacitor top view



Percolation path with trap-assisted tunneling

- this is **Anomalous Stress-Induced Leakage Current** = a-SILC (non-volatile memories) (Okada et al. IEDM 2001, Degraeve et al., IEDM 2001)
- this is **Micro-Breakdown** (Cellere et al. TED 49(8), 2002) or **pre-Breakdown** (Degraeve et al, IEDM 2001)

THIN OXIDE: MICRO-BREAKDOWNS



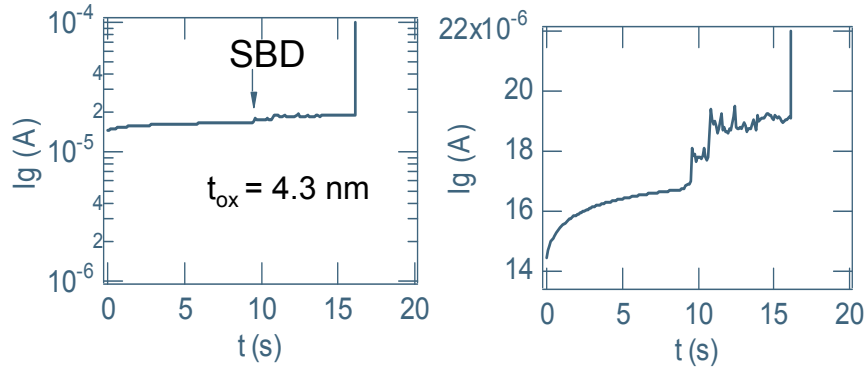
single trap conduction path

different statistics
different I_G-V_G

2-trap conduction path

- No significant change of the gate current noise after micro-BD
- Is this a breakdown or not?
  - Application dependent specifications needed

SOFT BREAKDOWN



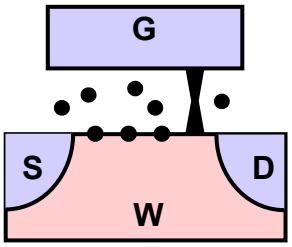
Soft breakdown: localized at one spot

Soft breakdown makes classical detection of breakdown problematic: alternatives have been introduced, based on current noise increase

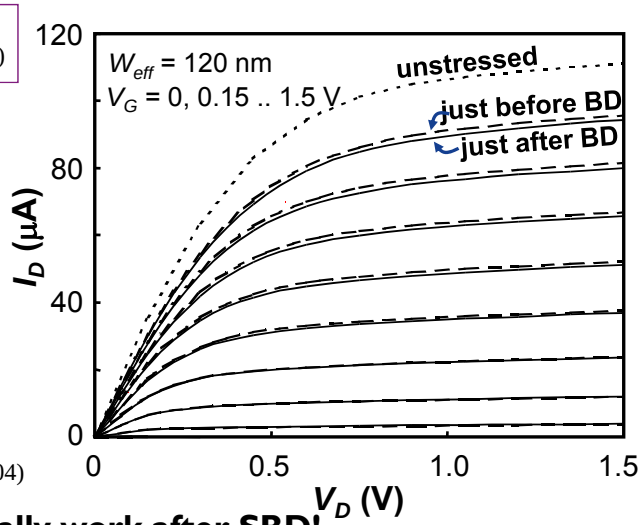
 63

NO SIGNIFICANT EFFECT ON FET CHARACTERISTICS AT THE MOMENT OF SBD

Already in
Weir *et al.*, IEDM, p. 73 (1997)



Kaczer *et al.*, IRPS, p. 79 (2004)



Circuits will generally work after SBD!

Gerrer *et al.*, ESSCIRC 2009

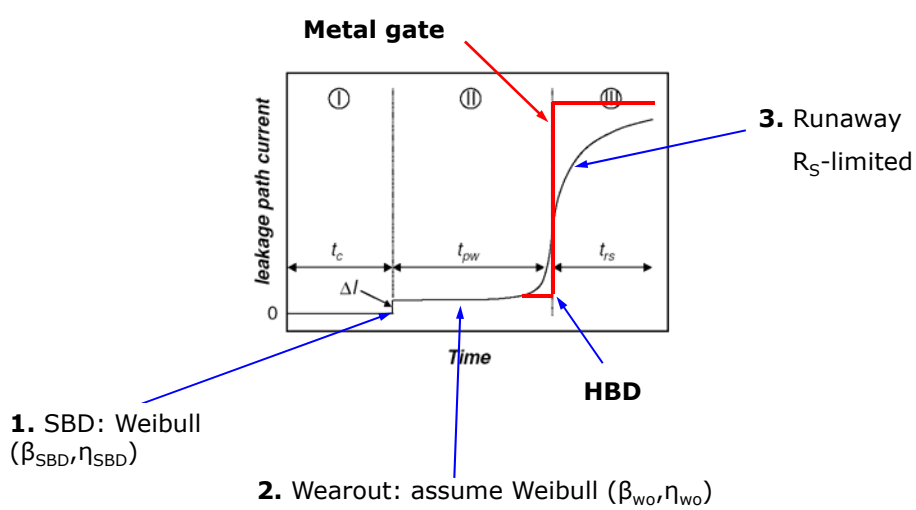
 64

OVERVIEW

NAME	Conduction model	physical damage	Observable properties
SILC (=A-mode SILC)	trap-assisted tunneling	single trap	- no noise change - RTS behavior
Micro BD (=pre-BD, anomalous SILC)	trap-assisted tunneling	cluster of two traps	- no noise change - RTS behavior
Soft BD (=quasi BD, partial BD, B-mode SILC)	localized conduction over lowered barrier (quantum point model)	percolation path with limited wear out	noise increase
Hard BD	resistor (+diode)	percolation path with thermal damage	very large current increase

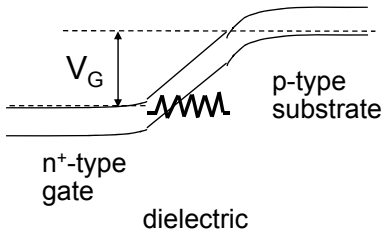
 65

PHASES OF DEGRADATION AND WEAR OUT IN THIN OXIDES

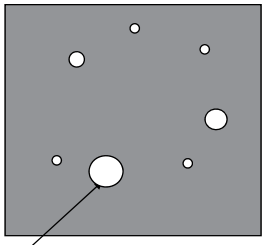


 66

CONDUCTION PATH + THERMAL DAMAGE



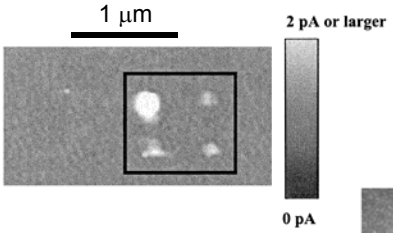
capacitor top view



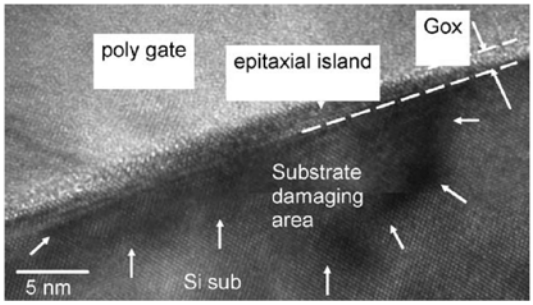
hard breakdown

- Mass transport and Si regrowth in the breakdown spot *(Lei Jun Tang et al., TDMR 4(1), 2004)*
- Localized current flow through resistor (+diode) *(Kaczer et al. TED 49(3) 2002)*
- This is a **hard breakdown**

HARD BREAKDOWN AND MASS TRANSPORT CONFIRMED BY AFM AND TEM

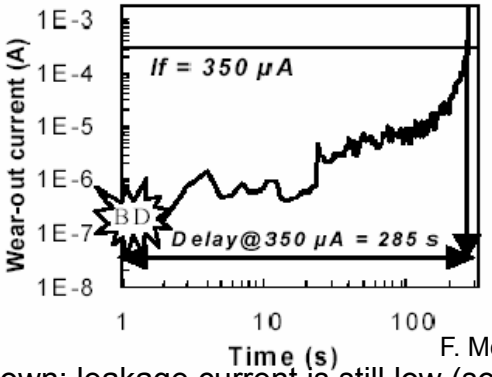


Porti *et al.*, TED **50**, p. 933 (2003)



Tang *et al.*, TDMR **4**, p. 38 (2004)

SEARCHING MORE RELIABILITY MARGIN



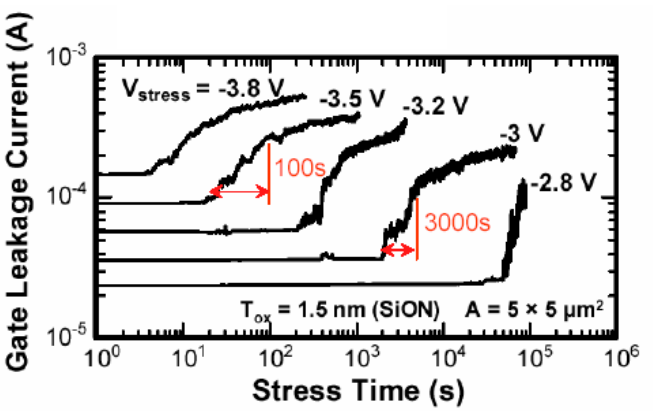
F. Monsieur et al, IRPS2002

At breakdown: leakage current is still low (soft breakdown)

Leakage path is wearing out as a function of time

Delay time is available until the leakage current reaches unacceptable levels

PROGRESSIVE BREAKDOWN

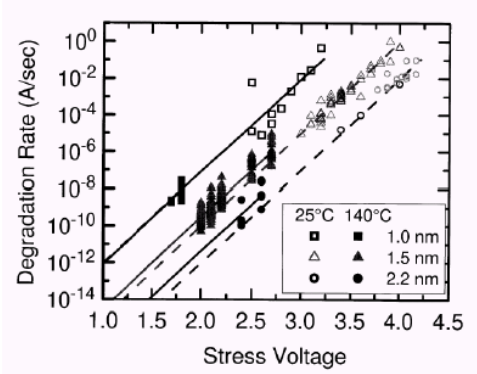


Hosoi et al, IEDM p. 155, 2002

Wearout of breakdown path progresses gradually, rate is lower at low stress voltages

IMPACT OF PROGRESSIVE BD ON RELIABILITY MARGIN

DR≡slope of I(t) between 10μA and 100 μA



B. Linder at al, EDL 2002

Post-SBD degradation rate depends on voltage:

>1mA/s at 4V

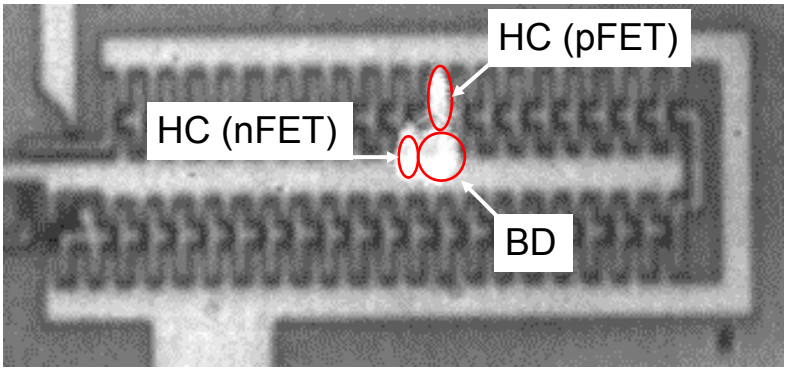
< 1nA/s at 2V

Extrapolations to 10fA/s at 1.2V

More then 10 years to grow BD-path from SBD to >10 μA at 1.2V: gives us again reliability margin

imec 72

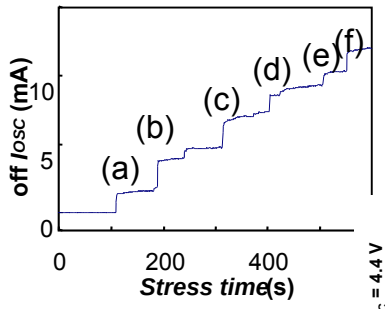
OXIDE BD IS OBSERVABLE WITH EMISSION MICROSCOPE

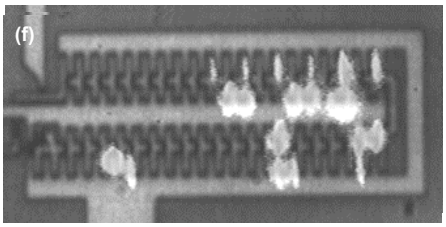


"Satellite" spots are observed, identified as hot carrier emission by spectral and SPICE analysis

imec 73

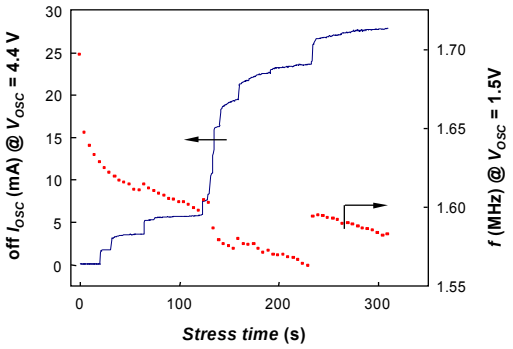
RING OSCILLATOR BREAKDOWN



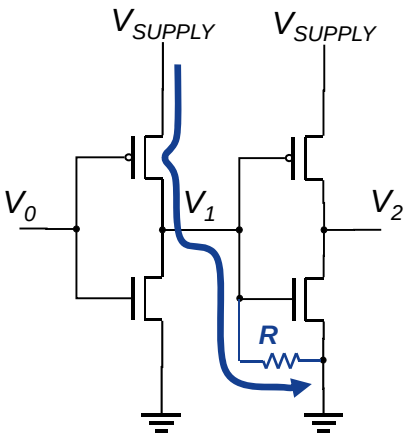


Logical functions are maintained even after many FET oxide (hard) breakdowns

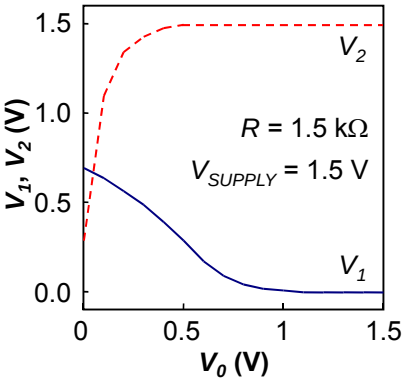
Kaczer et al, IEDM 2000



CIRCUIT OPERATES DOWN TO RBD ~ 1KΩ



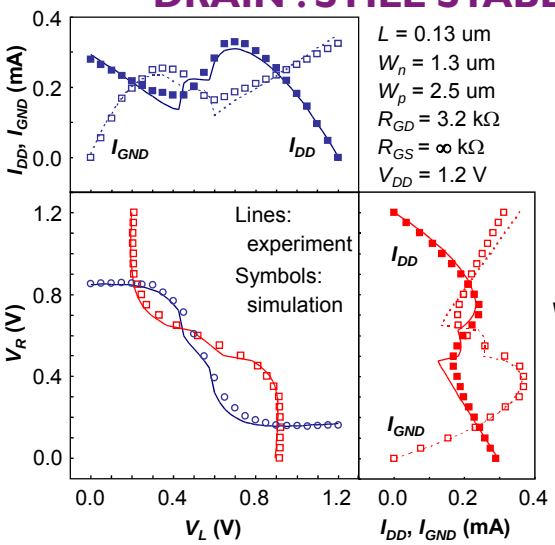
Border case



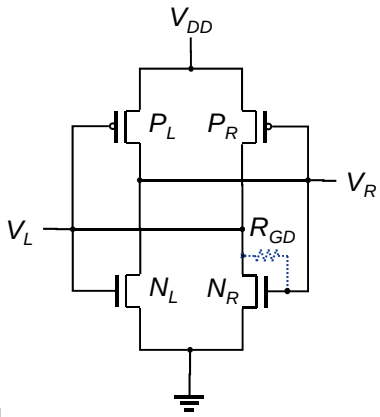
For Rbd > 1.5kΩ logic function is maintained

Soft BD has ~ MΩ resistance → BD effect much smaller

WIDE SRAM AFTER HBD AT NFET DRAIN : STILL STABLE



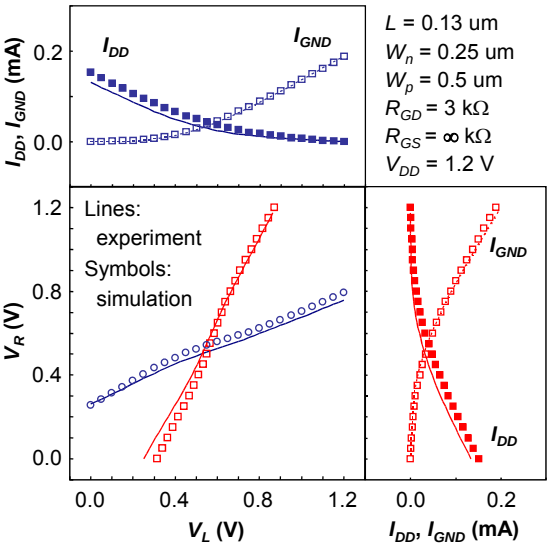
L = 0.13 um
W_n = 1.3 um
W_p = 2.5 um
R_{GD} = 3.2 kΩ
R_{GS} = ∞ kΩ
V_{DD} = 1.2 V



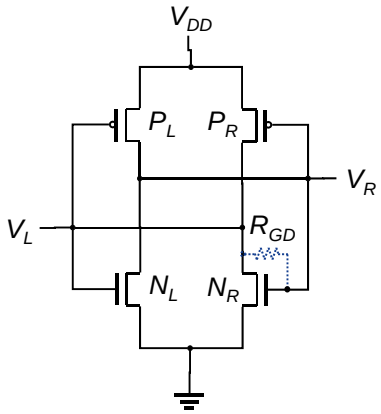
Kaczer et al,

 76

"NARROW" SRAM AFTER HBD : DISABLED!

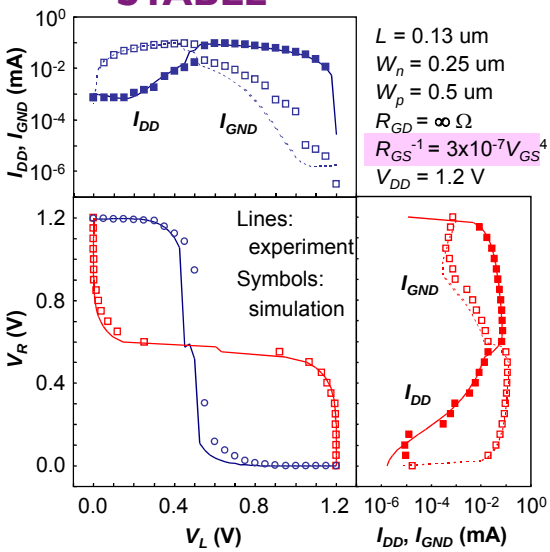


L = 0.13 um
W_n = 0.25 um
W_p = 0.5 um
R_{GD} = 3 kΩ
R_{GS} = ∞ kΩ
V_{DD} = 1.2 V

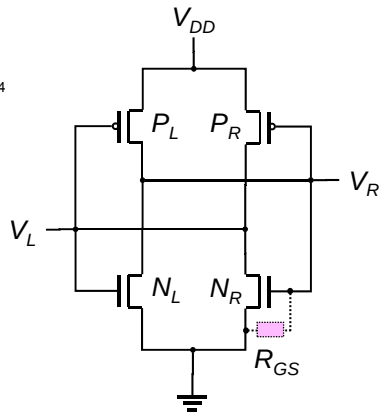


 77

"NARROW" SRAM AFTER SBD : STABLE



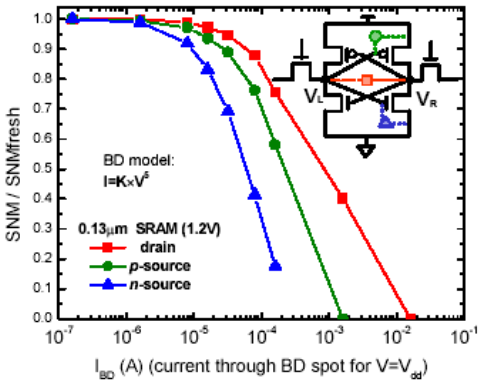
L = 0.13 um
W_n = 0.25 um
W_p = 0.5 um
$R_{GD} = \infty\ \Omega$
$R_{GS}^{-1} = 3\times10^{-7} V_{GS}^{4}$
V_{DD} = 1.2 V



Good news : SBD is expected prevalent failure mode

imec 78

EFFECT OF BD ON SRAM STATIC NOISE MARGIN



Rodriguez et al, EDL 2002

50% reduction in Static Noise Margin (SNM) for BD current >50μA

Reliability specification becomes strongly dependent on application: requires interaction with designers !

imec © IMEC 2016 79

OUTLINE

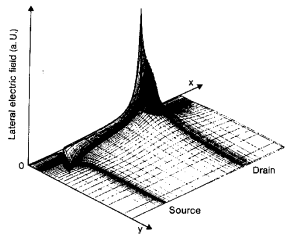
1. Introduction
2. Basic reliability concepts
3. Time-dependent Dielectric Breakdown (TDDB)
4. Hot carrier degradation
   - Hot carrier injection
   - Effects of hot carrier injection
   - Acceleration models and examples
   - Dynamic degradation
5. Bias-Temperature Instability (NBTI)

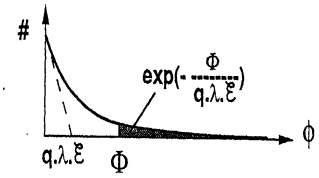
imec © IMEC 2016 86

DEFINITION OF "HOT CARRIERS"

"Hot carriers" are channel electrons and/or holes with high energy

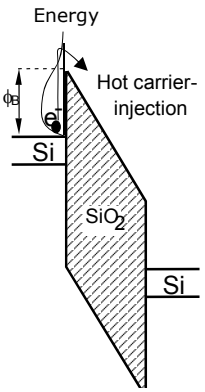
- Generation: high lateral electric field at drain side
- The distribution of the carrier energy can be approximated by a Fermi-Dirac or Maxwell-Boltzman distribution with a high energy tail (high electron temperature)
- Hot carriers are always present when a transistor operates in saturation!

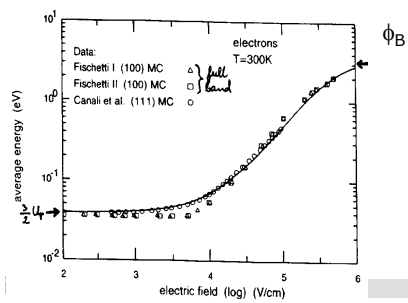




imec © IMEC 2016

HOT CARRIER INJECTION

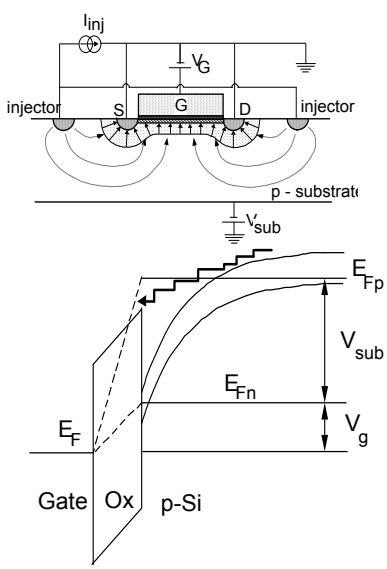




- Hot carrier = carrier that has gained large energy in a **high electric field**
- Hot carrier is **NOT** in equilibrium with the crystal: energy distribution is NOT Maxwell-Boltzmann distribution
- This means that hot carriers can be injected at much **smaller oxide fields** then tunneling injection
- Once the electrons are in the oxide conduction band they travel with a relatively high mobility to the anode

88

SUBSTRATE HOT ELECTRON INJECTION



- Electrons injected from an external injector junction or by illumination are heated in depletion layer and injected into the gate
- Separate control of oxide current density, oxide field and silicon field (i.e. carrier field)
  - Oxide field controlled by V_g
  - Electron energy controlled by V_{sub}
  - Gate current controlled by substrate current
- Allows to measure oxide degradation and breakdown at fields considerably lower than 9MV/cm (i.e. closer to normal operation conditions)
- - Use p-channels for hole injection

imec © IMEC 2016 89

HOT CARRIER INJECTION

High-energetic carriers are generated in the high lateral electric field at the drain side of the MOS transistor

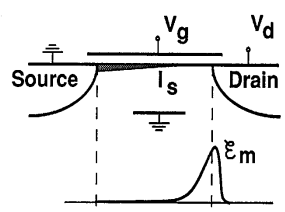
$$E_m = \frac{V_d - V_{dsat}}{l}$$

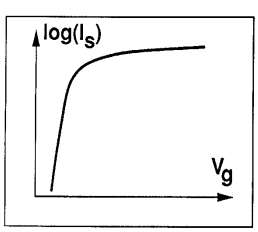
$$V_{dsat} = \frac{(V_g - V_t) \times L_{eff} \times E_{sat}}{(V_g - V_t) + L_{eff} \times E_{sat}}$$

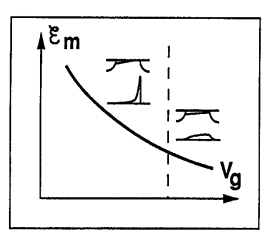
$$l = 0.22 \times t_{ox}^{1/3} \times x_j^{1/m}$$

$$l = 0.017 \times t_{ox}^{1/8} \times x_j^{1/3} \times L_{eff}^{1/5}$$

HOT CARRIER INJECTION

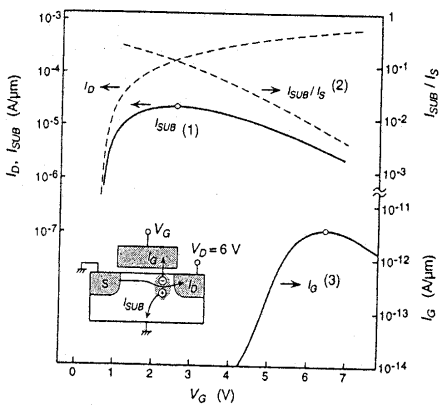


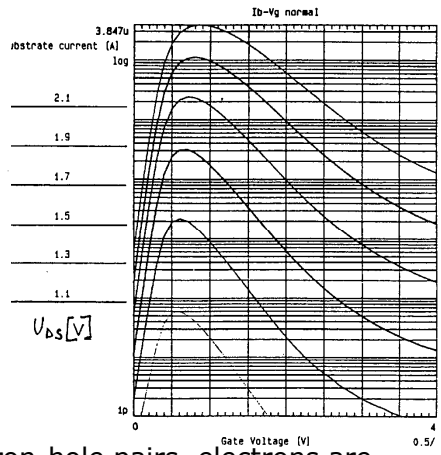




Large electric fields at drain lead to high energetic carrier generation

HOT ELECTRON CURRENTS





Impact ionization causes electron-hole pairs, electrons are flowing to the drain, holes are flowing to the substrate
Hot electron generation and injection causes gate current

SIMPLIFIED EQUATIONS SUBSTRATE CURRENT

Substrate current: $$I_{sub} = I_s \cdot C \cdot \exp\left(-\frac{\phi_i}{q\lambda_e E_m}\right)$$

Multiplication factor: $$M = \frac{Isub}{Is} = C \cdot \exp\left(-\frac{\phi_i}{q\lambda_e E_m}\right)$$

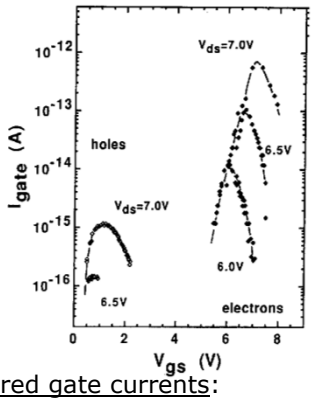
$$\ln\left(\frac{Isub}{Is}\right) = \ln C - \frac{\phi_i}{q\lambda_e E_m} = \ln C - \frac{l \cdot \phi_i}{q\lambda_e (V_d - V_{dsat})}$$

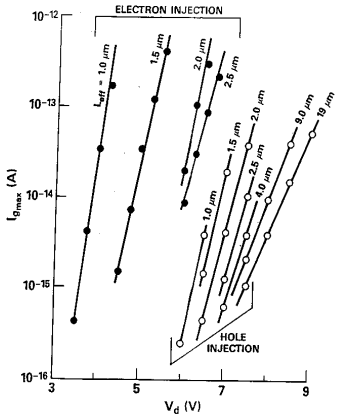
Multiplication factor Isub/Is is a measure for the lateral electrical field E_l

ϕ_i = impact ionization energy threshold (typically 1.5-1.6 eV)
λ_e = mean free path of electron in Si (typically 9.2 nm), T-dependent

for increasing T: λ_e becomes smaller: less hot carriers generated !

HOT CARRIER INJECTION



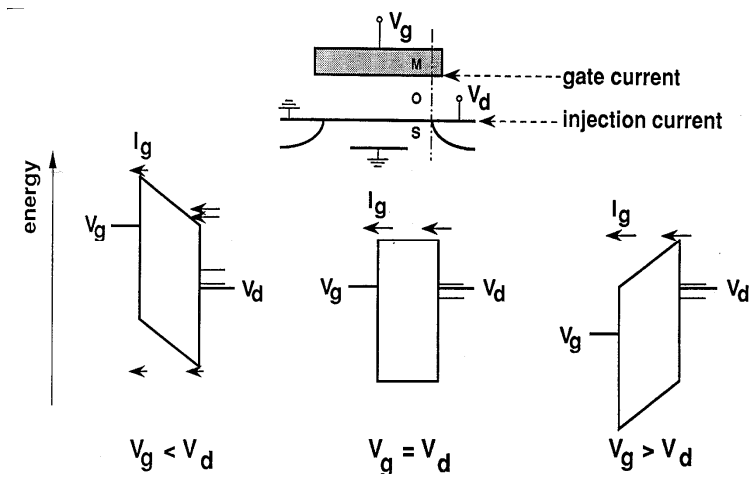


Measured gate currents:
At large V_g (~V_d) :
negative gate current: electron injection

For small V_g (near V_t) :
positive gate current: hot hole injection

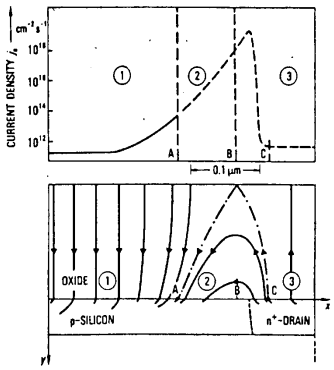
Currents scale exponentially with drain voltage

HOT CARRIER INJECTION

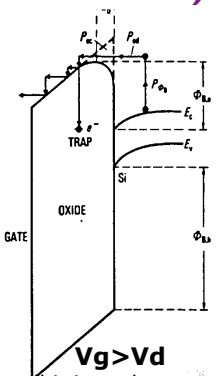


Injection current vs. gate current: influence of gate voltage

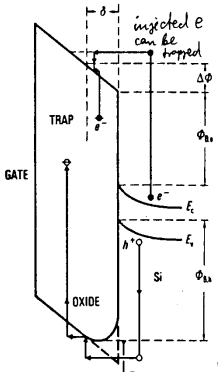
HOT CARRIER INJECTION: ROLE OF OXIDE FIELD (GATE VOLTAGE)



When Vg<Vd: repulsive field for electrons exists at the drain
Large injection current is repelled back into the substrate

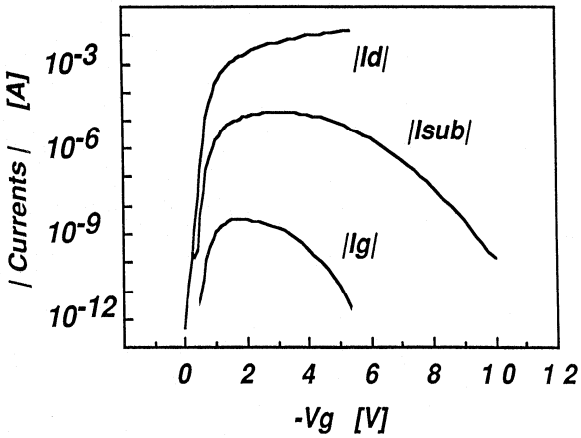


Vg>Vd
all injected electrons are traveling to the gate: e-current
lateral field is usually too low for hole injection, holes are pushed back into channel



Vg<Vd
most injected electrons are pushed back into channel: no e-current
all injected holes will travel to the gate: h-current

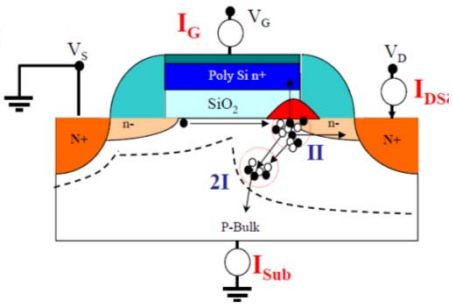
HOT CARRIER INJECTION FOR PMOS

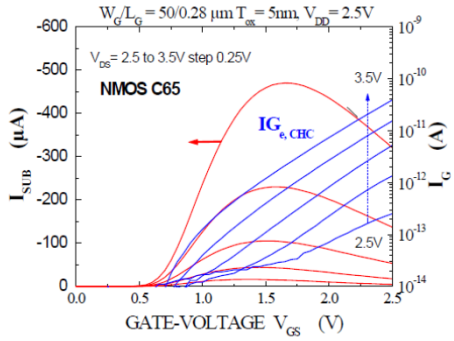


Drain, substrate and gate currents for a pMOS device

HOT CARRIER BASICS

A. Bravaix, IRPS Tutorial 2014





Substrate current is determined by product of drain current and multiplication current

Measured gate current is determined by generated hot carriers and attractive or repelling oxide field at the drain

Both electron and holes can be injected, depending on the oxide (gate voltage) and lateral silicon (drain voltage) fields.

HOT CARRIERS (HC) CAUSE MANY EFFECTS

HC generate electron-hole pairs by impact ionization

- carrier energy > 1.6eV
- generated current is measured as a bulk current (I_b)

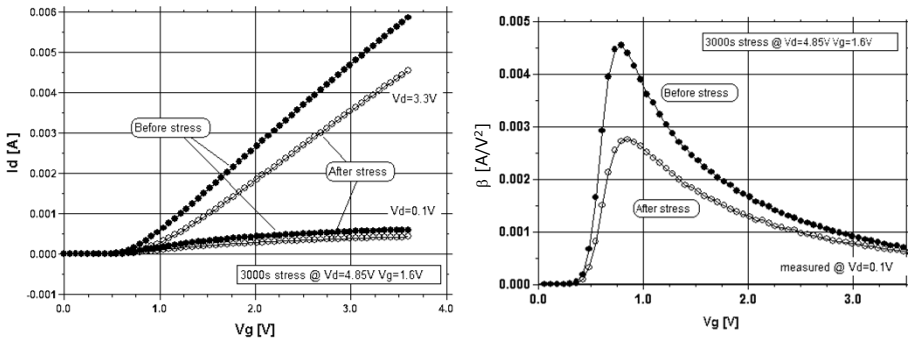
HC can be injected into the gate oxide

- damage to the channel - gate oxide interface and electron trapping in the gate oxide → transistor degradation
- Carrier energy > 3.1eV (for electrons), > 4.8eV (for holes)
- $I_{inj} \sim I_b$
- Can also be measured as I_g (under specific conditions)

HC cause also other phenomena

- Light emission
- Secondary effects (e.g. too high I_{sub} can cause CMOS latch-up, …)

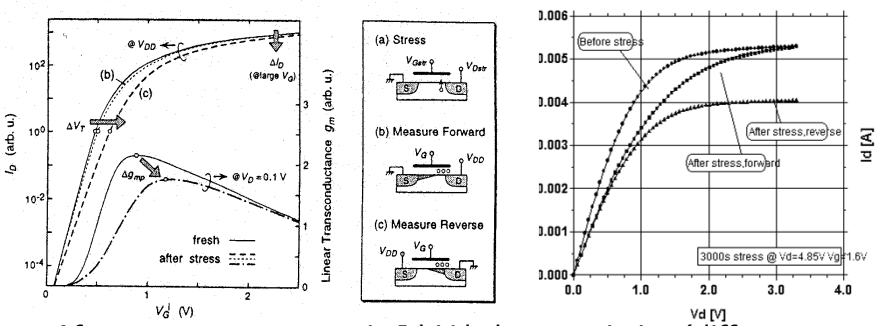
INFLUENCE ON NMOS PERFORMANCE



Guido Groeseneken

Change in Id-Vg characteristics and transconductance

INFLUENCE ON NMOS PERFORMANCE

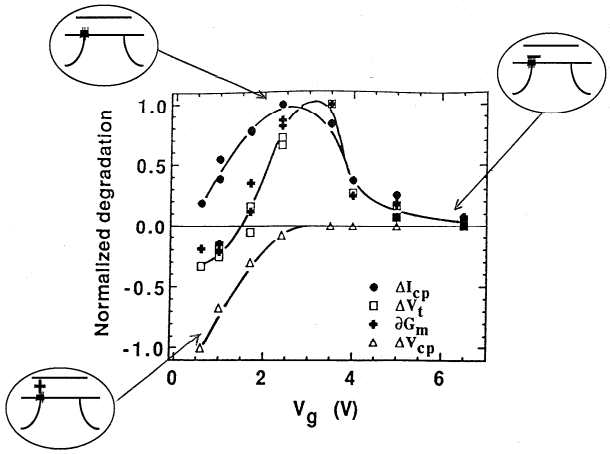


After stress assymmetric Id-Vd characteristics (different when S-D are reversed)

- when damage is located at drain side: damaged area is depleted in saturation
- S-D reversed: damage is located at source side, influence I-V characteristic for all voltage

In linear region: characteristics are symmetrical but degraded

NMOS DEGRADATION



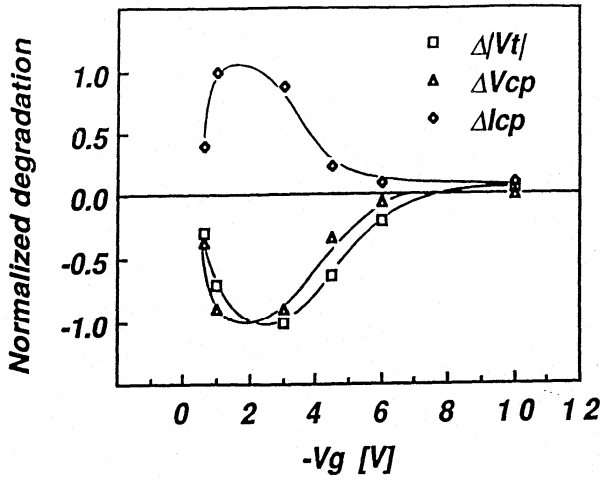
Leff = 1.5 µm
tox = 21 nm

stess :
Vd = 6.5 V
time = 3600 s

Maxima :
ΔIcp : 250 %
ΔVcp : 1.24 V
ΔVt : 15 mV
∂M : 59 %

Gate voltage dependence of the nMOS hot carrier degradation

PMOS DEGRADATION



Gate voltage dependence of hot carrier degradation
for p-MOSFET's

INFLUENCE ON PMOS PERFORMANCE

Fixed negative oxide charge gives rise to a channel shortening effect (magnitude dependent on short channel effect) ⇨ increase of drain current

Interface trap generation causes a decrease of I_d

Since $\lambda_e > \lambda_h$ and because of smaller electric fields, hot-carrier degradation in pmos normally is no problem.

For technologies down to 0.5μm, the channel shortening dominates and screens the effect of D_{it}-generation.

For deep-submicron technologies, the effect of interface trap generation starts to be visible.

imec 104

HOW TO DEAL WITH HC DAMAGE?

Hot carriers are always generated when a transistor operates in saturation

- Hot carrier damage cannot be avoided! It can only be limited.

HC damage is not allowed to affect circuit operation during the lifetime of the product

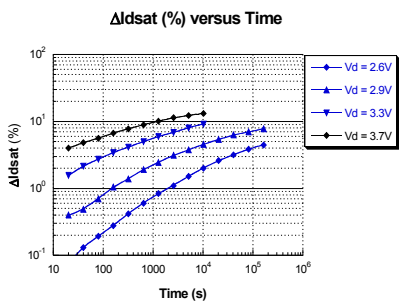
- Specification to guarantee this (simplified).
  - $\Delta Id_{sat} < 10\%$
  - After one year of DC operation
  - At Vd = Vdd + 10%
  - "HC lifetime for the parameter Id_{sat} must be one year under worst case operating conditions"
- This specification has to be met by every individual transistor on the chip.
- This specification is validated by many years of practice.

imec 105

HOW IS THE HC LIFETIME MEASURED?

Accelerated Stress

- HC damage is proportional to the amount of hot carriers
- higher Vd = more hot carriers → the lifetime is lower at higher Vd
  - C018 example:
  - # hot electrons (Vd = 3.5V) ≈ 1e6 # hot electrons (Vd = 2.0V)
- measurement times per transistor: 20min – 4 days, typically 3 hours



 106

ACCELERATION MODELS

Degradation law:

$$\Delta N_{it}(t) = C_1 \bullet \left[\frac{I_d}{W} \cdot t \cdot \exp\left(-\frac{\phi_{it,e}}{q\lambda_e E_m} \right) \right]^n$$

Multiplication factor:

$$M = \frac{I_{sub}}{I_d} = C_2 \cdot \exp\left(-\frac{\phi_i}{q\lambda_e E_m} \right)$$

$$\frac{\tau I_d}{W} = C_3 \cdot \left(\frac{I_{sub}}{I_d} \right)^{-\phi_{it,e}/\phi_i} = C_3 \cdot M^{-m}$$

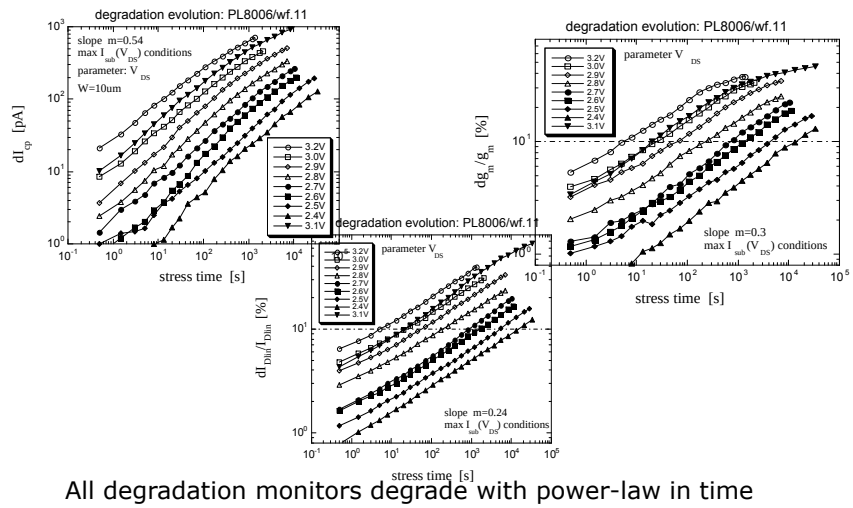
Model of Hu et al.

$$\tau = C_4 \cdot \exp\left(\frac{B}{V_d} \right)$$

Model of Takeda et al.

 107

0.18 μm DEGRADATION



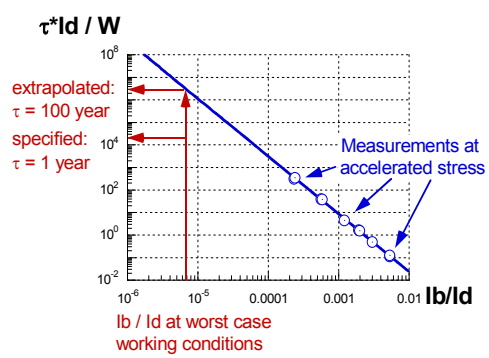
All degradation monitors degrade with power-law in time

$\Delta I_{Dlin}/I_{Dlin}=a*t^m$, with m=0.7 to 0.3

THE HC LIFETIME AT WORK CONDITIONS IS EXTRAPOLATED FROM THE ACCELERATED STRESS

Model of Hu

- Hu plot
  - **X-axis: Ib / Id**
  - Ib ~ # hot carriers
  - Id ~ # available carriers
  - **Y-axis: τ * Id / W**
  - τ = lifetime (s)
  - W = transistor width (μm)



- Power Law

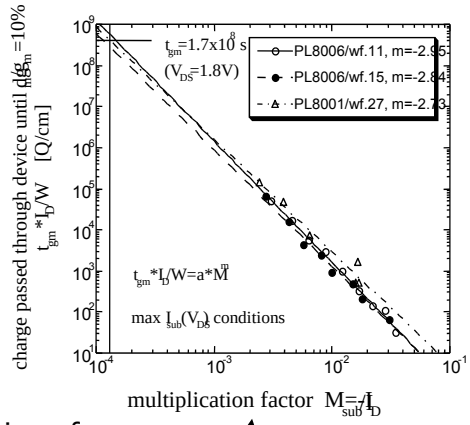
$$\frac{\tau.Id}{W}=C.\left(\frac{Ib}{Id}\right)^{-\phi_{it,e}/\phi_i}$$

- Slope $-\phi_{it,e}/\phi_i$ corresponds to the energy needed
- to create an interface trap
- $\phi_{it,e}$ = energy needed to create an interface trap
- ϕ_i = energy needed to create an electron-hole pair

LIFETIME PLOT

A more "physically" based lifetime evaluation procedure

$$\frac{\tau . I_d}{W} = C \left[\frac{I_{sub}}{I_d}\right]^{\frac{\phi_{it,e}}{\phi_i}}$$

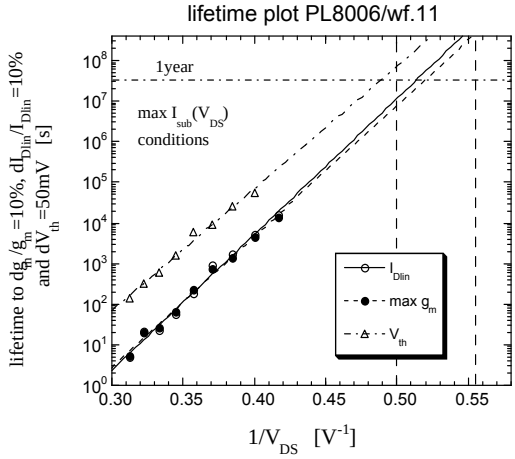


ϕ_i : impact ionization energy (~1.3eV)

$\phi_{it,e}$: energy needed for creation of an interface trap (~ 3.5eV)

Measure of the electric field

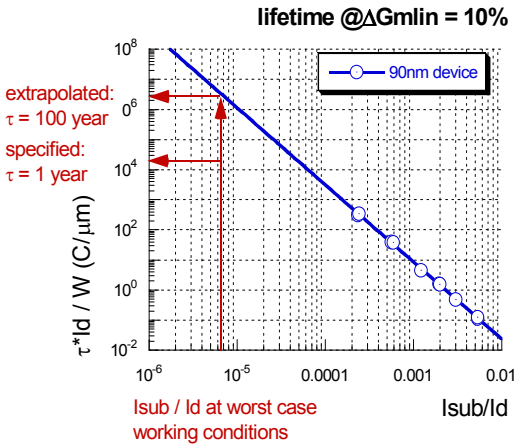
LIFETIME



I_{Dlin} and max g_m are the device lifetime limiting parameters.
Lifetime of more then 10 year is reached at 1.8V Vdd

HC LIFETIME OF A 90NM TECHNOLOGY

Wafers finished after 1LM



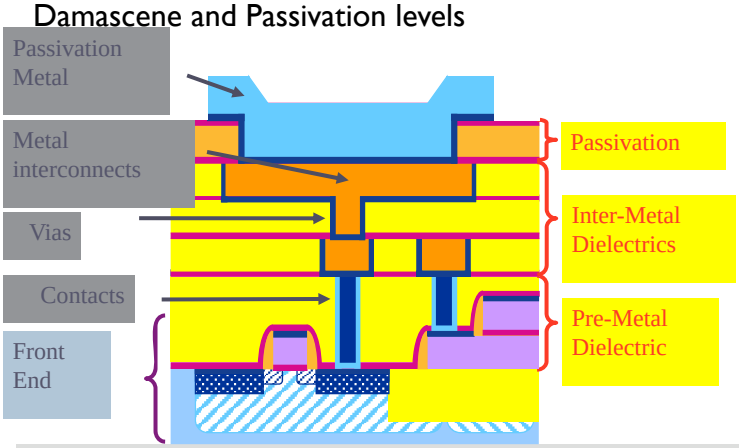
HC lifetime of this 90nm technology = ~100 years >> 1 year spec!

 112

IMPACT OF BACK END PROCESSING

Back End Processing consists of

- Deposition of the Pre-Metal Dielectric (PMD), Inter-Metal Dielectric (IMD) and Passivation dielectrics
- metallisation of Contact, Single Damascene, Dual Damascene and Passivation levels



 113

IMPACT OF BACK END PROCESSING

Each dielectric layer can affect the gate oxide and the Si-gate oxide interface quality (and thus the HC lifetime)

- ☒ Their deposition can create interface states
- ☒ Their presence can block efficient sintering
- ☑ Their deposition can diminish the amount of interface states
- ☑ Their presence can avoid that subsequent process steps to create interface states (they act as a barrier layer)

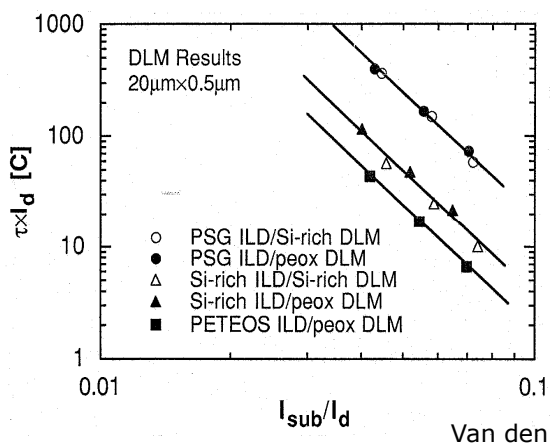
→ Effect of dielectric layers is very difficult to predict

- Case by case analysis necessary!

Can metallisation steps affect the interface quality?

- There is no clear evidence gathered at IMEC
- Some reports exist in literature, e.g. on Al-metal etch

INFLUENCE OF BACKEND PROCESSING



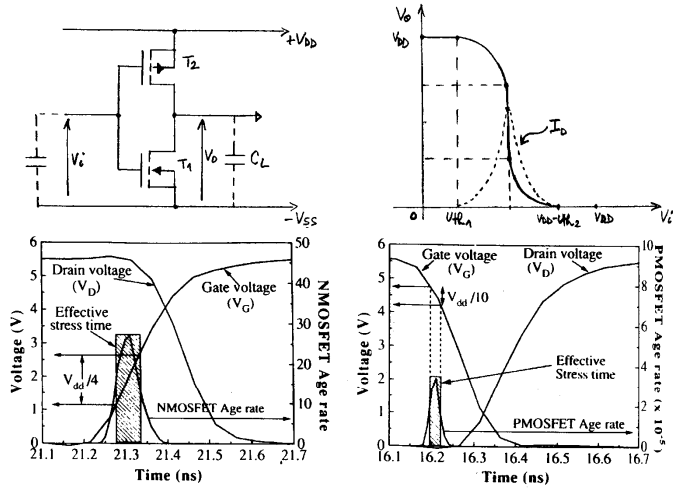
0.5µm CMOS (DLM, TLM)
SOG planarization

ILD=interlevel dielectric
IMD=intermetal dielectric

Van den bosch et al., ESSDERC 1994

Backend processing can have a tremendous influence on the hot carrier lifetime !

DYNAMIC DEGRADATION

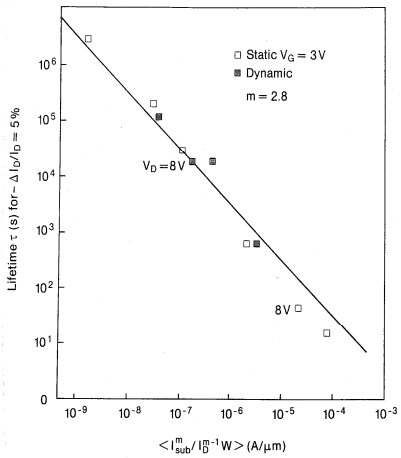


N-channel MOSFET (input low -> high)

P-channel MOSFET (input high -> low)

In digital circuits: transistors are only stressed during switching transitions: calculated as a "duty cycle"

LIFETIME PREDICTION AC CONDITIONS



$$\tau = C\left[\frac{1}{T}\int_0^T \frac{I_{sub}^m}{I_d^{m-1}}dt\right]^{-1}$$

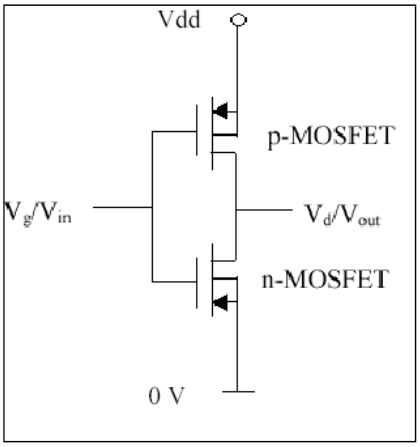
OUTLINE

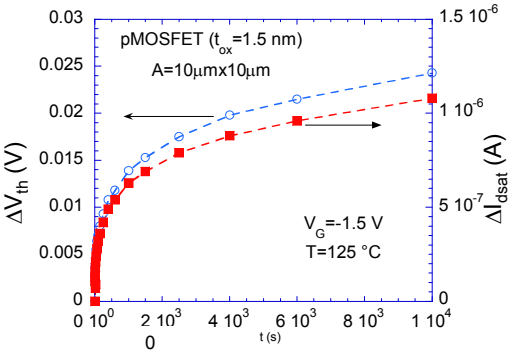
1. Introduction
2. Basic reliability concepts
3. Time-dependent Dielectric Breakdown (TDDB)
4. Hot carrier degradation
5. Bias-Temperature Instability (NBTI)
   - Basics
   - Acceleration model
   - Physical models
   - Frequency dependence
   - Impact of processing

INTRODUCTION

Negative bias temperature instabilities

CMOS inverter





V_{th} shifts and reduction of I_{Dsat} occur when p-MOSFET is switched on: Negative Bias Temperature Instabilities

CAUSE OF THRESHOLD VOLTAGE V_{TH} SHIFT (Δ): GENERATION OF INTERFACE AND OXIDE TRAPPED CHARGE

$$\Delta V_{th} = \frac{\Delta Q_{it} + \Delta Q_{ot}}{c_{ox}} = \frac{q \Delta N_{eff}}{c_{ox}}$$

$$\Delta Q_{it} = q \, \Delta N_{it}$$

$$\Delta Q_{ot} = \frac{1}{t_{ox}} \int_0^{t_{ox}} (t_{ox} - z) \Delta \rho(z) dz$$

Note: sometimes used

$$\Delta N_{eff} = \frac{c_{ox} \Delta V_{th}}{q}$$

c_{ox} … Oxide capacitance per area [Fcm^{-2}]
t_{ox} … Oxide thickness [cm]
Q_{it} … Interface charge density [Ccm^{-2}]
N_{it} … Interface state density [cm^{-2}]
Q_{ot} … Oxide trapped charge density [Ccm^{-2}]
$\rho(z)$ … Oxide trapped charge density [Ccm^{-3}]

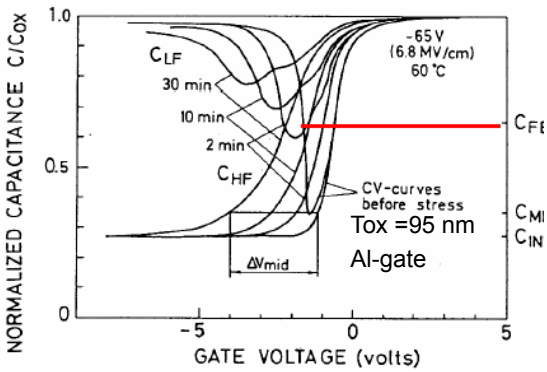
BTI: CHARGED OXIDE BULK AND INTERFACE STATES

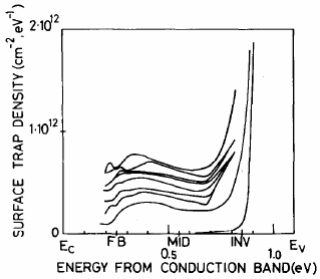
NBTI (pFET)	PBTI (nFET)
Positive oxide charge (negative V_{th} shift)	Negative oxide charge (positive V_{th} shift)
Interface states (mobility, transconductance, subthreshold-slope degradation) Mitani *et al.*, ECS 2005 Garros *et al.*, ICICDT 2010	X (but observed in sub 1nm EOT)
Generally at substrate interface	**Generally trapping in high-k**

Zafar *et al.*, VLSI 2006
Kerber *et al.*, TED **55**, 3175 (2008)
Aoulaiche *et al.*, IRPS 2009

NEGATIVE BIAS TEMPERATURE INSTABILITY

Occurs at relatively low voltage/fields and high temperatures
Mostly pMOS problem (negative Vg)
Problem exists from early days of MOSFET technology !
Damage not related to charge transport through dielectric
Interpretation: fixed positive charge and interface trap generation (acceptor in upper, donor in lower half of bandgap)

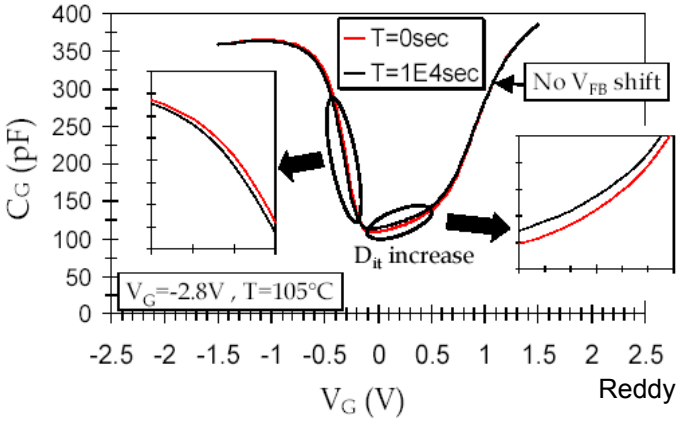




Jeppson, Svensson, JAP 1977

ORIGIN OF NBTI SHIFTS

Other interpretation:
- no positive charge, no Vfb shift
- donor type interface traps

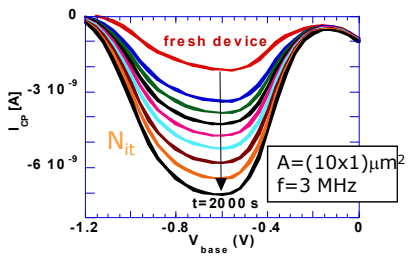


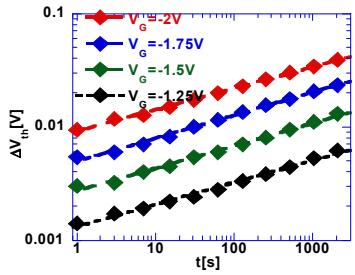
Tox = 2.7 nm
Poly gate

Reddy et al, IRPS 2002

imec

INTERFACE STATE DENSITY GENERATION OBSERVED BY CHARGE PUMPING



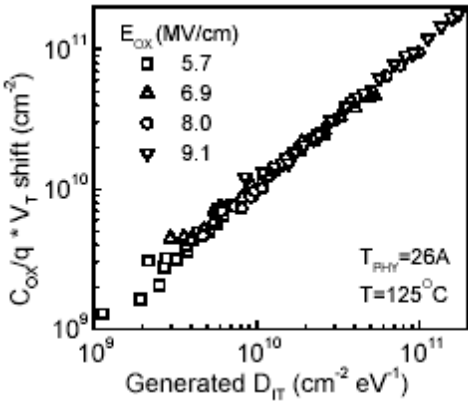


$$\Delta N_{it}(t) = \frac{\Delta I_{CP,\max}}{q.A.f}$$

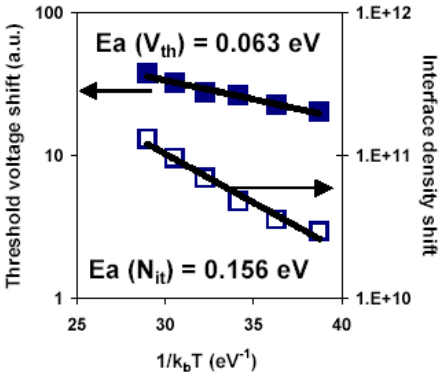
e.g. M. Aoulaiche *et al.*, Microelectron. Eng. **80**, 134-137 (2005).

Note: also gives V_{th} and V_{FB} shifts

ORIGIN OF NBTI SHIFTS



M. Alam et al., IEDM 2003

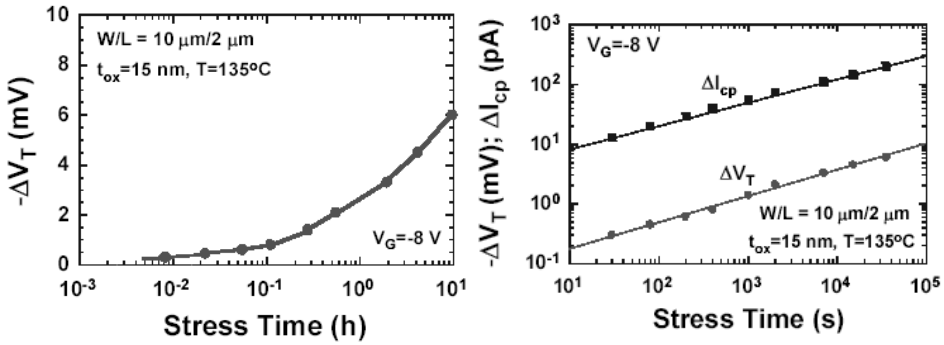


V. Huard et al., IRPS 2003

1:1 Correlation between threshold voltage shift and interface trap generation indicates that Dit generation is dominant !

But Vt-shift and Dit increase exhibit different activation energies: no consensus !

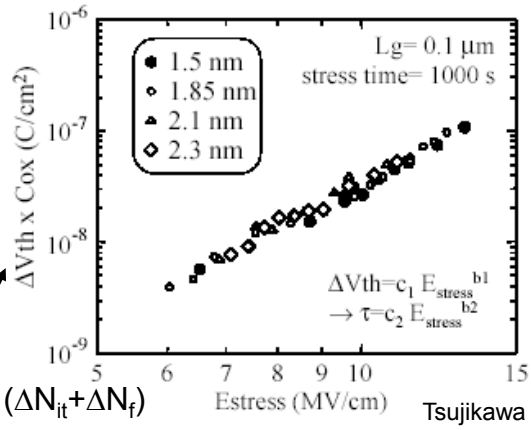
TIME DEPENDENCE



$$\Delta V_T = A\, t^n$$

Threshold voltage shift and Dit-generation show power law Dependence with slope n=0.2-0.3

OXIDE THICKNESS DEPENDENCE



ΔV_{th} Cox = q (ΔN_{it}+ΔN_f)

Tsujikawa et al, IRPS 2003

Normalized Vt shift as a function of E shows universal behaviour for all oxide thicknesses

Data show power law field dependence:~E^b

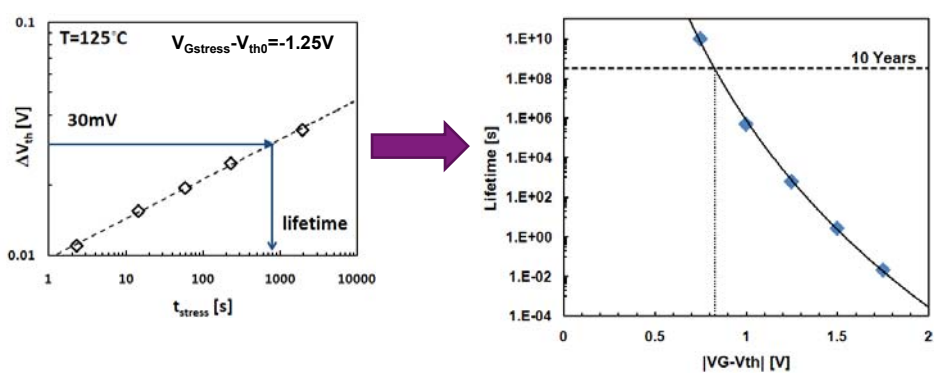
ACCELERATION MODELS

$$\Delta V_T = C \cdot \exp\left(-\frac{E_a}{kT}\right) \cdot \exp\left(\beta \left|V_G\right|\right) \cdot t^n$$

Voltage/field acceleration: no consensus
- linear (~ E)
- power law (~ E^n, n=1.5)
- exponential (~exp(E))
- 1/Vg

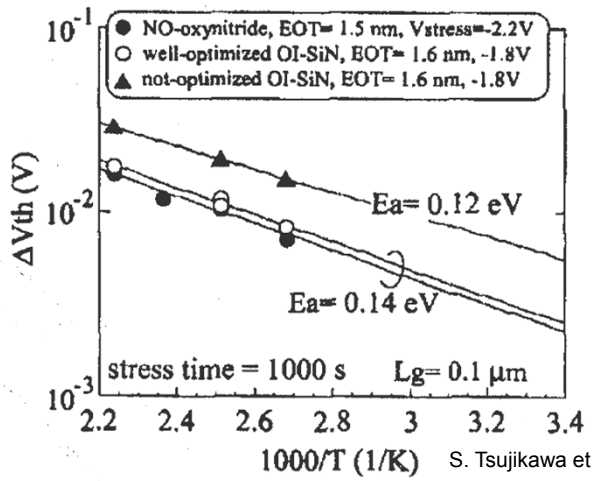
Temperature acceleration: consensus
- Arrhenius

EXAMPLE OF BTI LIFETIME EXTRAPOLATION



- Failure Criterion: ΔV_{th} = 30mV at T = 125°C
- Minimized relaxation: t_{sense_delay} = 2ms
- Stress experiment at different voltages ($V_{Gstress} > V_{DD}$) → Estimate lifetime → Power Law extrapolation at 10 Years

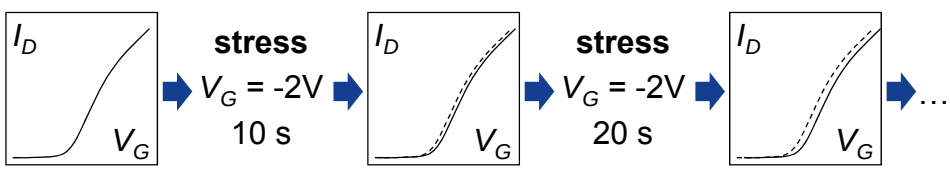
ACCELERATION MODEL: TEMPERATURE

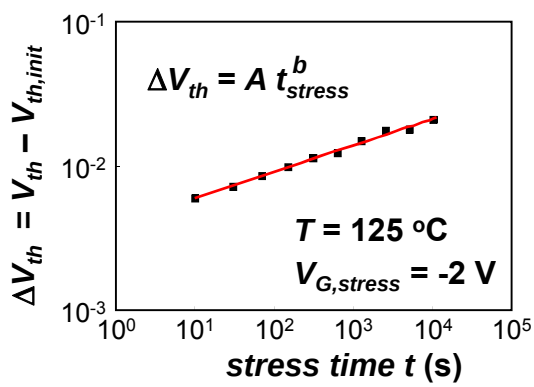


S. Tsujikawa et al., *IRPS 2003*, p. 183

Activation energies are usualy in the order of 0.12-0.15 eV

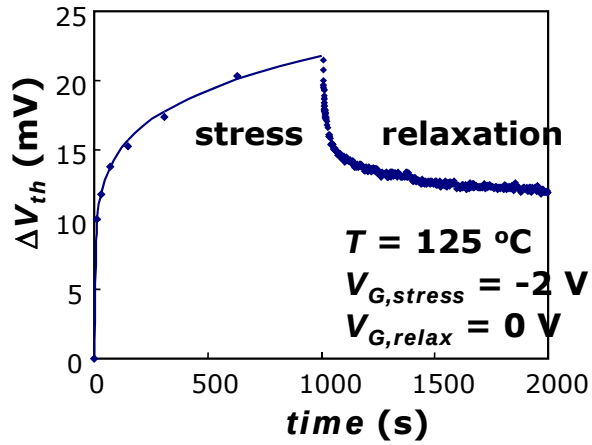
NBTI DEGRADATION—SEEMINGLY STRAIGHTFORWARD MEASUREMENT





V_{th} shift appears to follow power-law

"MINOR" COMPLICATION: THRESHOLD VOLTAGE SHIFT STARTS RELAXING IMMEDIATELY AFTER STRESS REMOVED



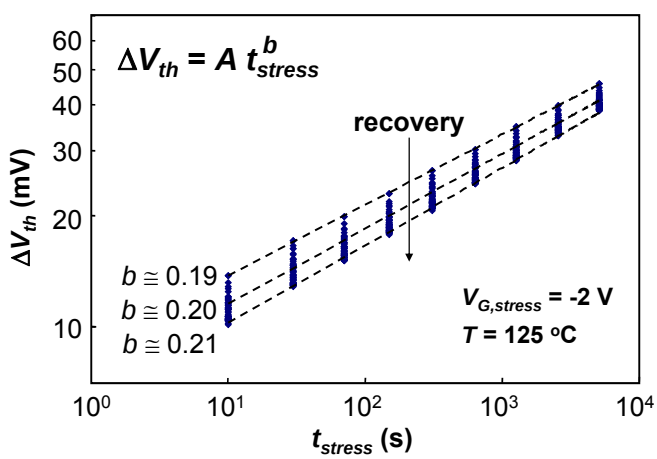
Crucial issue for all BTI measurements and interpretation!

Observed in p/nFETs, P/NBTI, DC and AC stress...

Kerber *et al.*, TED **55**, 3175 (2008); Kaczer *et al.*, IRPS 2008

imec © IMEC 2016 132

A AND *B* DEPEND ON T_{MEAS}



A decreases while *b* increases with increasing t_{meas}

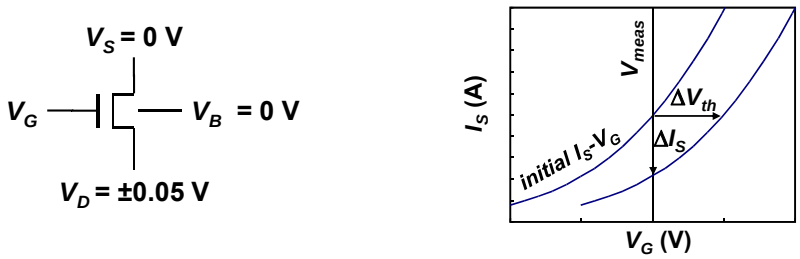
imec © IMEC 2016 133

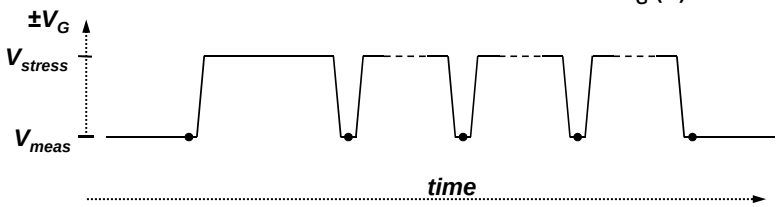
MEASURING BTI

- Several methods developed to compensate relaxation, based on
  - Measure-Stress-Measure
  - On-the-fly
- No single "silver bullet" approach to measuring BTI
- Relaxation time needs to be considered otherwise ΔV_{th} measurement meaningless
- JEDEC standards give some guidance
- Rule of thumb: when comparing stacks/processing, use the same measurement setup (fields, timing, etc)

FAST MEASURE-STRESS-MEASURE (MSM) TECHNIQUE

...devised to speed up BTI threshold voltage shift measurements

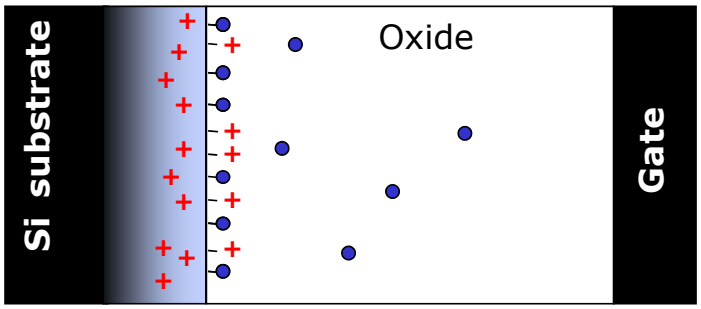




Measurement speed increased to ~ 0.1 s

B. Kaczer *et al.*, SISC 2004, IRPS 2005

MOST POPULARIZED EXPLANATION FOR NBTI : REACTION-DIFFUSION MODEL : DIFFUSION OF HYDROGEN IS THE RATE-LIMITING STEP



- All effects explained by interface states generation (ΔN_{it}):
  - Channel holes break hydrogen bonds passivating interface state
  - Hydrogen released, diffuses through SiO_2
  - Repassivation of interface states during relaxation

Jepsson & Svensson, J. Appl. Phys. **48,** 2004 (1977)

M. A. Alam, IEDM 2003

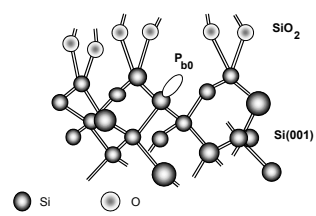
imec © IMEC 2016 136

REACTION-DIFFUSION MODEL

= Most popular models for NBTI

$$Si_3 \equiv SiH + X \underset{k_t}{\overset{k_f}{\rightleftarrows}} Si_3 \equiv Si^{\bullet} + Y$$

$$Y_{\text{interface}} \rightarrow Y_{\text{bulk}}$$



Model orginally proposed by Jeppson and Svensson, 1977, further elaborated by Ogawa et al, 1995 and recently by many other groups

-Si-H bonds interact with holes (species X) and are broken (reaction)

- Result: Si dangling bond (interface trap)

- H-related species Y diffuses away from the interface (diffusion): H_2, H, H^+, OH

- H-species diffusion is rate limiting step: explains power law slope n=0.25

K. Jeppson and C. Svensson, JAP **48**, 2004 (1977)

S. Ogawa and N. Shiono, PRB **51**, 4218 (1995)

S. Ogawa et al., JAP **77**, 1137 (1995)

imec 137

REACTION-DIFFUSION MODEL

Generation Annealing

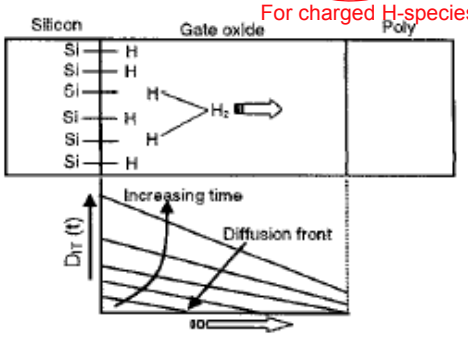
$$\frac{\partial N_{it}}{\partial t} = k_1(N_0 - N_{it}) \cdot p - k_2 N_{it} N_H(x,t)$$ Reaction

$$N_{IT}(t) = \int_0^\infty N_H(x,t)dx$$

$$\frac{\partial N_H}{\partial t} = D_H \frac{\partial^2 N_H(x,t)}{\partial x^2} - \mu E_{ox} \frac{\partial N_H}{\partial x}$$ Diffusion

For charged H-species

N_o=Initial SiH bonds



Early stress phase:
Reaction rate k_1 is dominant

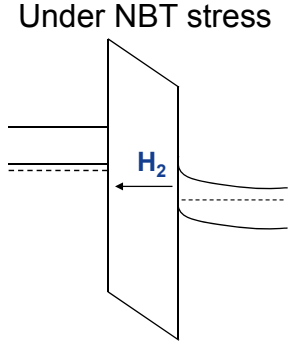
Later stress phase:
Diffusion rate is dominant

M. Alam et al, IEDM 2003

REACTION-DIFFUSION MODEL

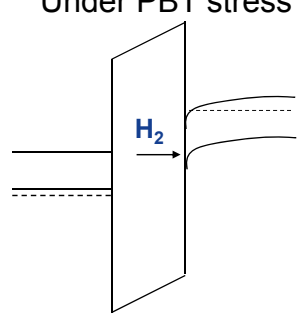
Recovery effects:

Under NBT stress



p^+ poly-Si SiO_2 n-Si

Under PBT stress

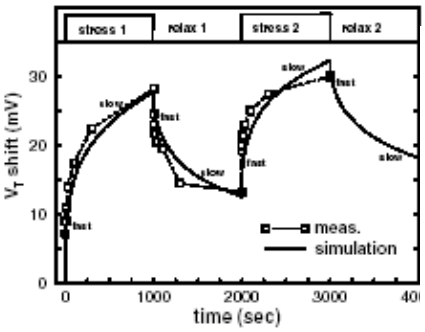


p^+ poly-Si SiO_2 n-Si

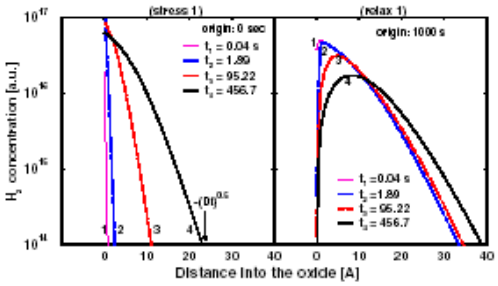
Using the reaction-diffusion model, Alam proposed that partial V_{th} recovery is due to the passivation of P_{b0} centers by H_2 (or H) that diffuses back towards the Si/SiO_2 interface when the gate bias is switched or set to zero.

M. Alam, *IEDM 2003*, 345

REACTION-DIFFUSION MODEL



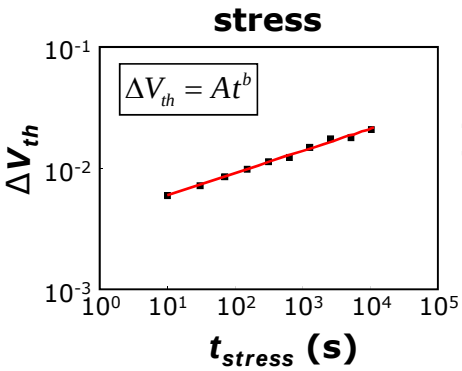
Stress (kf) Relax (kf=0)

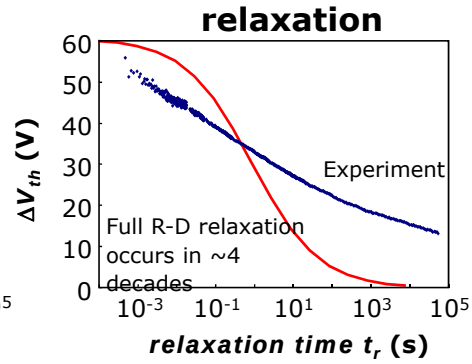


M. Alam et al, IEDM 2003

R-D model allows good simulation of stress/relaxation cycles

PREDICTIONS OF THE CLASSIC R-D MODEL





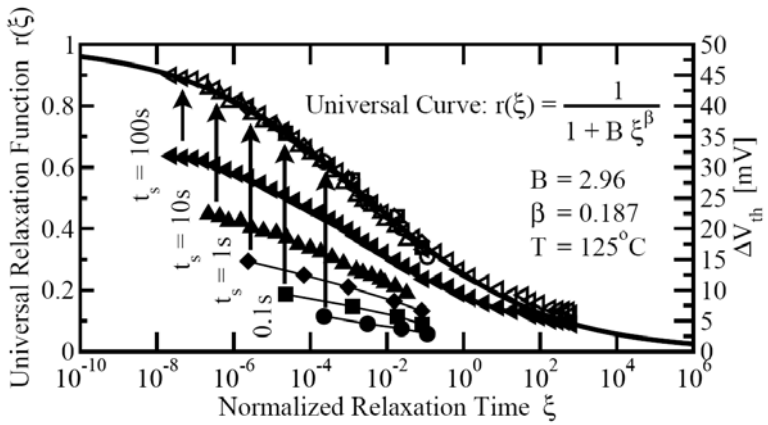
$$\Delta = f(G, R)$$

intricate balance between generation recombination (relaxation)

$$\Delta = f(0, R)$$

→ Stress phase cannot be described correctly if "R" not described correctly…

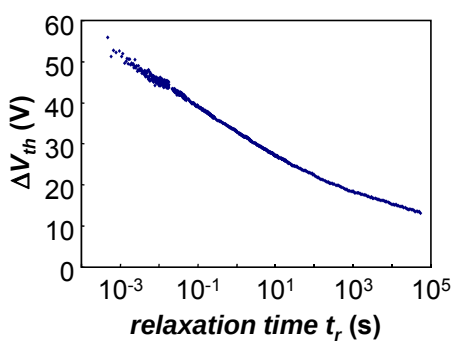
PROPERTY OF BTI RELAXATION: RELAXATION TRANSIENTS CAN BE RESCALED TO THE SAME UNIVERSAL RELAXATION CURVE

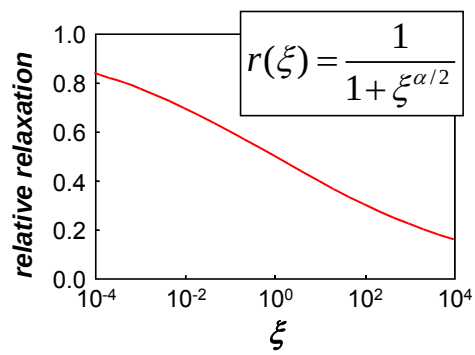


- $\xi = t_{relax} / t_{stress}$
- $R(t_{trelax}) / S(t_{stress})$

Grasser *et al.*, IEDM 2007

DISPERSIVE NBTI RECOVERY : LONG LOGARITHMIC RELAXATION TAIL WELL DESCRIBED

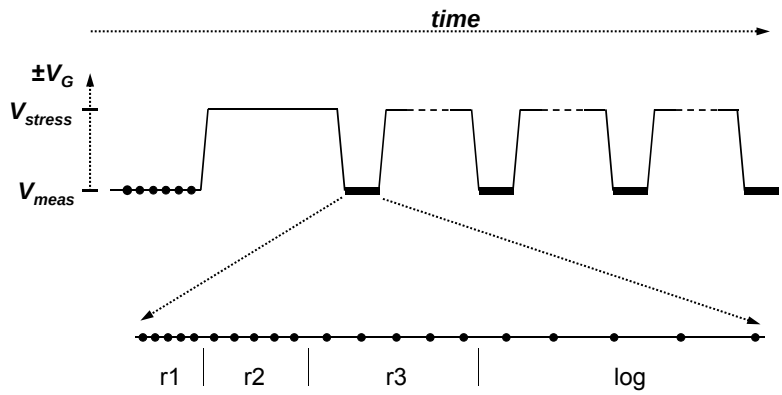




$\xi = t_{relax} / t_{stress}$ is the dimensionless relaxation time

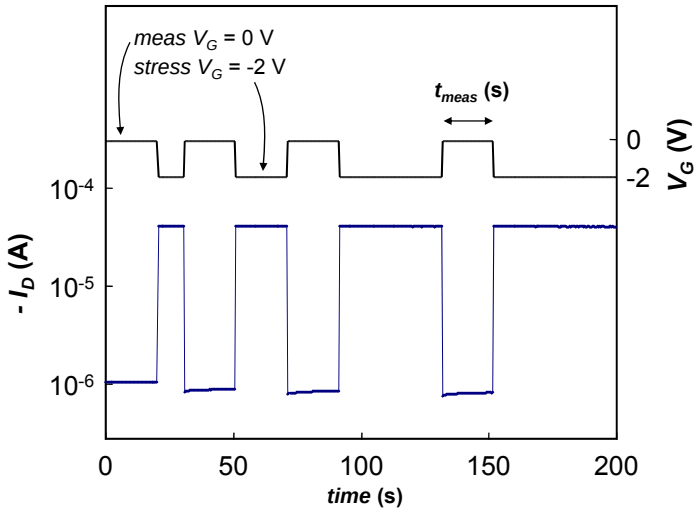
Kaczer *et al.*, IRPS 2005

NEW, "EXTENDED" MSM TECHNIQUE: SEVERAL DECADES OF RELAXATION TREND RECORDED AFTER EVERY STRESS



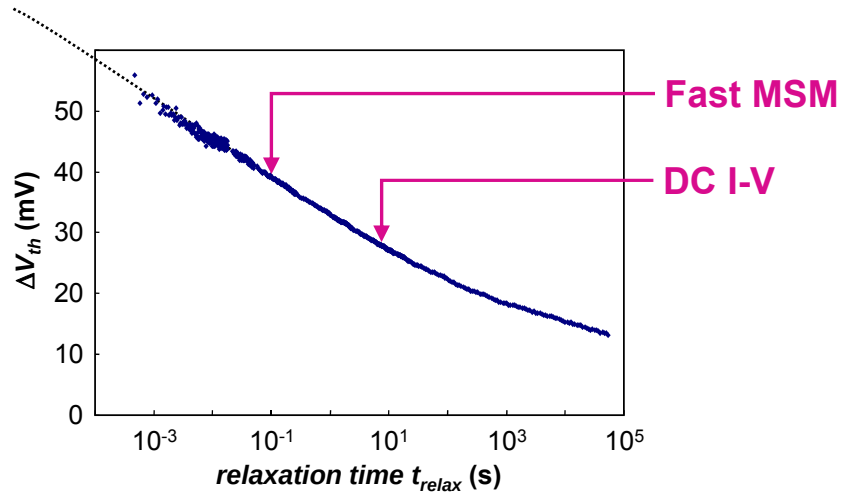
Advantage: can be done with standard off-the-shelf equipment

MEASURING V_{TH} SHIFT (2)



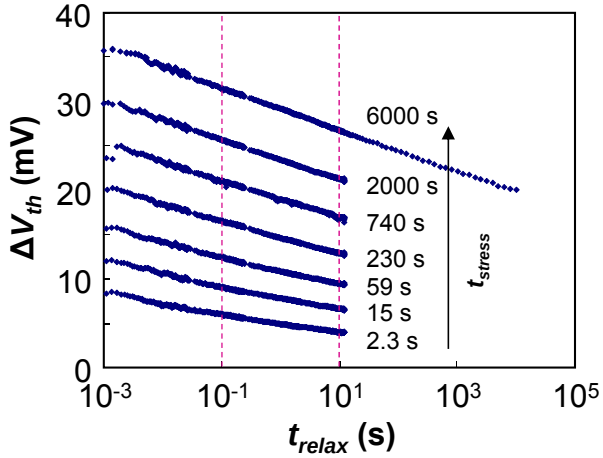
Flexible: 1) fast measurement, or 2) the effect of **recovery** can be studied

BTI DEGRADATION RELAXES "DISPERSIVELY" OVER MANY TIME SCALES: MICROSECONDS OR LESS TO DAYS OR MORE



Improvement of a few decades negligible on the logarithmic scale

TYPICAL EXTENDED MSM MEASUREMENT : RELAXATION TRENDS RECORDED INSTEAD OF SINGLE POINTS



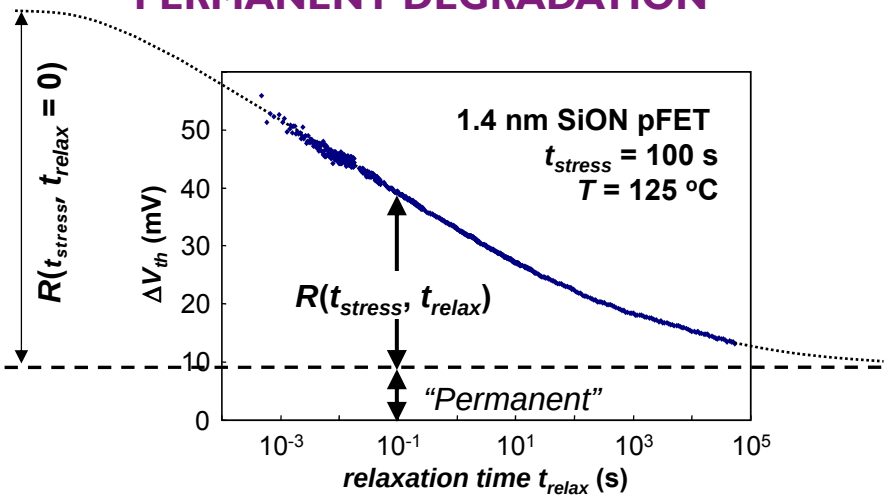
HfSiO pFET

T = 125 °C

$V_{stress} = V_{meas} - 1.8V$

The effect of techniques measuring at different speeds (Fast MSM, DC-IV) can be looked up on this graph (allows "fallback")

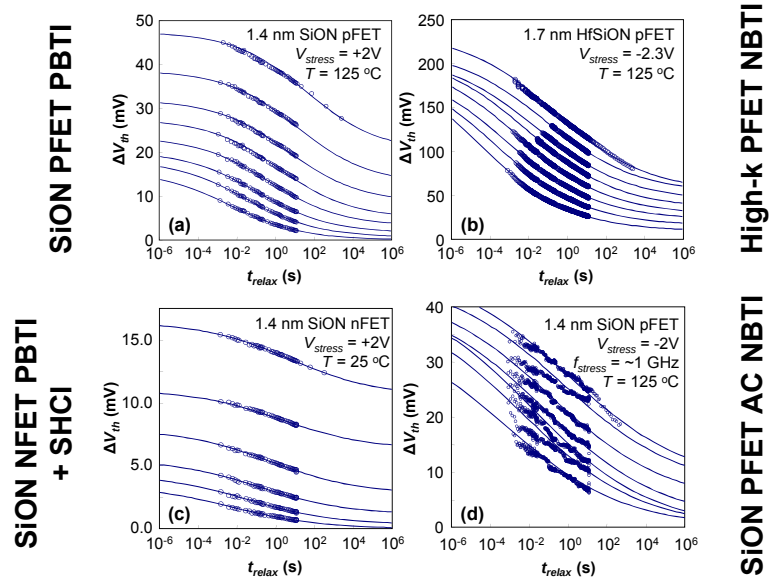
RELAXATION NOT COMPLETE: PERMANENT DEGRADATION



$$\Delta V_{th} = R(t_{stress}, t_{relax}) + P(t_{stress})$$

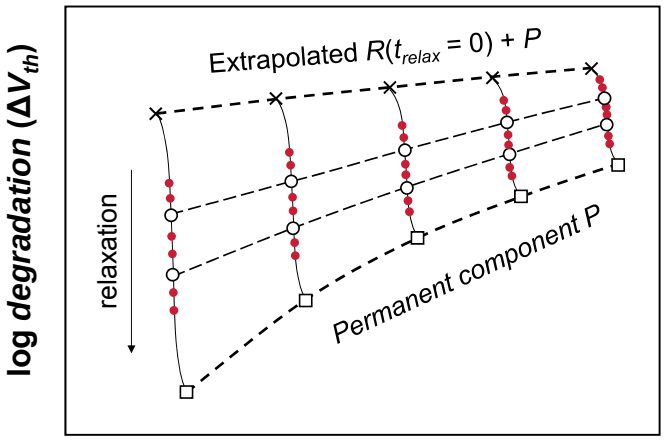
imec © IMEC 2016 148

BTI RELAXATION IS PRESENT IN MOST SYSTEMS



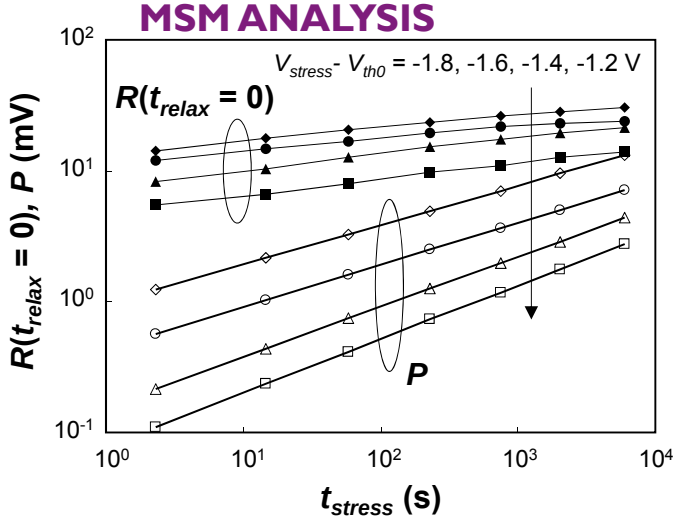
imec © IMEC 2016 149

SCHEMATIC SUMMARY: PREVIOUS VS. NEW ANALYSIS



Recorded relaxation transients carry additional information, used to separate recoverable and permanent components

TYPICAL RESULT OF EXTENDED MSM ANALYSIS



HfSiO pFET

T = 125 °C

Recall: total $\Delta V_{th} = R(t_{stress}, t_{relax}) + P(t_{stress})$

PRESENT UNDERSTANDING OF THE NBTI COMPONENTS

Recoverable component "R":

- Interface states (N_{it})
  - Cannot be due to discharging of interface states (too fast)
  - Cannot be due to R-D passivation of interface states (long relaxation tails)
  - Cannot be due to R-dispersive Diffusion passivation of interface states
- Hole trapping (N_{ot})
  - Elastic tunneling too fast in thin oxides
  - **Most likely after inclusion of inelastic phonon component**

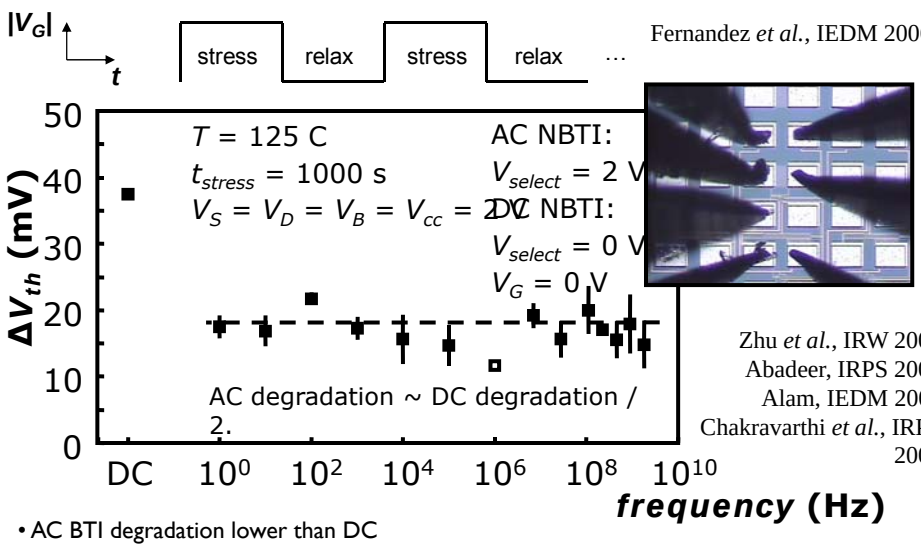
Permanent component "P":

- Hole trapping (N_{ot})
  - Possibly not fully permanent but really long relaxation
- Interface states (N_{it})
  - **Most likely component**

imec © IMEC 2016 152

PFET AC NBTI: (FAST) SEQUENCE OF STRESS AND RELAX PHASES

Fernandez *et al.*, IEDM 2006

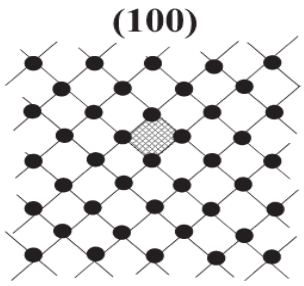


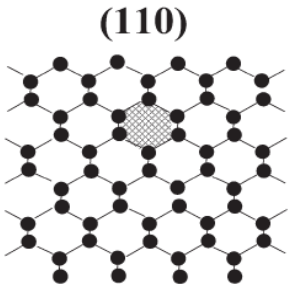
Zhu *et al.*, IRW 2002
Abadeer, IRPS 2003
Alam, IEDM 2003
Chakravarthi *et al.*, IRPS 2004

- AC BTI degradation lower than DC
- *f*-independent up to GHz → no "cut-off" time scale down to ~1 ns

imec © IMEC 2016 153

(110) AND (100) SURFACE ORIENTATIONS





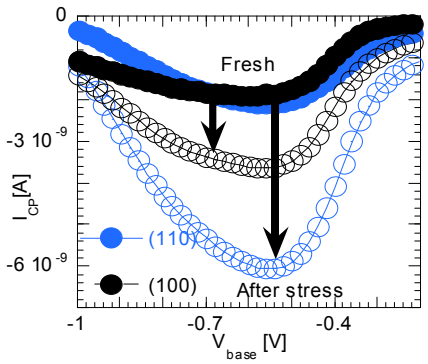
Higher electron mobility

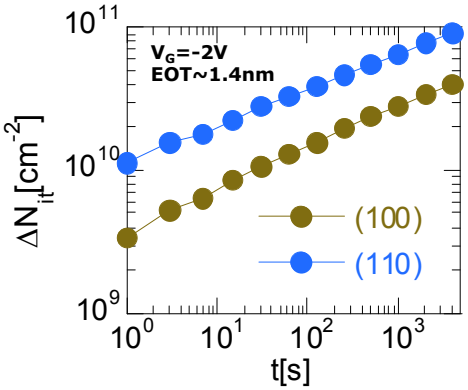
- Higher hole mobility
- Higher density of Si-H bonds

M. Yang, et al. IEDM pp. 453-456, 2003.

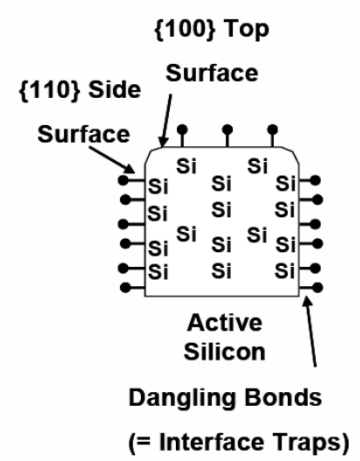
(110) SURFACE ORIENTATION DEGRADED MORE BY NBTI

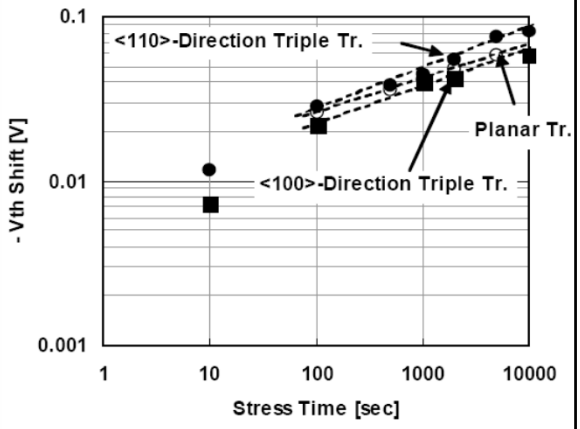
M. Aoulaiche *et al.*, SISC ,2006





INFLUENCE OF SIDEWALL ORIENTATION





S. Maeda *et al.*, IRPS 2004

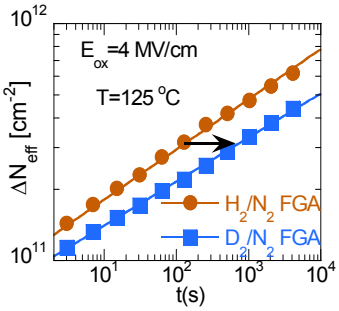
NBTI was reported to be slightly worse for MuGFET devices due to (110) sidewall orientation

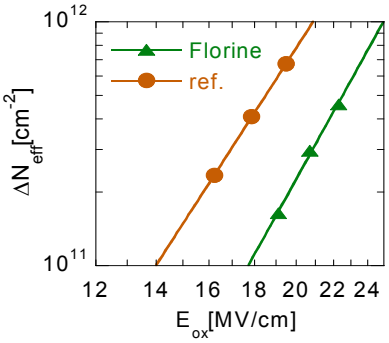
IMPROVEMENT DUE TO DEUTERIUM AND FLUORINE

$$Si_3 \equiv Si - D \approx Si_3 \equiv Si - H$$

$$Si - H \approx 2.2eV$$
$$Si - F \approx 5.8eV$$

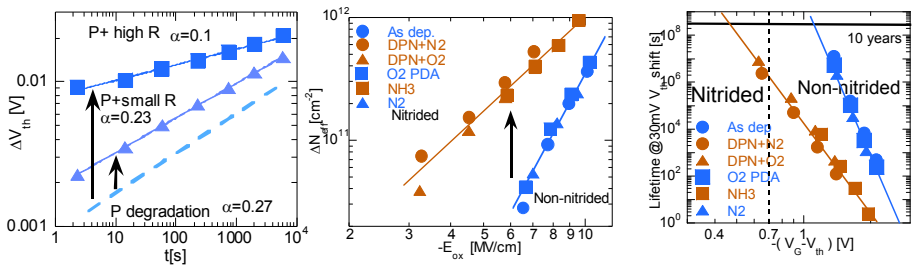
Difference in the dissociation dynamics multiple-vibrational excitation [Van de *walle et al.*]





M. Houssa *et al.*, Electrochemical and Solid-State Letters, 2006

INCREASED NBTI DEGRADATION DUE TO NITROGEN INCORPORATION



NBTI has become important again with the introduction of nitrided oxides: V_{th} shifts and I_{dsat} reduction are much enhanced in oxynitride layers, the more so when N content at the Si/dielectric interface increases.

M. Aoulaiche *et al.*,JVST B, 2009

imec © IMEC 2016 158

NBTI IN OXYNITRIDE LAYERS

Consensus more or less reached on the cause of NBTI acceleration in nitrided oxides:

presence of nitrogen-induced defects can trap holes and/or protons, leading to the generation of positive charges in the oxide:

Efficient hole trapping center (strained N-bond)

$$Si_2 = N - Si + h^+ \rightarrow (Si_2 = N - Si)^+$$

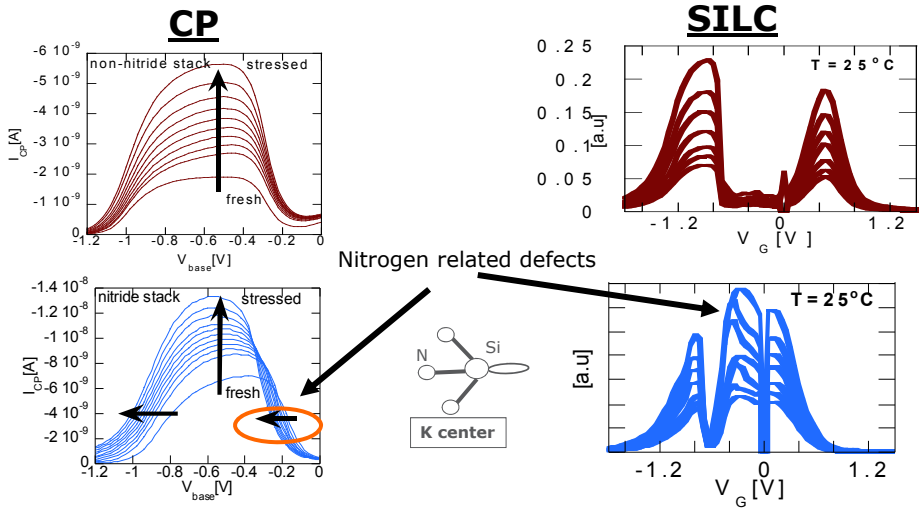
$$Si_2 = N - Si + H^+ \rightarrow (Si_2 = NH - Si)^+$$

Consequence: Larger V_{th} shift when [N] increases

N. Kimizuka et al., *2000 VLSI Symp.*, p.92.
K. Kushida-Abdelghafar et al., APL **81**, 4362 (2002)
S.S. Tan et al., APL **82**, 1881 (2003)
S. Fujieda et al., APL **82**, 3677 (2003)
M. Houssa et al., JAP **95**, 2786 (2004)

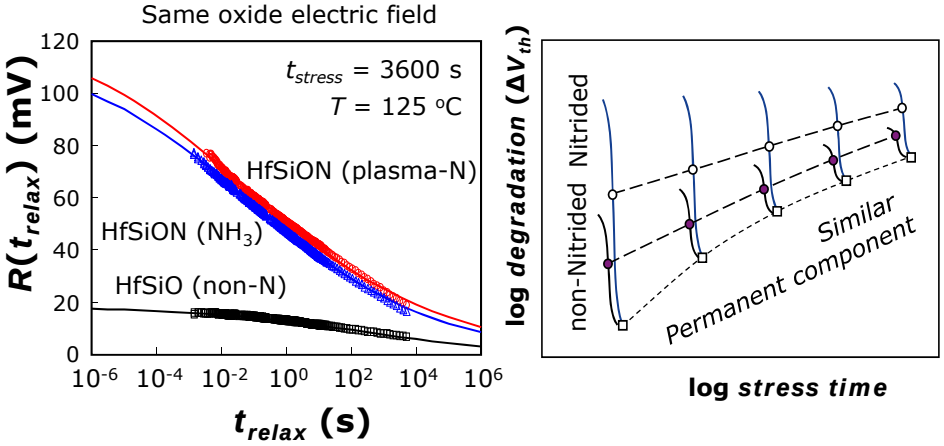
imec © 159

NITROGEN INDUCES ADDITIONAL HOLE BULK TRAPS



IMPACT OF NITROGEN— RECOVERABLE COMPONENT ONLY

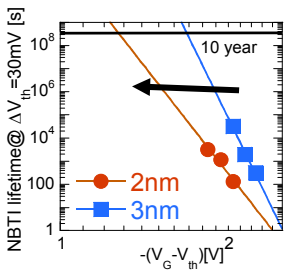
Same oxide electric field



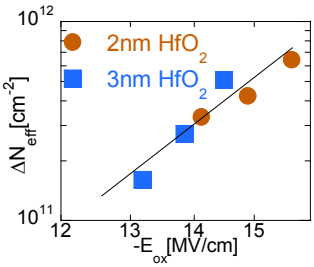
M. Aoulaiche *et al.*, JVSTB, 2009

IMPACT OF HFO_2 THICKNESS : MECHANISM CONTROLLED BY ELECTRIC FIELD AT SI/SIO_2 INTERFACE

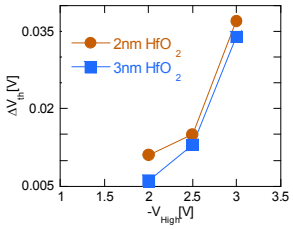
NBTI lifetime



ΔN_{eff}

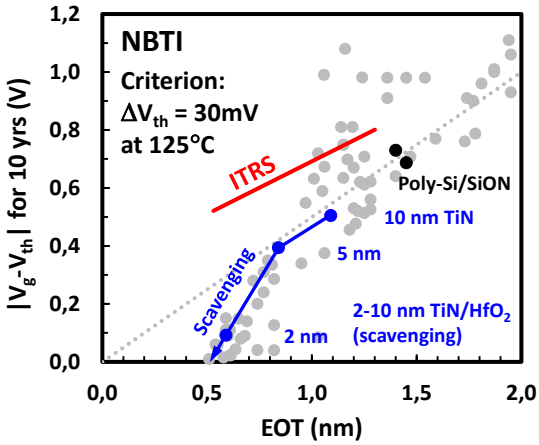


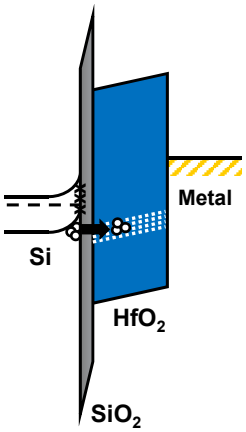
ΔV_{th} from IV-pulse



NBTI scales with E_{ox} at Si/SiO_2 interface
→ NBTI increases for thinner HfO_2 due to higher E_{ox} at the Si/SiO_2 interface

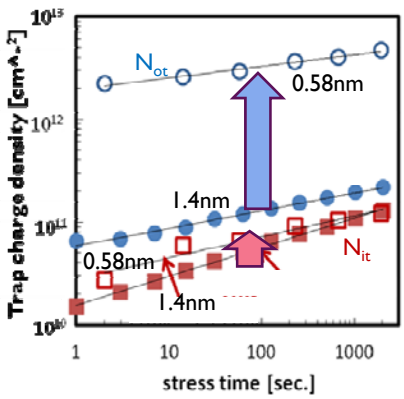
BTI IS A SERIOUS RELIABILITY PROBLEM

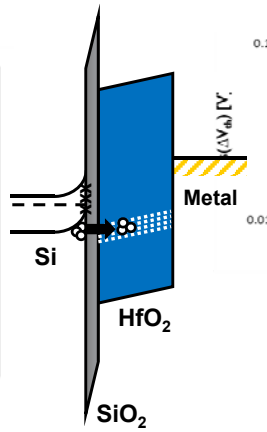


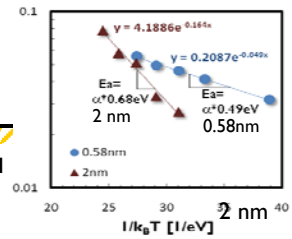


Example: Tolerable NBTI overdrive voltage for 10 years operation drops to zero in sub-1-nm EOT region

BULK DEFECTS DOMINATE THE NBTI DEGRADATION IN SUB-NANOMETER EOT REGIME







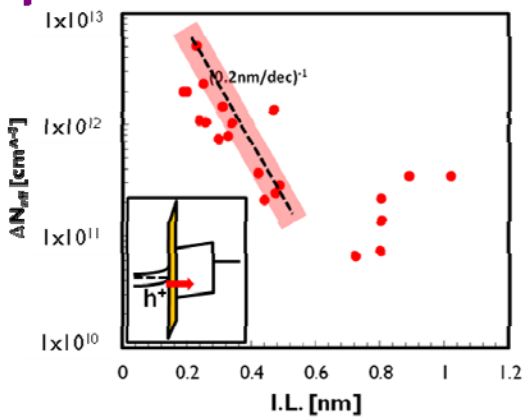
Lower activation energy for 0.58nm EOT devices: more direct tunneling of holes from the channel into the oxide

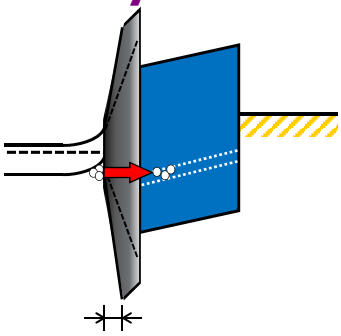
N_{ot} strongly increases in the 0.58nm EOT devices, Nit is similar in both devices

M. Cho et al, IEEE TED, pp. 2042-2048, 2012

imec © IMEC 2016

Minimum interfacial layer thickness is required to maintain reliability !





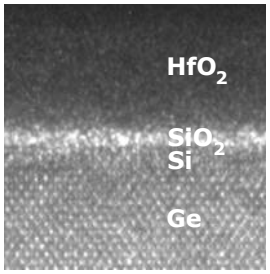
M. Cho et al, IEEE TED, pp. 2042-2048, 2012

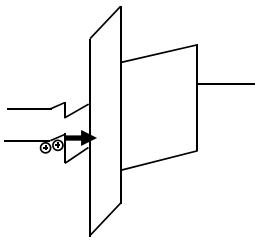
Minimum of 0.4nm interfacial layer needed to prevent sudden increase of the NBTI degradation

→ consistent with ab-initio modeling by Monaghan et al. (Phys. Rev. B, 2007)

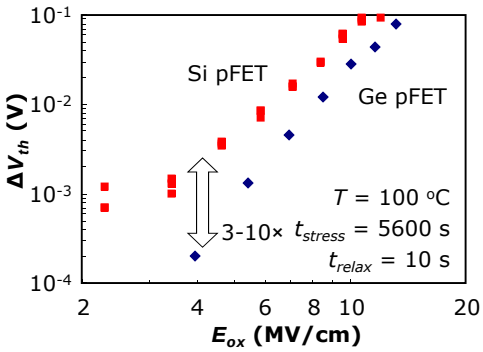
imec © IMEC 2016

NBTI IMPROVEMENT ON Ge-SUBSTRATE pFET





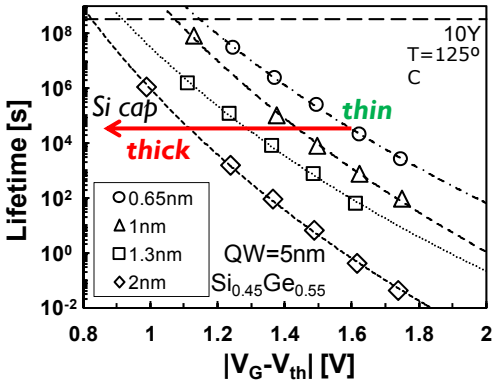
Ge Si SiO_2 HfO_2

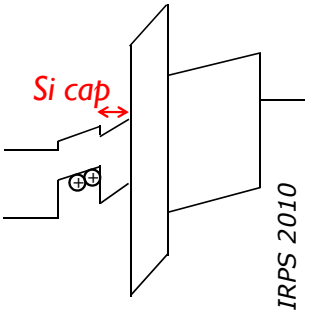


B. Kaczer *et al.*, Microel. Eng. 2009
J. Franco *et al.*, accepted to IRPS 2010

imec © IMEC 2016 166

Si CAP THICKNESS
THINNER CAP IMPROVES NBTI RELIABILITY



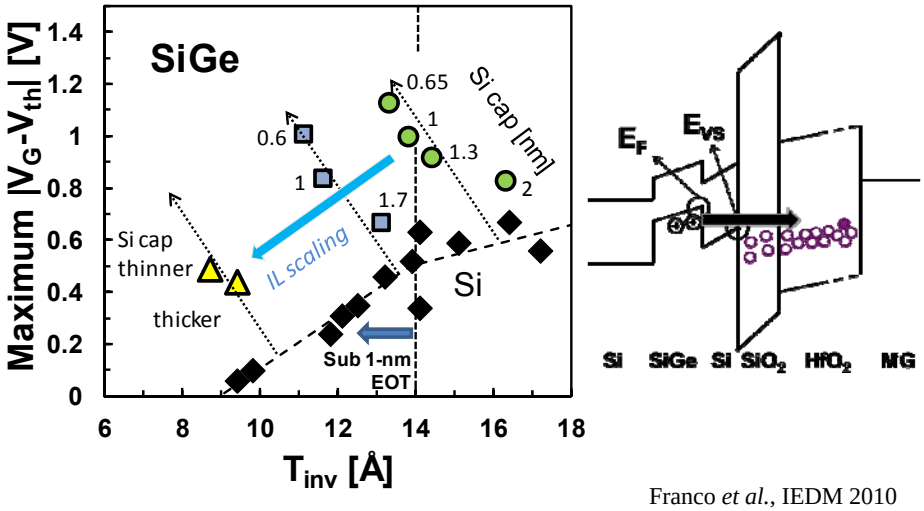


- Si cap thickness has a strong impact on NBTI
- ***Thinner*** Si cap → Reduced NBTI

J. Franco et al. IRPS 2010

imec © IMEC 2016

THIN SI CAP IMPROVES NBTI LIFETIME WHILE SCALING TINV

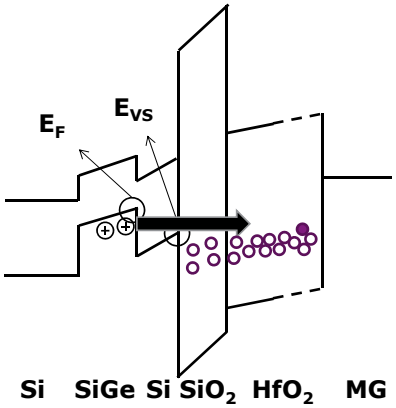


Franco *et al.*, IEDM 2010

Only solution so far: switch to SiGe substrates !

SiGe→LOWER ΔN_{OT}

MODEL: REDUCED INTERACTION WITH OXIDE DEFECTS



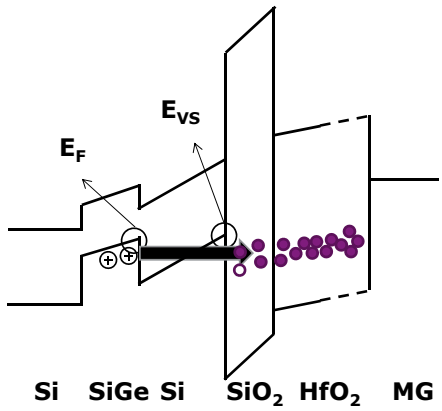
J. Franco et al. IEDM 2011

Thin Si cap: channel carriers (E_F) 'miss' part of the oxide defects

- Less defects, located on the gate side, are energetically favorable for holes
- Stronger field acceleration due to *'unaccessible'* traps becoming *'accessible'*

SiGe→LOWER ΔN_{OT}

MODEL: REDUCED INTERACTION WITH OXIDE DEFECTS



J. Franco et al. IEDM 2011

Thick Si cap: channel carriers (E_F) 'see' all the oxide defects

- Less defects, located on the gate side, are energetically favorable for holes
- Stronger field acceleration due to *'unaccessible'* traps becoming *'accessible'*

imec

CONCLUSIONS

1) Reliability becomes and more and more critical when downscaling technologies and needs to be taken into account in technology and material choices
2) TDDB, BTI and HCD are the three most critical device related failure mechanisms, lot of progress in the understanding of these failure mechanisms has been obtained in the past 3 decades
3) TDDB and HCD is under control provided the necessary technology measures are taken (e.g. corner rounding for FinFET's, drain engineering techniques)
4) NBTI reliability becomes a showstopper for Si based pMOS devices with sub-1nm EOT
5) (Si)Ge/SiO_2/HfO_2 pMOSFETs offer superior reliability w.r.t. Si for sub-1nm EOT nanoscaled pMOSFETs, optimized stack has been identified

imec