Contribution ID: **197** Type: **Oral**

Reliability and failure mechanisms of Integrated Circuits and devices

Friday, 30 September 2016 14:00 (3h 30m)

When scaling down CMOS towards smaller and smaller dimensions, the electrical fields inside the devices is increasing which leads to potential failures of the transistors. This can limit the lifetime of the circuits that are made in these technologies. As a result reliability is becoming more and more a fundamental limiting factor for the further downscaling of the technology. This lecture explains the main failure mechanisms that are acting at transistor level with focus on Time-dependent dielectric breakdown, Bias-temperature Instability and to a lesser extent also Hot carrier degradation. The basics as well as the test structures and characterization techniques needed to quantify the degradation, the voltage and temperature acceleration models and ways to cope with the problem and to improve the lifetime.

Summary

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Session Classification: Tutorial