Experience with igloo2 FPGAs in the CMS HCAL upgrade

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Date code and silicon revisions

Microsemi has changed a few times the revision of silicon chips inside the package, without notifying customers.

Customers can look at the date code on the package.
Format is YYWW , where YY = year, WW = weak

Date codes older than 1520 (20th week of 2015) have given many problems, with and without radiations.

You can specify this when you place an order

Igloo2 and SF2

As far as we know, igloo2 and SF2 are designed and manufactured identically.

A fuse is burned in igloo2 in order to permanently disable or power off the embedded processor

Programming files built for igloo2 do work on SF2

I think irradiation results on either family are valid for the other family.

Development software

The Development SW tool (Microsemi Libero) has a major fix related to the SERDES from version 11.6 SP1 (Jan 2016).

Must use this or newer versions for serial links

In the past it has been very painful to use igloo2 FPGAs, but now things are much better.

Even with the latest version, placement constraints, timing constraints and timing reports are difficult to understand, compared to other FPGA vendors.

igloo2 in our Control links

- bidirectional link running at ~4.8 Gbps (120 x LHC_clock)
- in sync with the LHC clock
- The Front-End side of the link recovers the clock and distribute it to the rest of the front-end (equivalent to the old TTCrx)
- The phase of the recovered clock can be monitored and corrected, so that it is constant
- GBT encoding with error correction
- 84 user bits every clock cycle, bidir

igloo2 in our Data links

- unidirectional link running at 5.0 Gbps
- async to the LHC clock
- Clocked by a local clock oscillator (low jitter easy to achieve)
- Logic circuits in the same igloo2 transfer the data from the LHC clock domain to the oscillator domain
- 8b10b encoding,
- 88 user bits every clock cycle
- Option to add error detection in the user bit (parity bit, Hamming codes, etc)
- Can implement multiple links a single FPGA

igloo2 in our Data links - continued

A practical consideration:

in our cards we needed 3 links (SERDES) out of 8 available in the FPGA.

The board designer chose to use the first consecutive 3 SERDES.

This has made the P&R inside the FPGA very difficult.

A better choise would be to alternate used and unused SERDES.

Triple Modular Redundany

The development tool comes with a special edition of the Symplify synthesiser

The synthesiser has an option to apply TMR on selected modules

The syntax is different for verilofg vs VHDL, and it is also different from other Microsemi FPGAs (ProASIC3)

Anyway we use it on most of the logic and it seems ok (altough we have not studied its performances)

Irradiation of a CMS HCAL system slice

Report on: https://cds.cern.ch/record/2128433

In a nutshell:

Mixed radiation, 10 krad (100 Gy).

Transient errors observed, but probably ok for our needs (difficult to find the root cause).

No permanent damage, including no damage to the FPGA programming.

NB: other groups have reached higher doses. See:
https://twiki.cern.ch/twiki/bin/viewauth/FPGARadTol/InformationOfInterest

Remote programming

Our front-end has been designed to support remote-programming of certain igloo2 FPGAs (not the igloo2 supporting the Control link).

The programming file is streamed over the control link. Then a ProASIC3L FPGA converts the format, and drive the JTAG lines of the target igloo2 FPGA.

We got it to work, but occasionally the operation fails.

Not clear while, but it seems that we can just repeat the operation till we succeed.

Questions ?