LHCb Calorimeter Upgrade

Electronics meeting

The LHCb calorimeter upgrade group

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- **Dose estimates**
  - The simulation indicates a dose of
    - 100 rad per fb^{-1} in the worst (bottom) part of the electronics above the calorimeter (calorimeter gantry)
    - Includes a factor 2 safety margin
  - Cross-check simulation/dosimeter show a relatively satisfactory agreement away from the beam pipe
  - The detector geometry changes for the upgrade
    - This has an impact on the dose
    - The simulations should be revisited
- **We should foresee**
  - ~ 5 krad for $50fb^{-1}$
- **SEL**
  - can be expected below 15 $MeV/cm^2/s$
- **SEU**
  - Triple voting mitigation of the configuration registers
  - Data are not protected but are not stored
  - Flash technology FPGA (program is SEU tolerant) from microsemi

FPGA for the upgrade of the calorimeter

- 3 main systems are concerned :
  - Front-end boards
  - Control boards (3CU)
  - HV/Calibration/Monitoring systems

- The calorimeter is mainly focusing on the IGLOO2
  - Decided for FEB and HV/Calibration/Monitoring
  - Example of the FEB
    - 5 FPGA IGLOO2 of 2 types (MG2L150 and MG2L050)
  - GBT-X data transmission compatible

- A3PE could still be an options for the control board
  - Depends on
    - Processing resources / IO of the chip with respect to the needs
    - Costs
  - However, the acquired experienced (FEB) could favour the IGLOO2

Overview of the dose/SEL/SEU problems

- Our understanding is that A3PE and IGLOO2 should be fine for us according to
  - SEL
  - SEU
  - Dose (A3PE_Limit ~ 50 krad, IGLOO2_Limit ~ 100 krad)
- However, the reprogramming of the FPGA is sometimes problematic
  - Some tests showed that IGLOO2 could not be reprogrammed after 10 krad
    - JTAG mechanism failure ?
  - Experience the same type of problem on the old ProASIC-3 family
- Get our information mainly from (Tullio)
  https://twiki.cern.ch/twiki/bin/viewauth/FPGARadTol/InformationOfInterest
- We should get a new proto board with IGLOO2 in a couple of weeks
  - Plan is to test it in beam for radiation tolerance
  - Our FPGA have been heavily tested and the expected dose is limited
  - Mainly focusing on the other components of the board
    - Thinking about having a specific test board to be irradiated
    - The analog chip should be tested soon (CERN, Louvain-la-Neuve)