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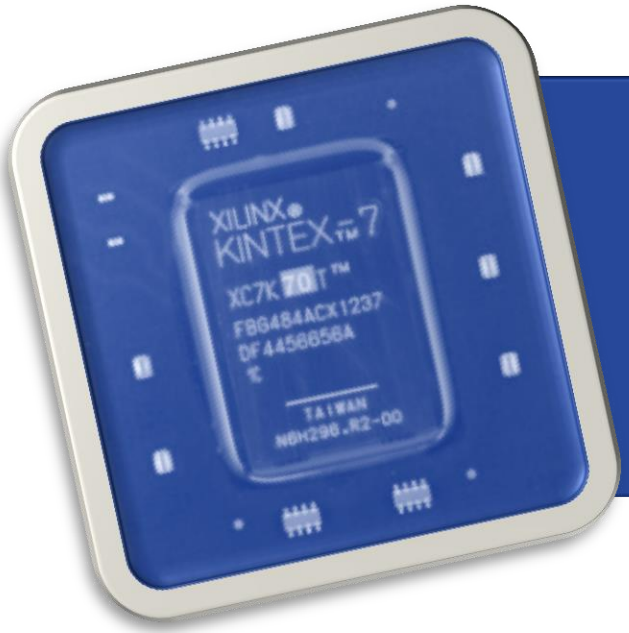

Kintex-7 FPGA radiation hardness studies, test bench, firmware, error mitigation & scrubbing

LHCb Upgrade Electronics
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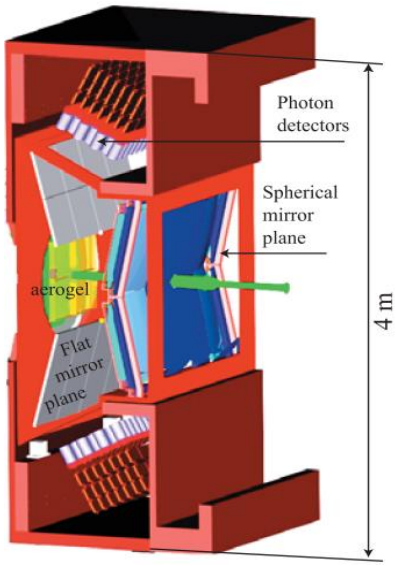
Summary

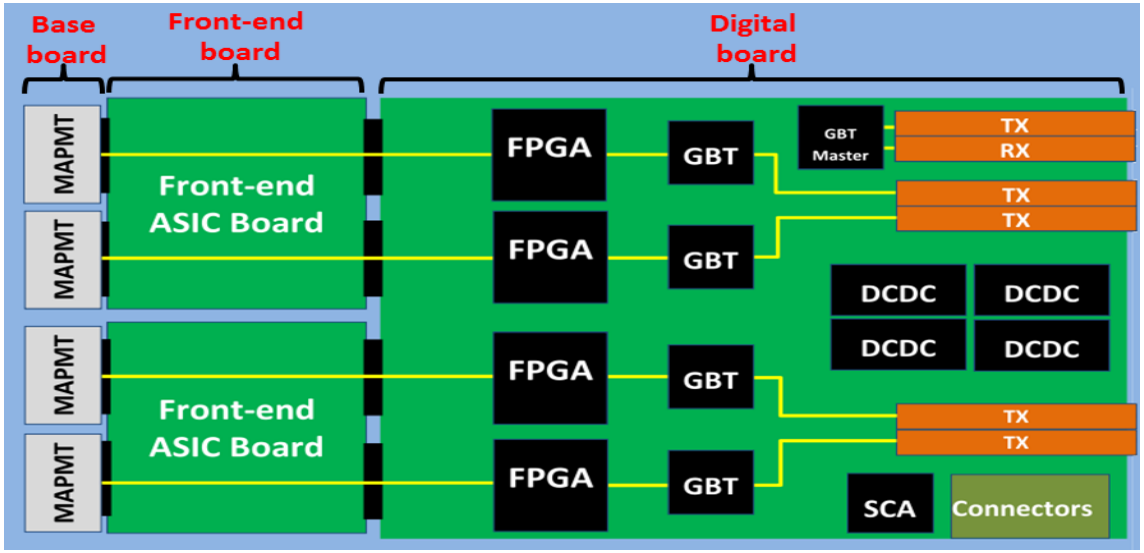
- Introduction
- Setup for irradiation
  - ✓ Hardware
    - Thinning results
  - ✓ GUI
  - ✓ Configuration file
- Heavy ions irradiation
  - Results
- New K7 firmware
  - Scrubbing, mitigation
- Conclusion & Future Work

Introduction

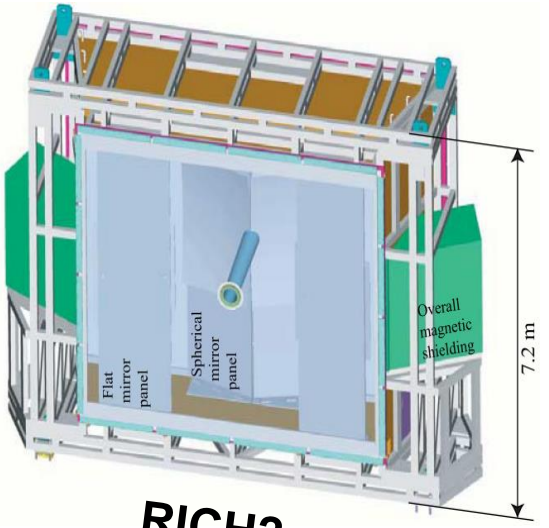
- The RICH photodetectors will be redesign to work at a trigger rate of 40 MHz.
- The Digital Board is intended to be designed is an SRAM based FPGA from KINTEX-7 family.
- *Device considered for the DB:* ***XC7K70T-FBG676***
- *Device Under Test:* ***XC7K70T-FBG484C6***



RICH1



Elementary cell

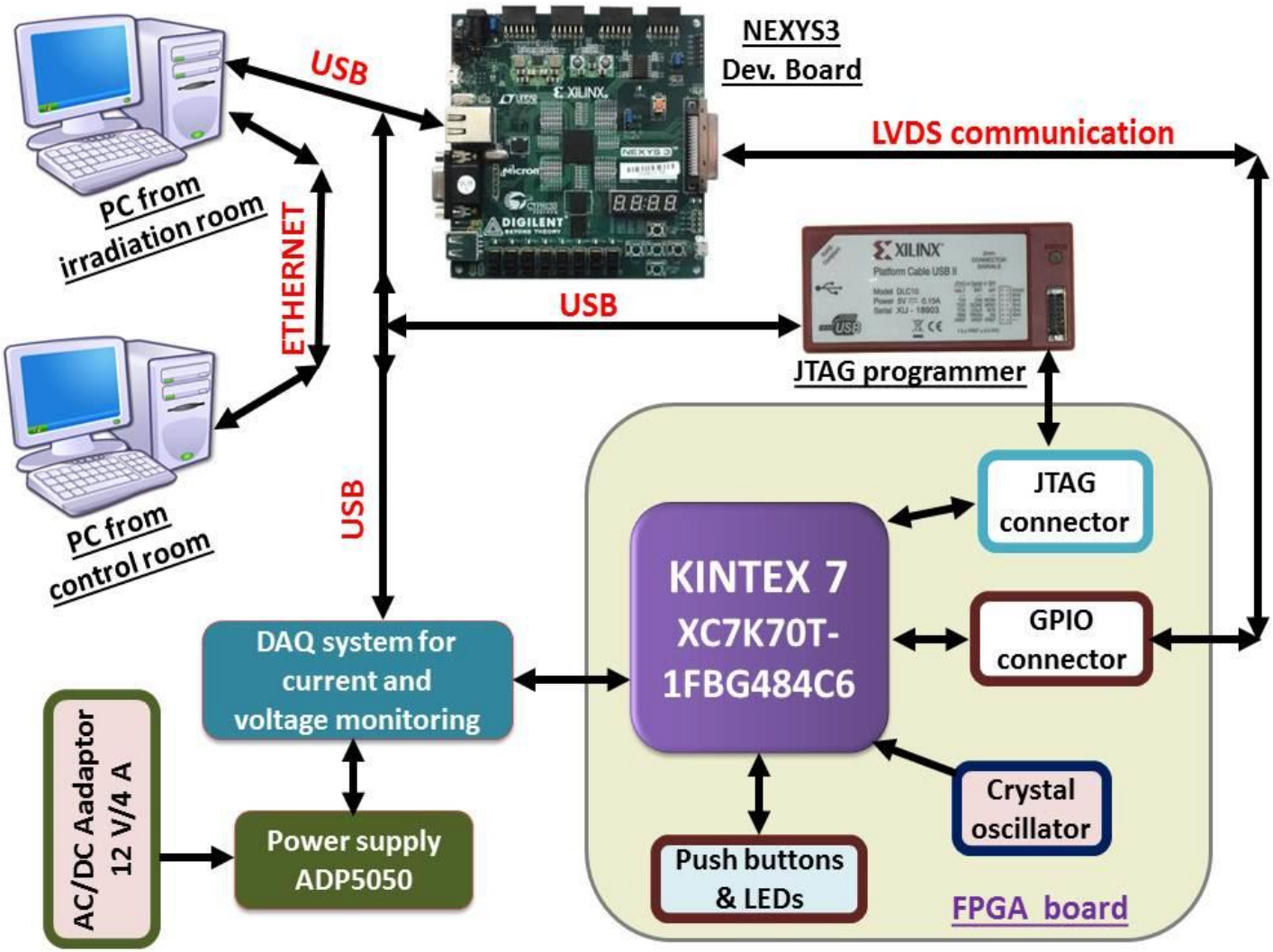


RICH2

Test bench status

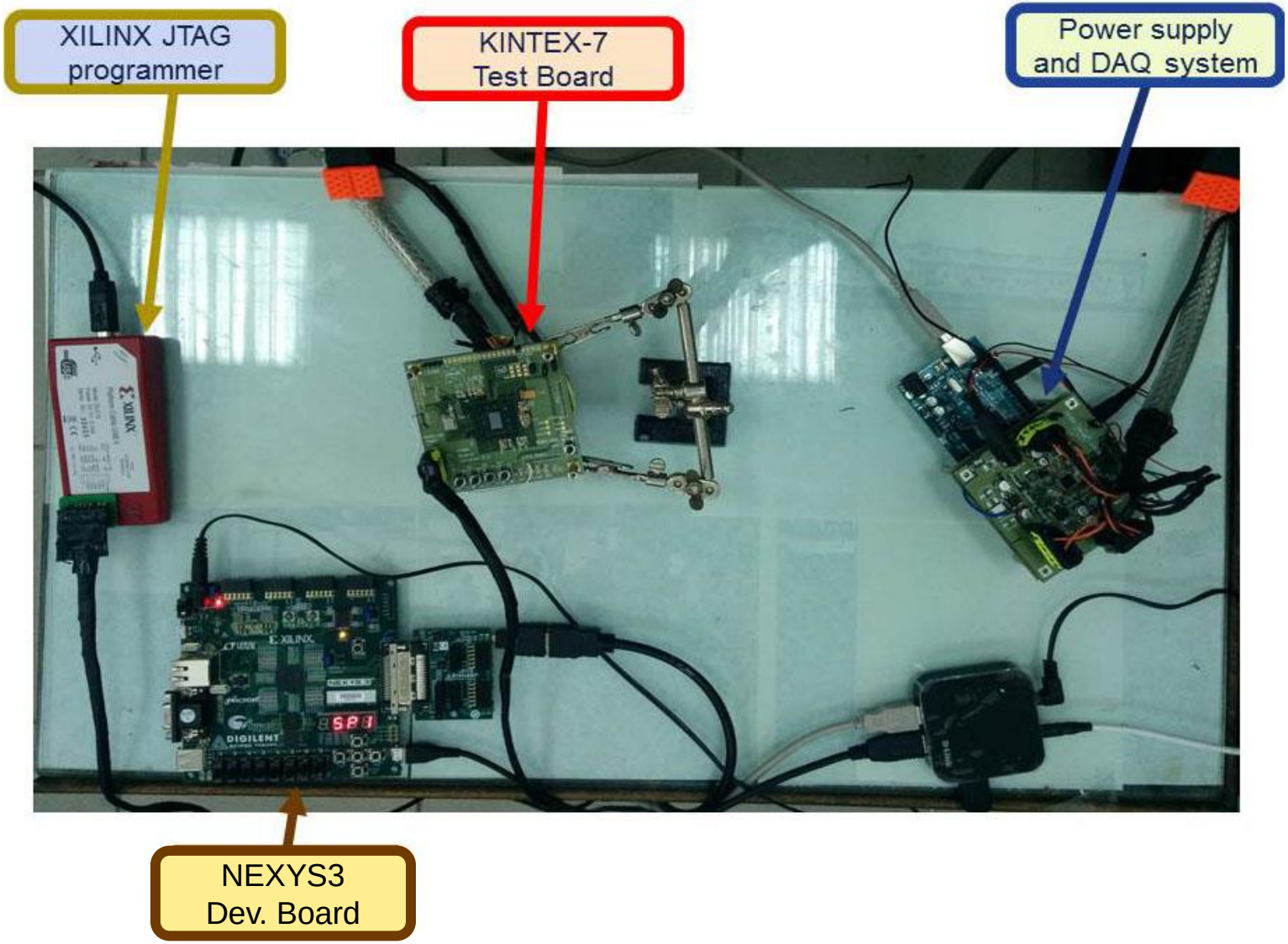
- ***Hardware:*** *7 fully assembled FPGA boards; 4 power supply modules tested on active loads; 2 DAQ boards; 2 Nexys3 dev. board; communication and power supply cables.*
- ***Software:*** *GUI for FPGA power consumption monitoring; GUI for SEU rate reading from the DUT error counters, configuration files for Nexys3 dev. board and KINTEX-7; DUT internal scrubbing using SEM IP core.*
- **Work is in progress to finalize a number of firmware versions for the KINTEX-7 evaluation under radiation.**
- **In the ongoing irradiation campaign plans are made to use mitigation and scrubbing techniques.**

Setup for irradiation (hardware)



The setup architecture for KINTEX7 irradiation

Test bench


XILINX JTAG programmer
KINTEX-7 Test Board
Power supply and DAQ system
NEXYS3 Dev. Board

Thinning results (given by HIREX)

Before

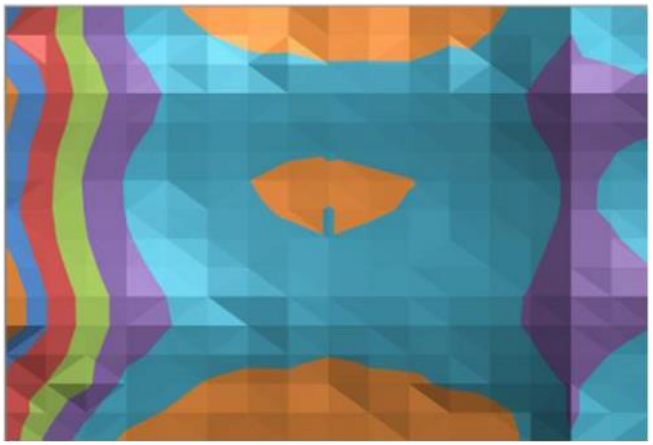
After

- Measurement tool:

IR interferometer with an optical Chrocodil II sensor.

- The measurement grid is 15 x 16 points on the total surface of the die with **0.1 µm resolution**.

Sample_1



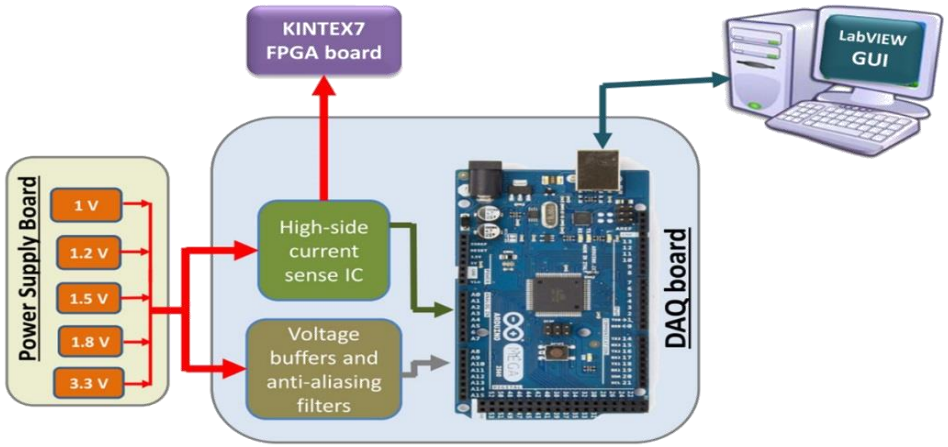
55-60
50-55
45-50
40-45
35-40
30-35
25-30
20-25

Photo # 2 :

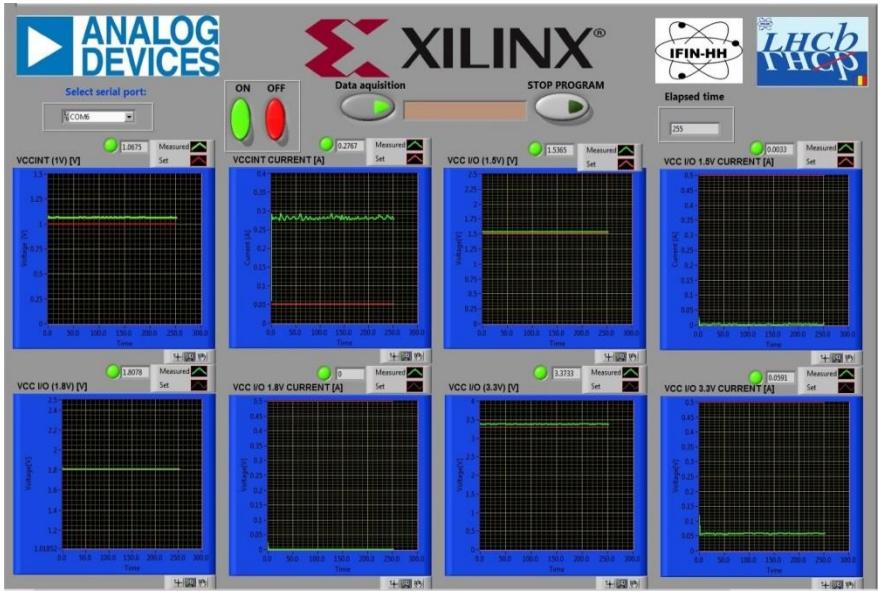
Thickness measurement

SN 1

FPGA power supply monitoring system



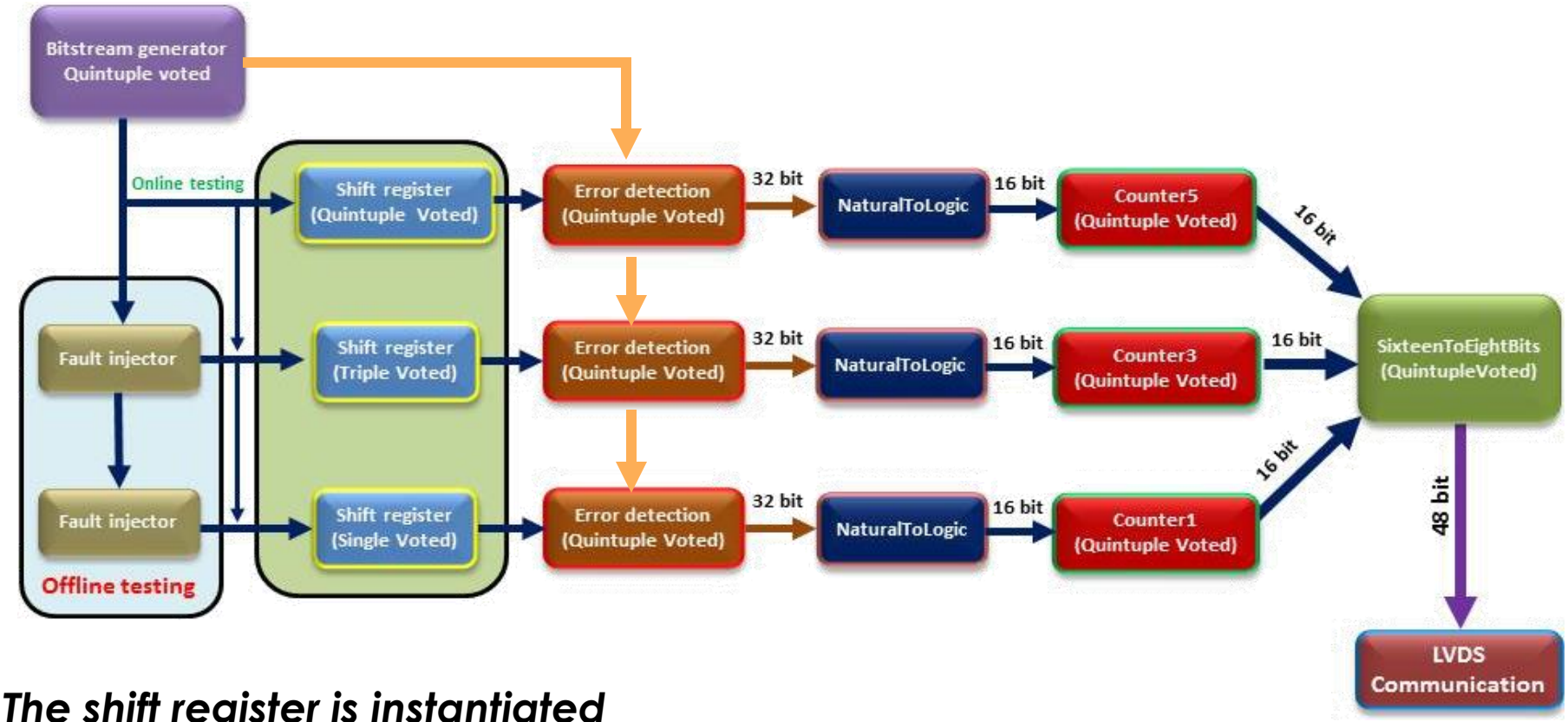
DAQ for FPGA power consumption monitoring



DAQ system GUI

- A custom DAQ system monitors 4 power of the Kintex-7 FPGA.
- Data are displayed to a GUI and saved into ASCII file.
- The FPGA board power supply is automatically cutoff when monitored parameters excide the user defined threshold.

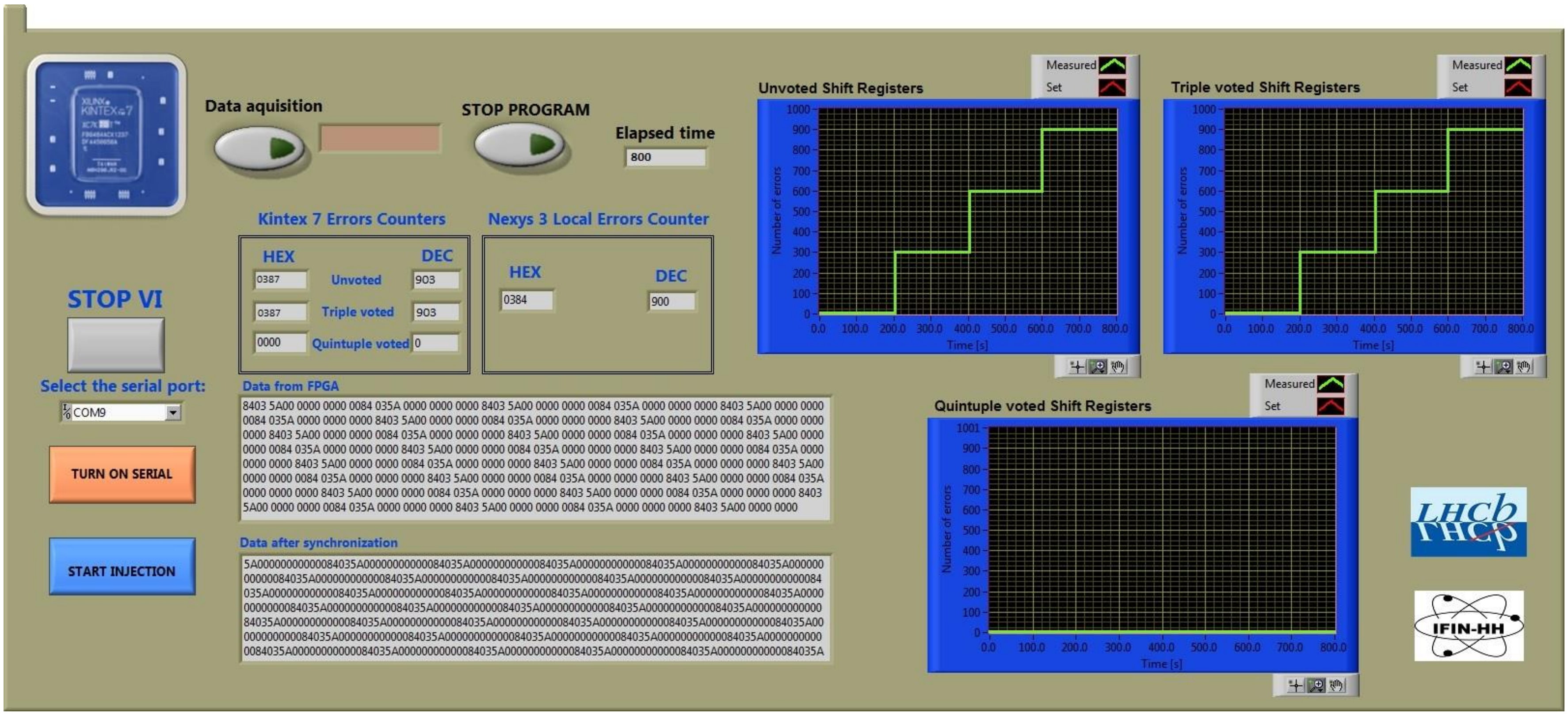
FPGA Configuration file



The shift register is instantiated multiple times to cover most of available FPGA surface.

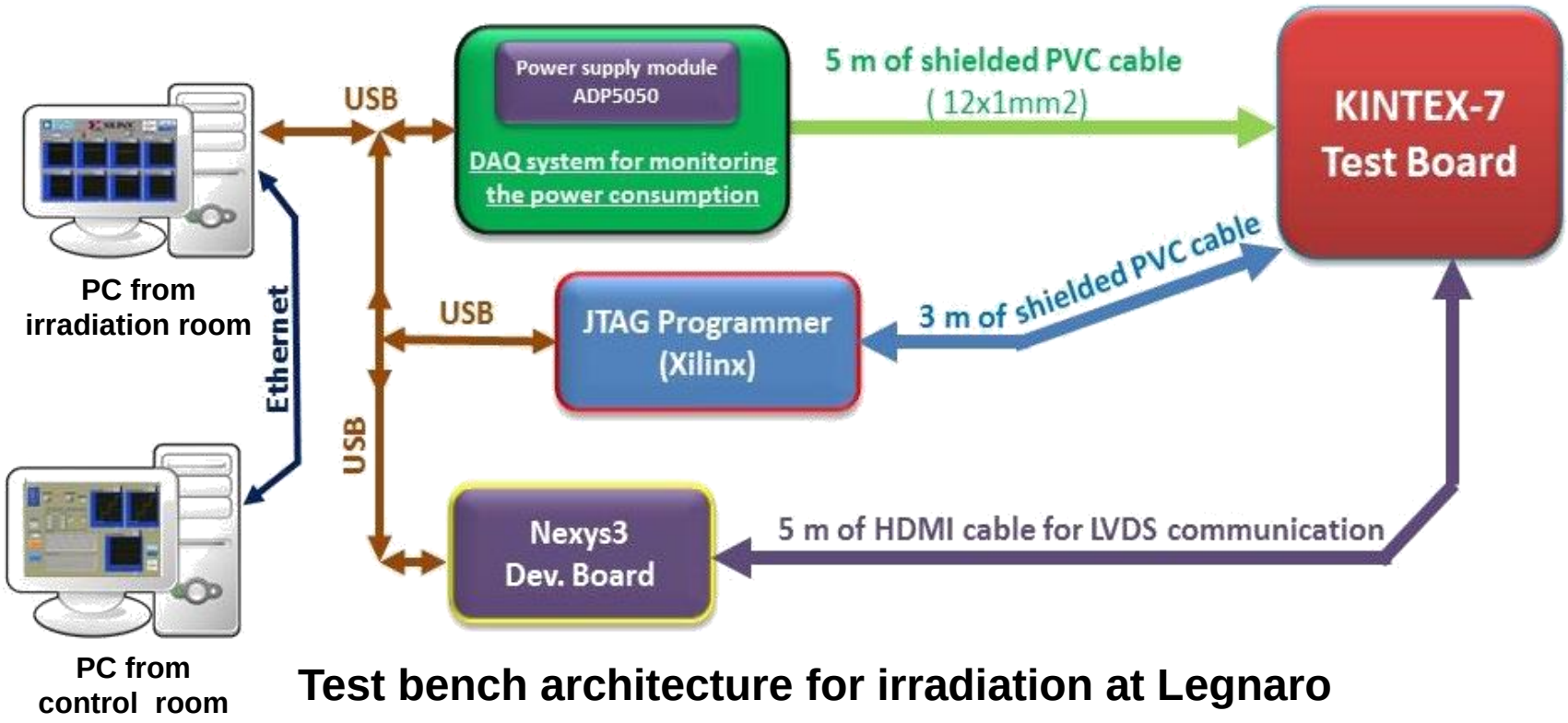
The VHDL software architecture implemented by Lukas Arnold.

LabVIEW GUI for SEU counting



- The GUI is designed to drop date into ASCII file.
- For offline test the KINTEX7 fault injector starts with one system clock earlier than the error counter implemented locally on NEXYS3.

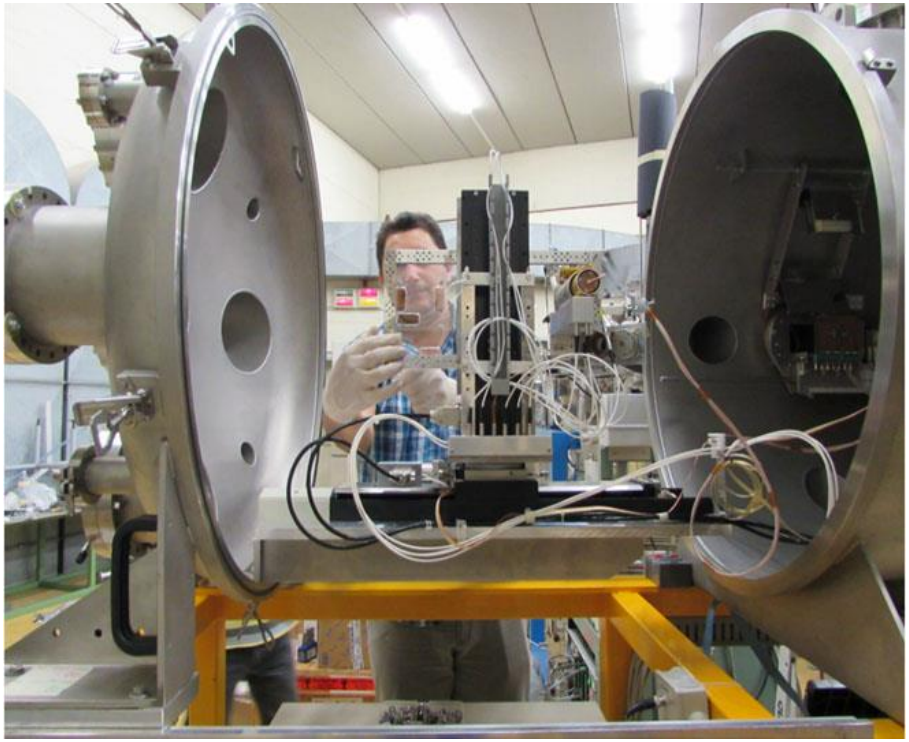
Setup for irradiation (hardware)



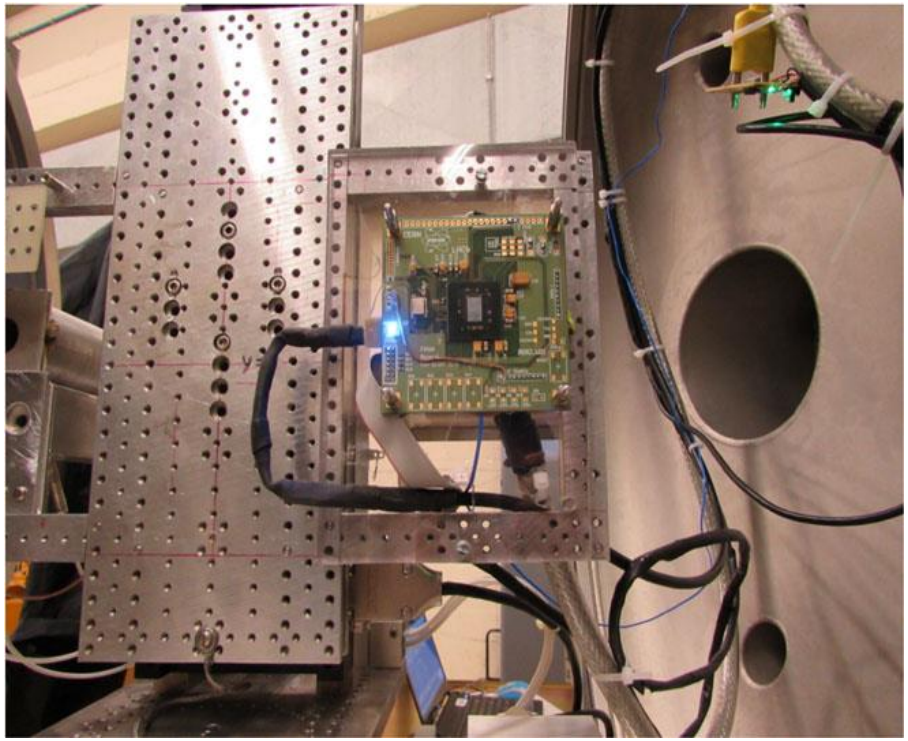
Test bench architecture for irradiation at Legnaro

- The NEXYS3 dev. board sends data to PC over an virtual RS232 COM port with a **baud rate** of **19.2 kbps** and the **KINTEX-7 internal errors counters content (48 bits) is read at every 3.7 ms.**
- **All cable in irradiation setup are shielded.**

Legnaro irradiation with Oxygen and Fluorine ions



Vacuum vessel in open position



Kintex-7 board residing on target support

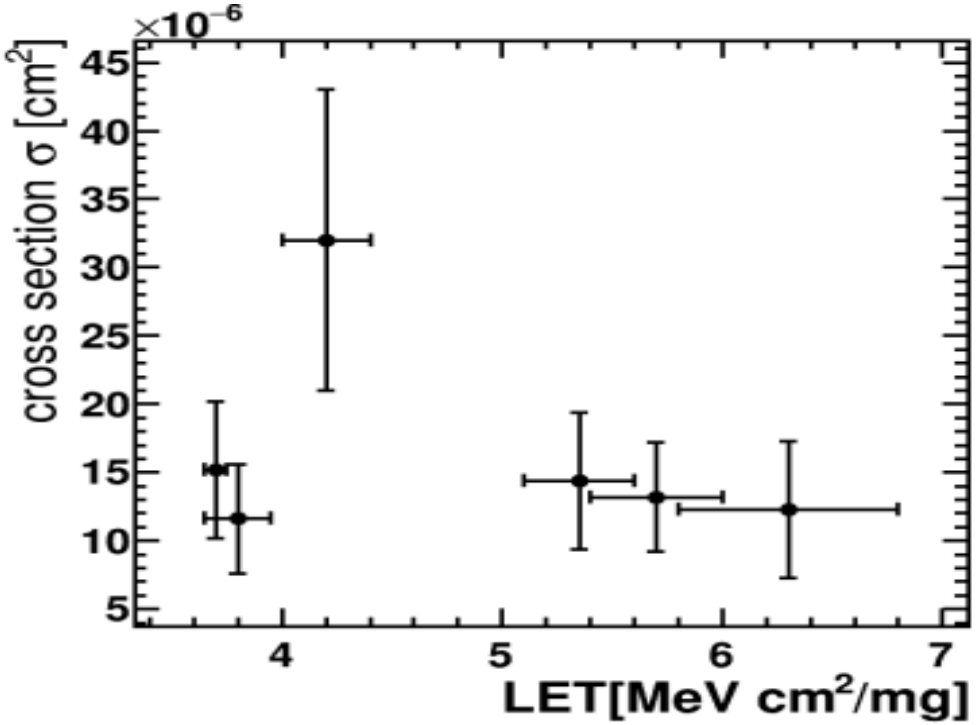
Irradiation with heavy ions

(Florin's talk)

- *Oxygen A=18 beam at 126 MeV and Fluorine A=19 at 118 MeV.*
- *LET or stopping power in range of 3.5-7 $MeV\ cm^2/mg$ for $0^0 - 45^0$ with respect to the beam.*
  - *Intermediate fluency of few thousand to hundreds ions per cm^2.*
- First measurement revealed a lot of SEU in few FPGA running seconds, and no difference was observed in the number of errors outcoming from simple, triple as well quintuple voted logic.
- We decrease the beam fluency to tens of ions per cm^2/s *as well as the* flip-flop occupancy on FPGA to 1-2 %. New SEU rate corresponds to one per few tens of seconds.

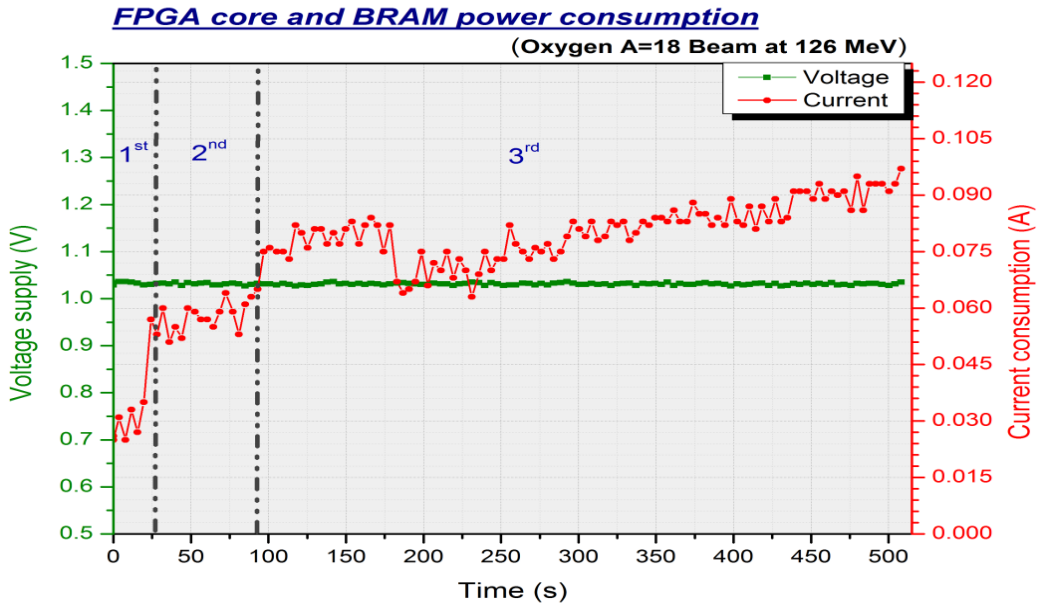
Results (Florin's talk)

- Cross-section of SEU at various LET values for Oxygen and Fluorine beams,



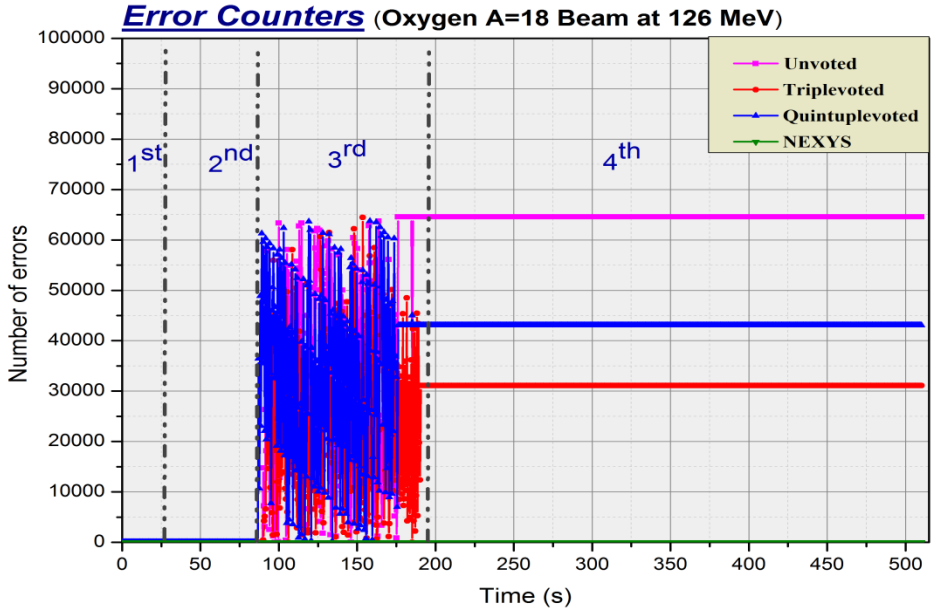
- Lack of scrubbing and unefficient mitigation technique led to more than 4 orders of magnitude difference between our values comparing to literature similar measurements.

Results



Current consumption variation:

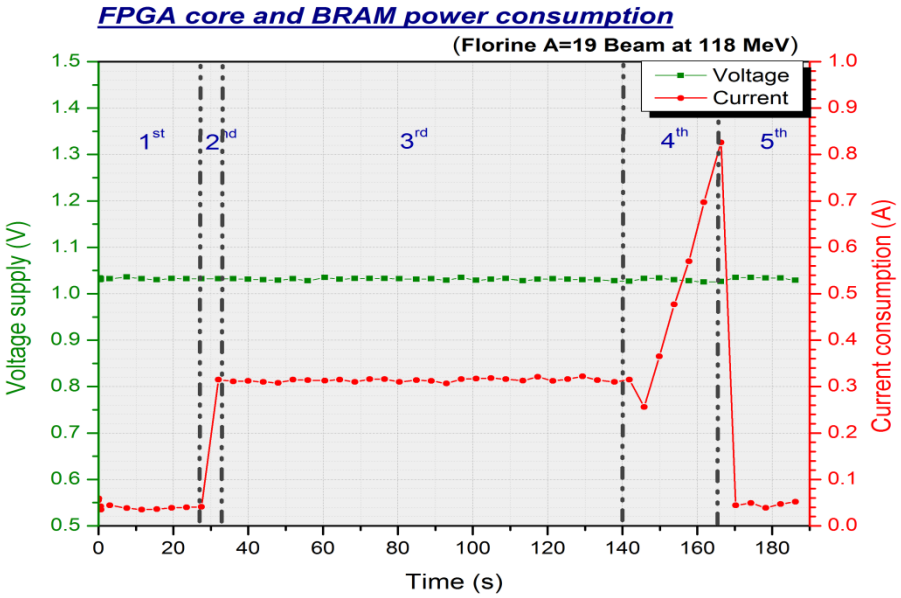
1) *device unprogrammed;*
2) *firmware download in FPGA;*
3) *operation under radiation.*

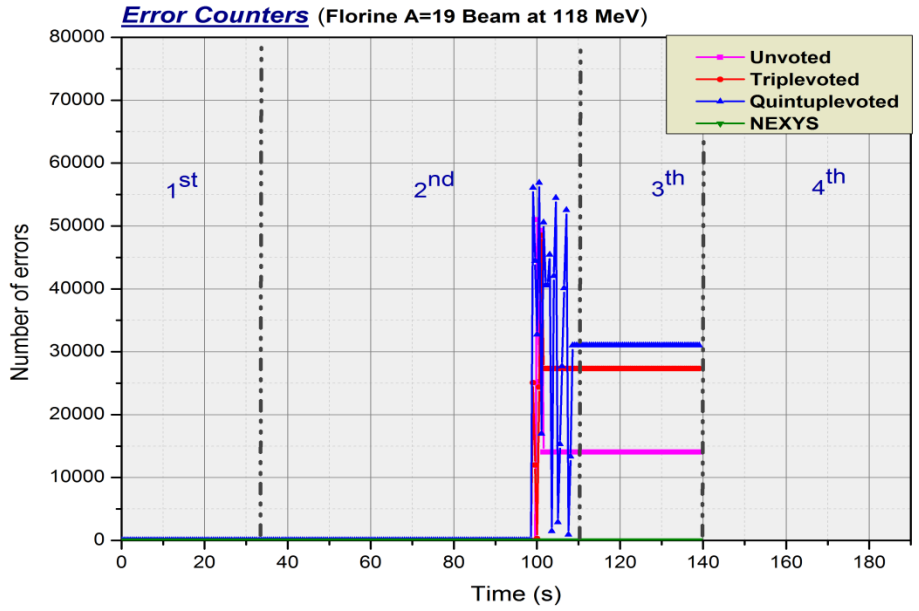


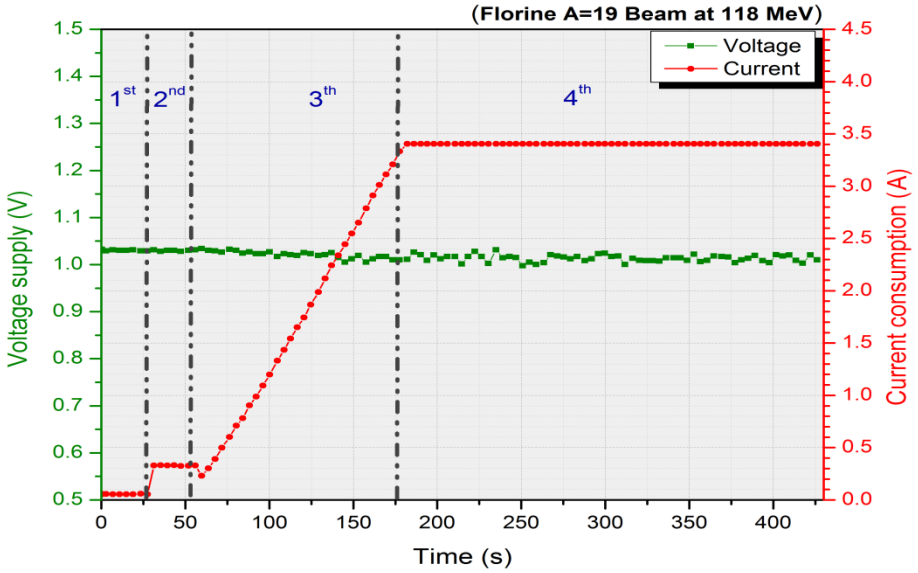
SEU counting:

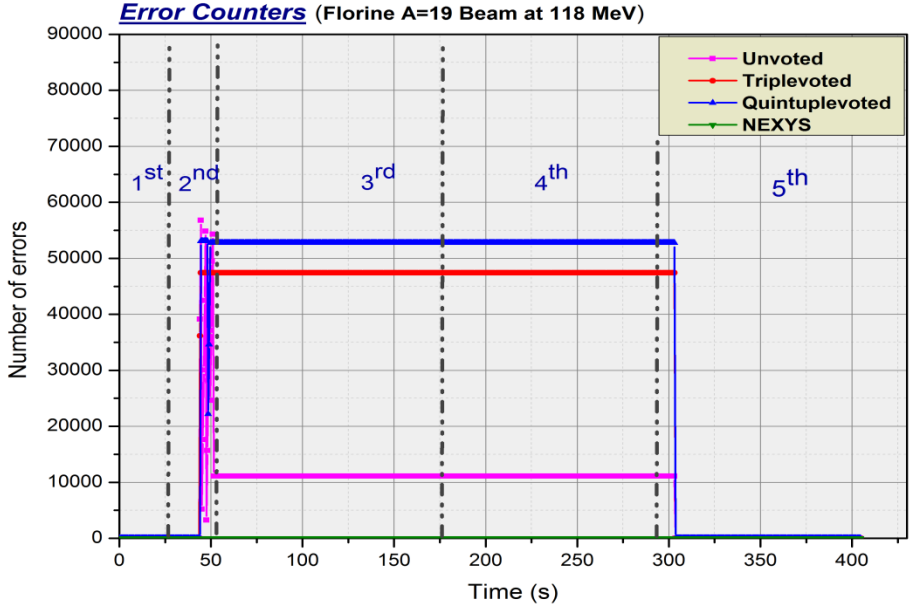
1-2) Kintex-7 configuration,
3) data taking;
4) configuration is corrupted.

Results

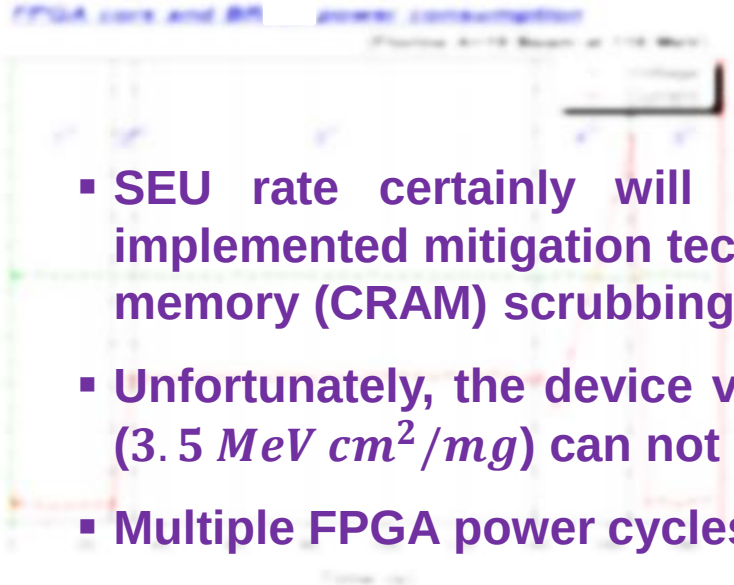

FPGA core and BRAM power consumption
(Florine A=19 Beam at 118 MeV)
Voltage
Current
1st
2nd
3rd
4th
5th
Voltage supply (V)
Current consumption (A)
Time (s)

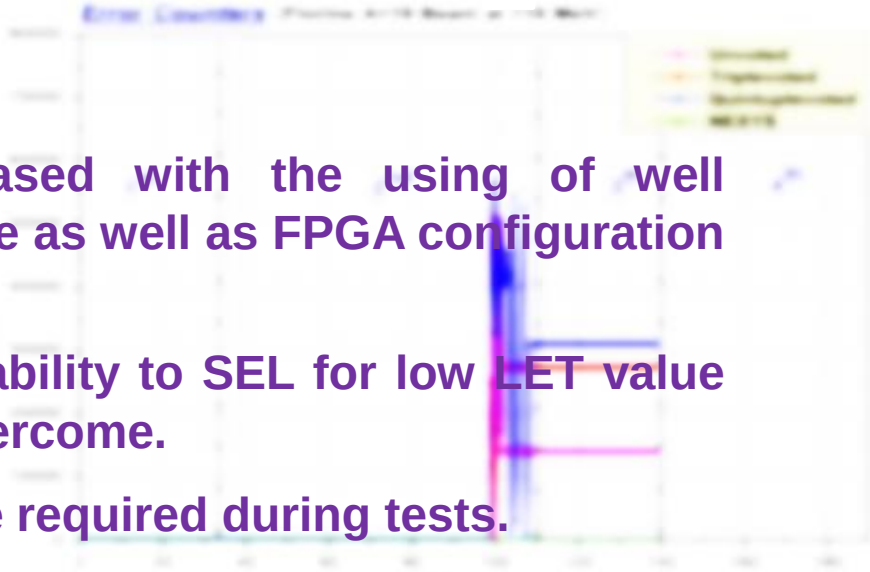

Error Counters (Florine A=19 Beam at 118 MeV)
Unvoted
Triplevoted
Quintuplevoted
NEXYS
1st
2nd
3th
4th
Number of errors
Time (s)


FPGA core and BRAM power consumption
(Florine A=19 Beam at 118 MeV)
Voltage
Current
1st
2nd
3th
4th
Voltage supply (V)
Current consumption (A)
Time (s)

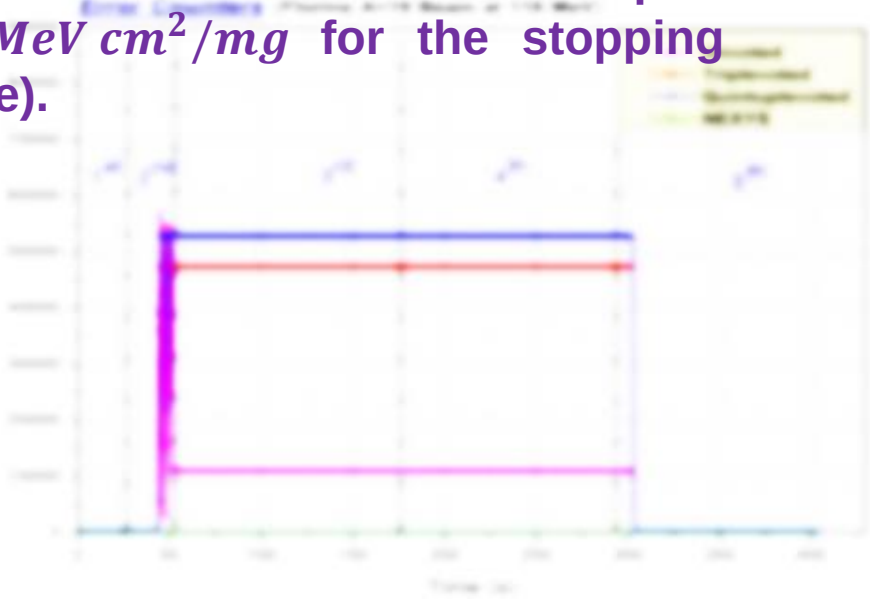

Error Counters (Florine A=19 Beam at 118 MeV)
Unvoted
Triplevoted
Quintuplevoted
NEXYS
1st
2nd
3rd
4th
5th
Number of errors
Time (s)

Results





- SEU rate certainly will decreased with the using of well implemented mitigation technique as well as FPGA configuration memory (CRAM) scrubbing.
- Unfortunately, the device vulnerability to SEL for low LET value ($3.5\ MeV\ cm^2/mg$) can not be overcome.
- Multiple FPGA power cycles were required during tests.
- In literature, similar tests on XC7K325T-1FBG900C Kintex-7 part highlighted a threshold of $15\ MeV\ cm^2/mg$ for the stopping power (it is no space grade device).

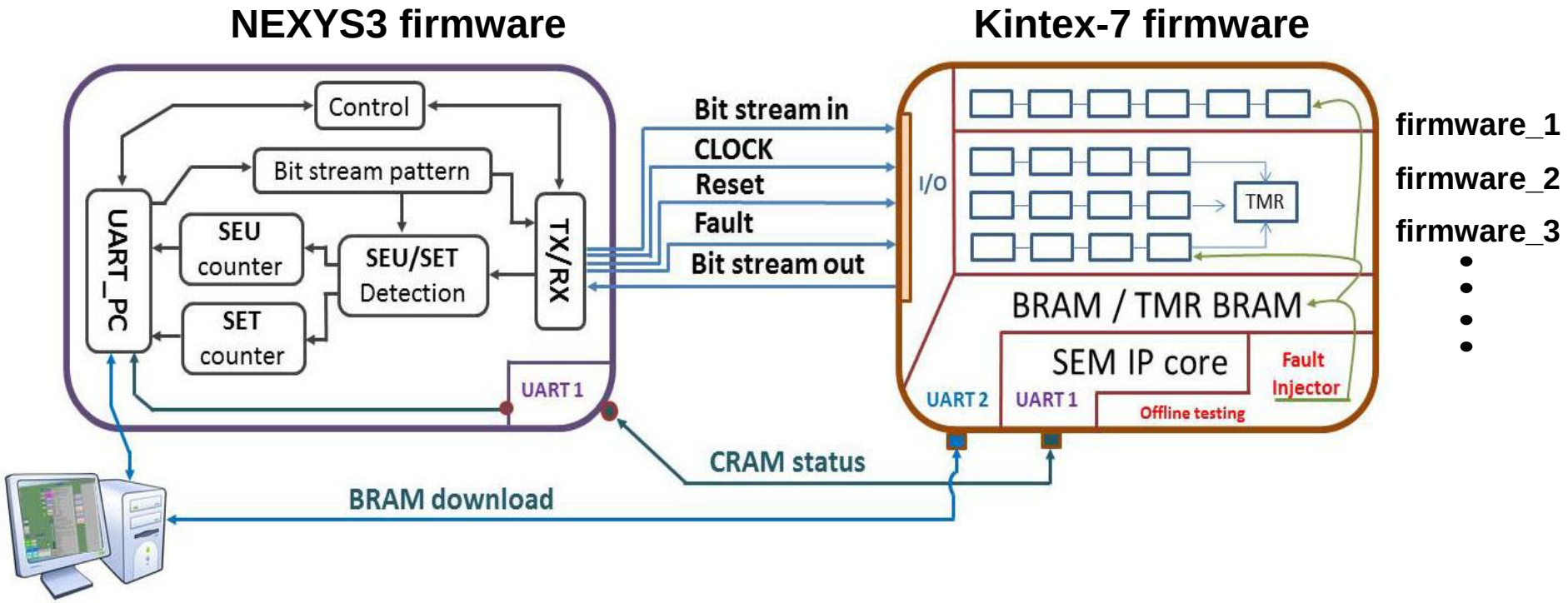


New K7 firmware

- The basic concept was to implement a number of firmware versions for the DUT testing by keeping the logic architecture as simple as possible**.**
- Each firmware is designed for testing specific FPGA resources like: SLR32, flip-flops and BRAM.
- We used the TMR as basic mitigation technique.
- Every version of firmware is governed by SEM IP core to ensure a better DUT evaluation during irradiation test.
- Routing constrains were used to place de logic on well defined FPGA dice region.
- A blind scrubbing procedure is implemented to be triggered in case of SEM IP core crush or MBU on single CRAM frame**.**

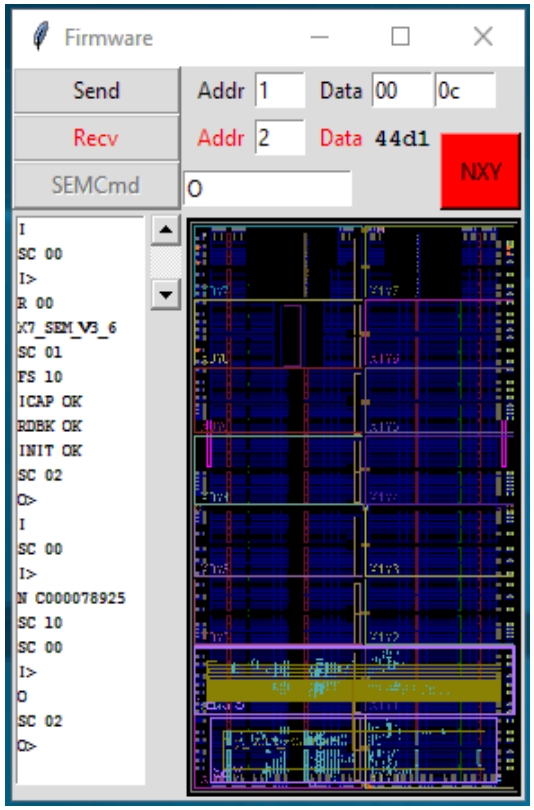
- **SEM IP core:** www.xilinx.com/products/intellectual-property/sem.html
- **SLR32:** SLICEM slice look-up tables (LUT) configured as shift-register
- **BRAM:** FPGA Block RAM
- **CRAM:** FPGA Configuration Memory
- **MBU:** Multiple-Bit Upset

New K7 firmware

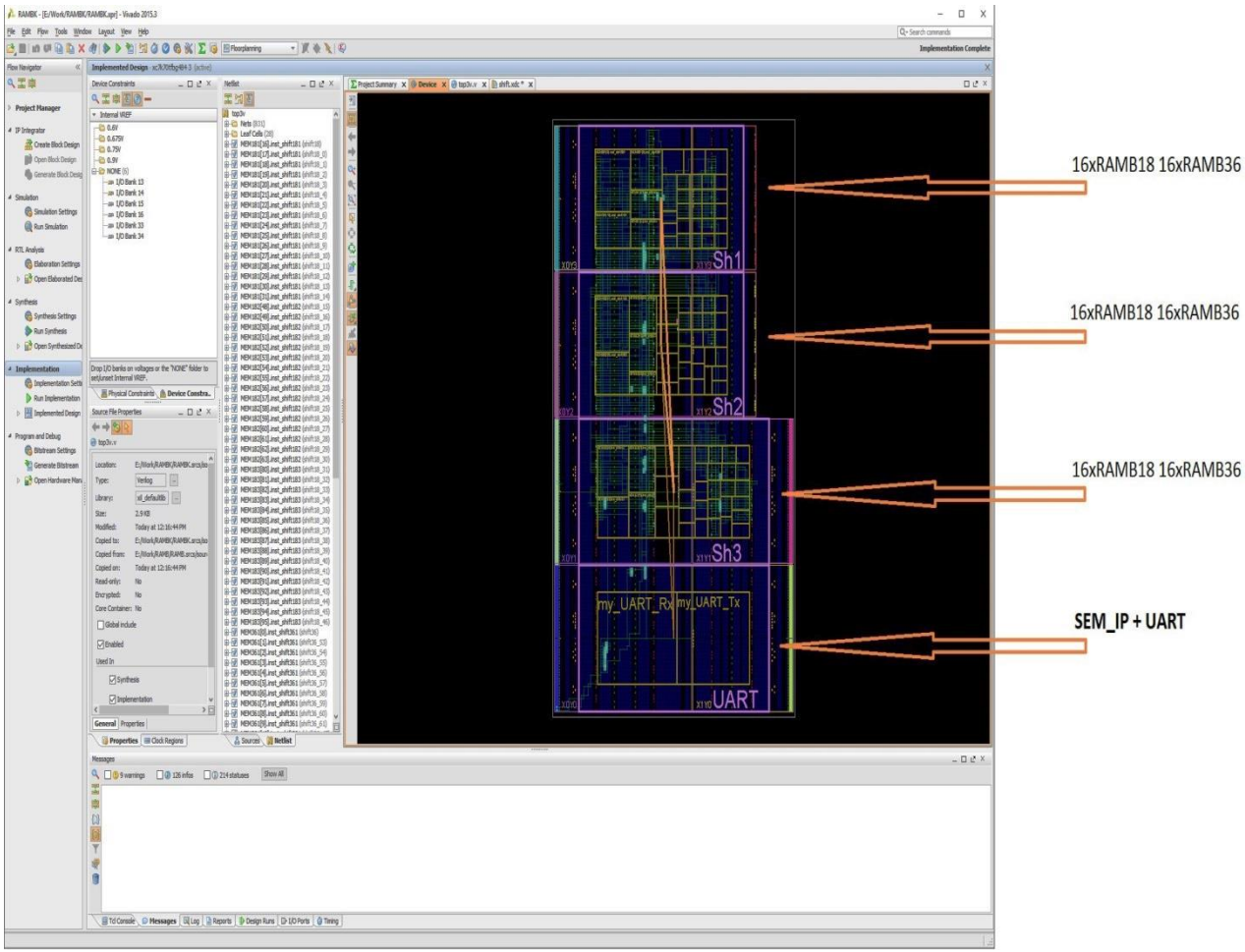


- SLR32 and flip- flops radiation tolerance will be tested using single and triple voted logic configuration.
- BRAM contents will be downloaded trough a separate UART at every half a second during irradiation procedure and stored in ASCII files for later analysis.
  - **UART:** Universal Asynchronous Receiver/Transmitter interface

New K7 firmware



SEM IP core GUI recently implemented



PlanAhead Design Tool

New K7 firmware

Firmware	Shift Registers testing	Notes
1:	Single voted Shift Registers with SLR32 plus SEM IP core	v
2:	TMR Shift Registers with SLR32 plus SEM IP core	v
3:	Single voted Shift Registers with FD plus SEM IP core	v
4:	TMR shift Registers with FD plus SEM IP core	v

BRAM testing		
5:	Single voted BRAM	v
6:	TMR BRAM	v
7:	Single voted BRAM plus SEM IP core	in progress
8:	TMR BRAM plus SEM IP core	in progress

- ***By default the FPGA configuration memory (CRAM) will be tested under radiation along with above firmware versions.***

New K7 firmware

Upcoming versions of firmware take into consideration to be implemented:

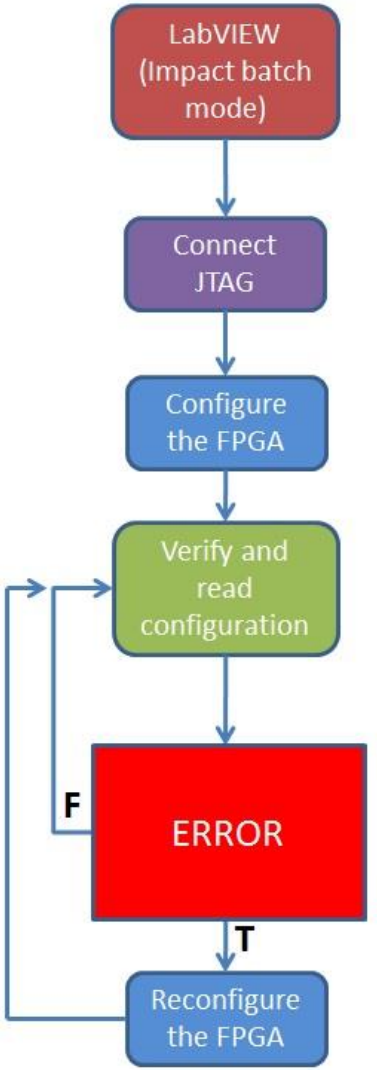
Firmware_1: FPGA I/O banks testing
Shift Registers testing
Firmware_2: Single voted Shift Registers with SLR32
Firmware_3: TMR Shift Registers with SLR32
Firmware_4: Single voted Shift Registers with FD
Firmware_5: TMR Shift Registers with FD
Firmware_6: Shift Registers with Fault Injector for offline tests
BRAM testing
Firmware_7: BRAM with Fault Injector for offline tests

Scrubbing & read back via JTAG

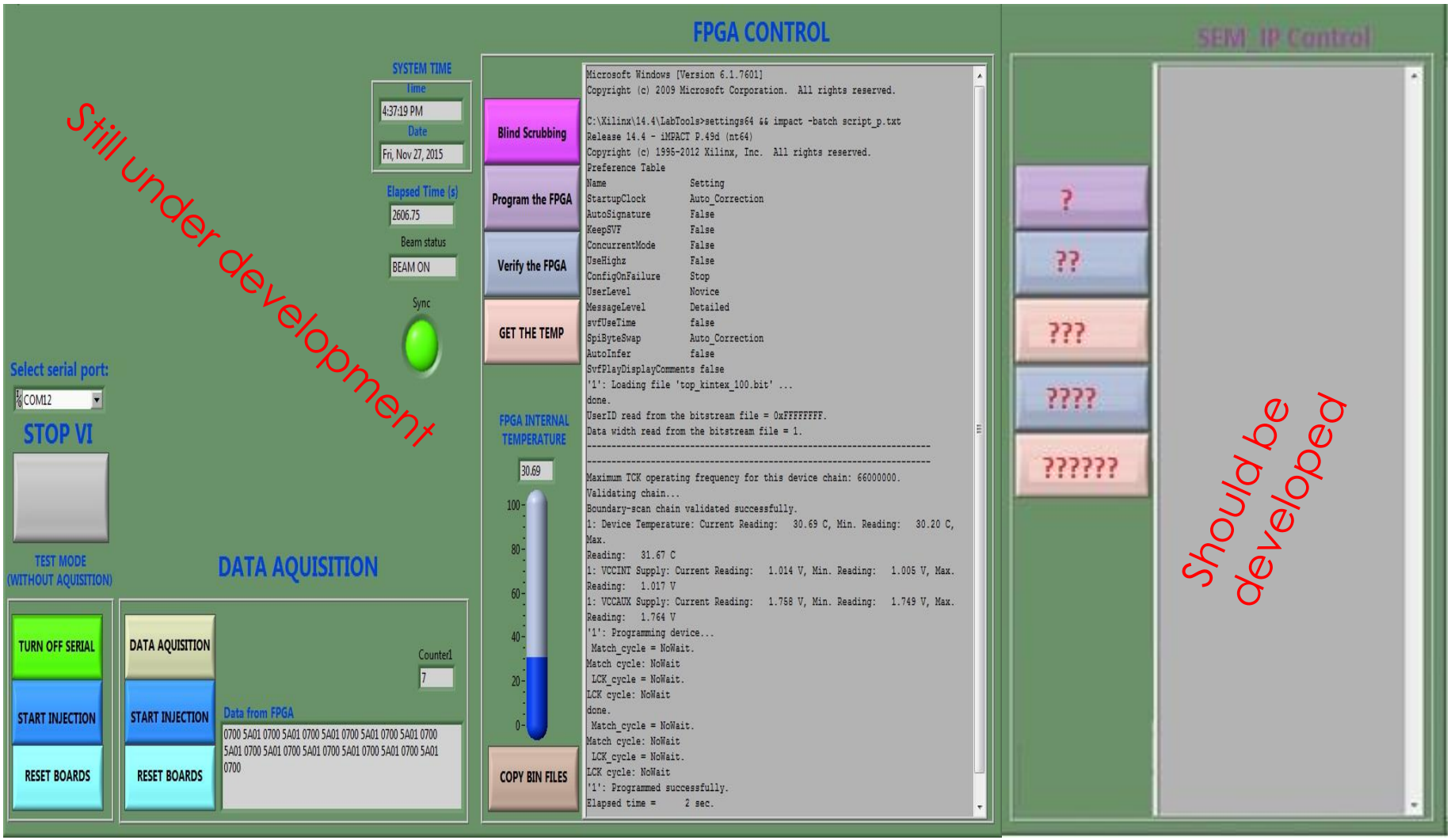
(Vlad's talk)

- A new LabVIEW GUI embeds:
  - ✓ SEU/SET counters readout;
  - ✓ **Impact batch mode**;
  - ✓ **SEM IP core** user interface.

- The LabVIEW GUI features:
  - Reconfigure the FPGA in about 1s;
  - Verify the content of configuration memory in about 2s;
  - Save the readback data in to a binary file for later analyses;
  - Read the internal FPGA temperature through JTAG interface;
  - It has SEM IP core control / status commands;
  - Trigger blind scrubbing procedure.



New GUI for SEU/SET readout and FPGA/SEM IP control



Conclusion & Future work

- **Heavy ions irradiation proved the device to be unstable, unreliable and sensible even at low LET value ($3.5\ MeV\ cm^2/mg$).**
- ***New firmware:*** *for NEXYS3 is finalized, while for the KINTEX-7 several versions of firmware are still under development. This time we will have a better control and debugging expertise on K7 behavior during tests. As firmware features we added SEM IP core and TMR.*
- ***New GUI:*** *embedding the SEM IP control / status commands as well as Impact batch mode for blind scrubbing and FPGA read back*.
- At the end of March we will be ready to irradiate KINTEX-7 at Krakow or Legnaro, depending on facilities availability.
- We intended to use 3 board with *"standard" FPGA chips for proton irradiation.*
- *Other 4 board assembled with thinned FPGA dices are reserved for heavy ion irradiation at Legnaro or/and Louvain .*

Backup slides

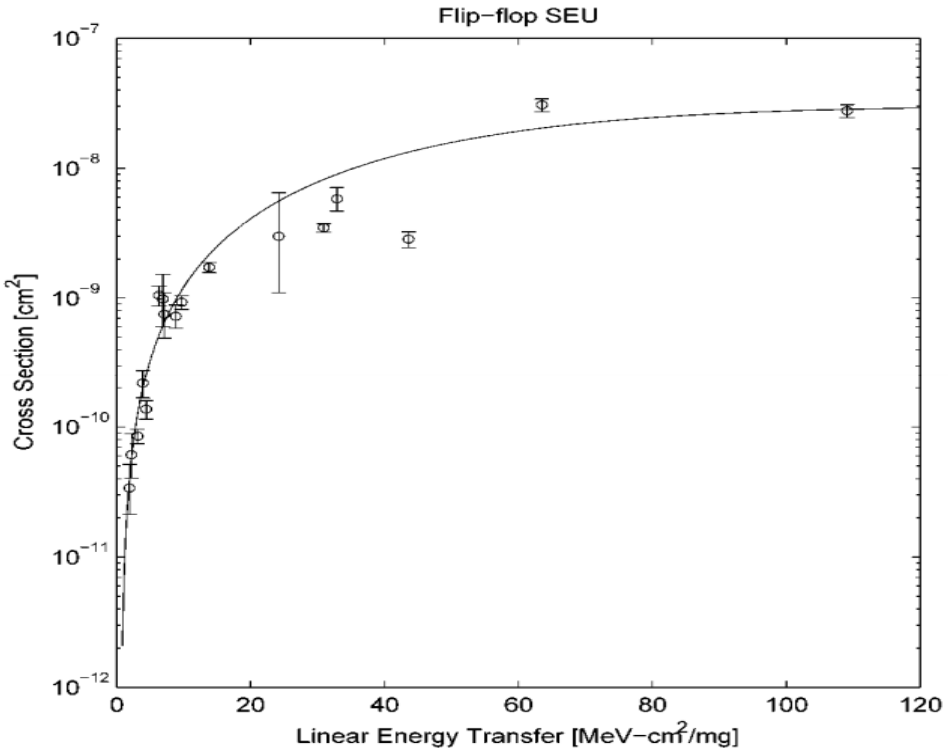


Fig. 3. Flip-flop memory cell SEU event Weibull curve. L_{th}=0.6 [MeV-cm^2/mg], σ_{sat}=3.0e-8 [cm^2/bit], W=58.4 [MeV-cm^2/mg], S=1.74.

Results from Sandia group associates of Xilinx

D. S. Lee, M. Wirthlin, G. Swift, and A. C. Le, "Single-Event Characterization of the 28 nm Xilinx Kintex-7 Field-Programmable Gate Array under Heavy Ion Irradiation," *Radiation Effects Data Workshop (REDW)*, pp. 1-5, 2014