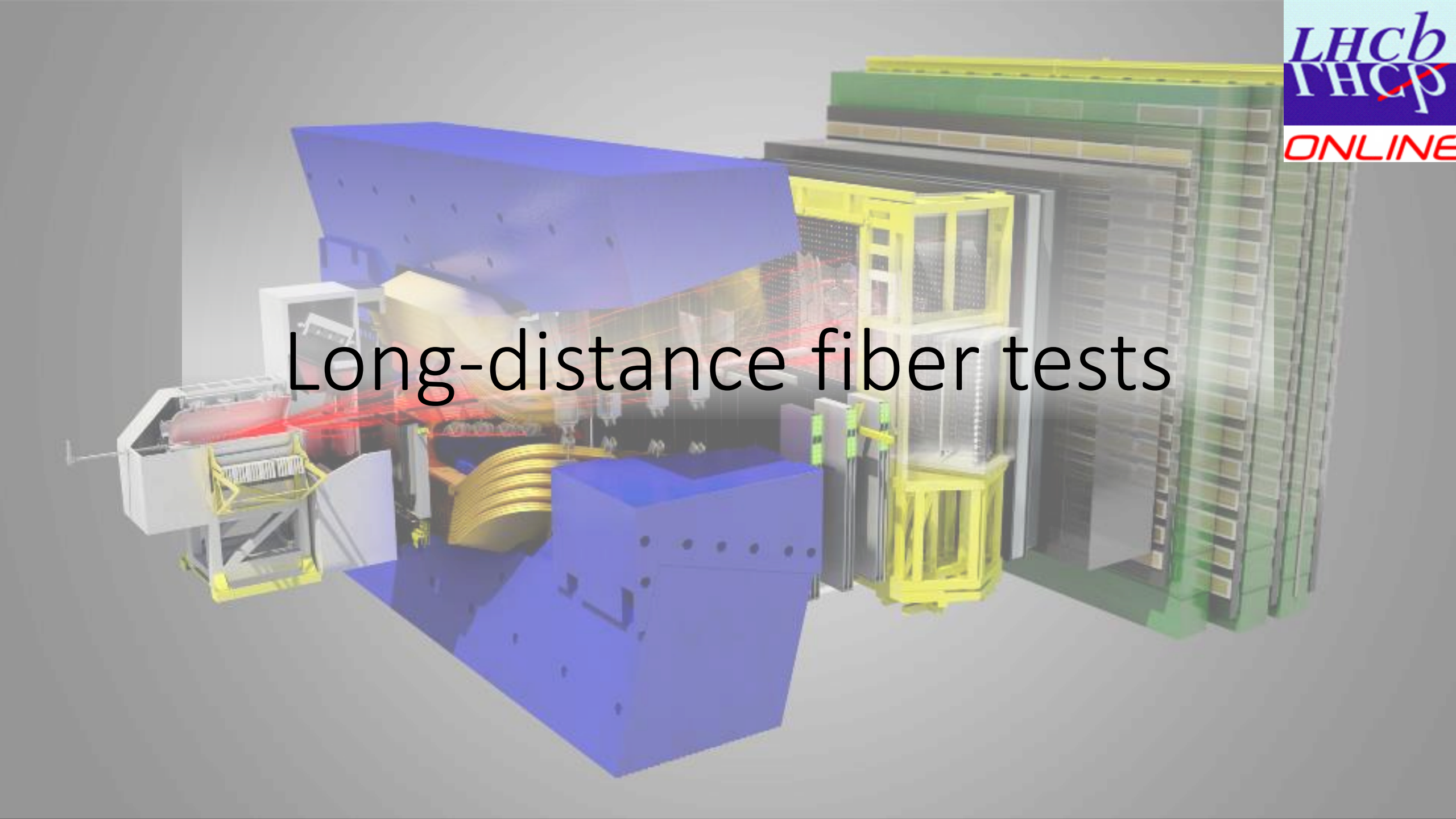
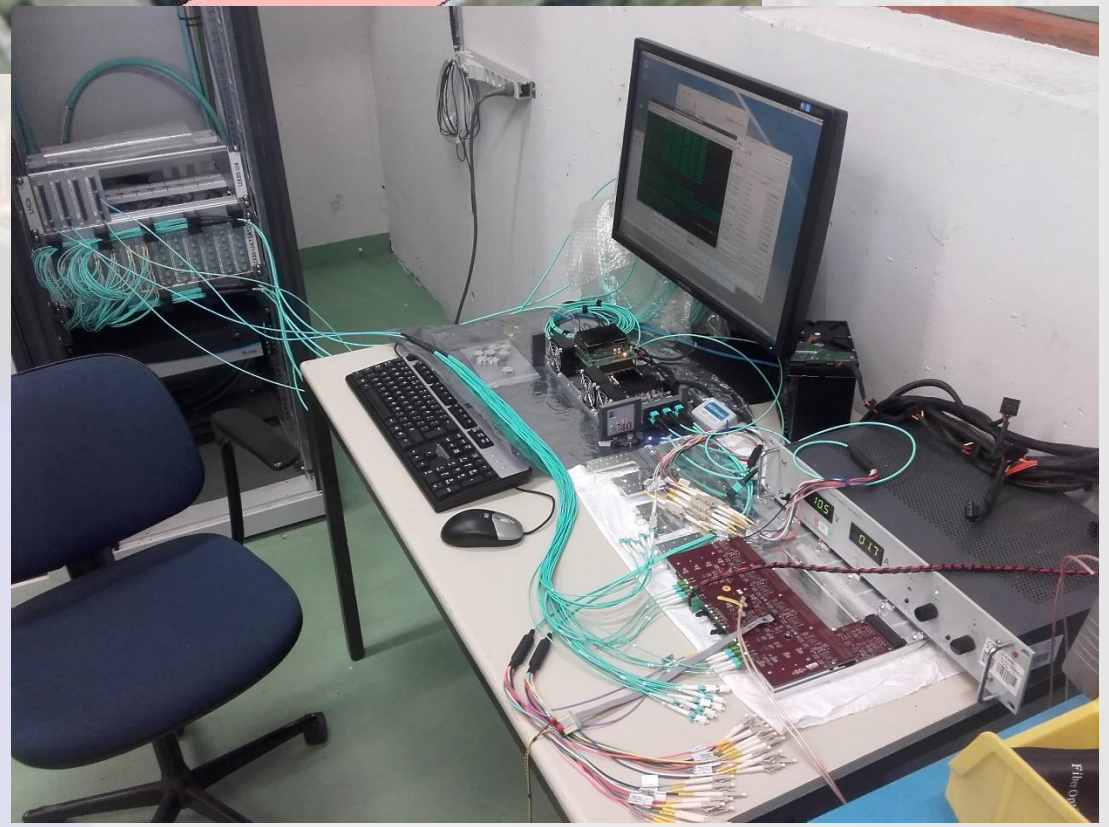


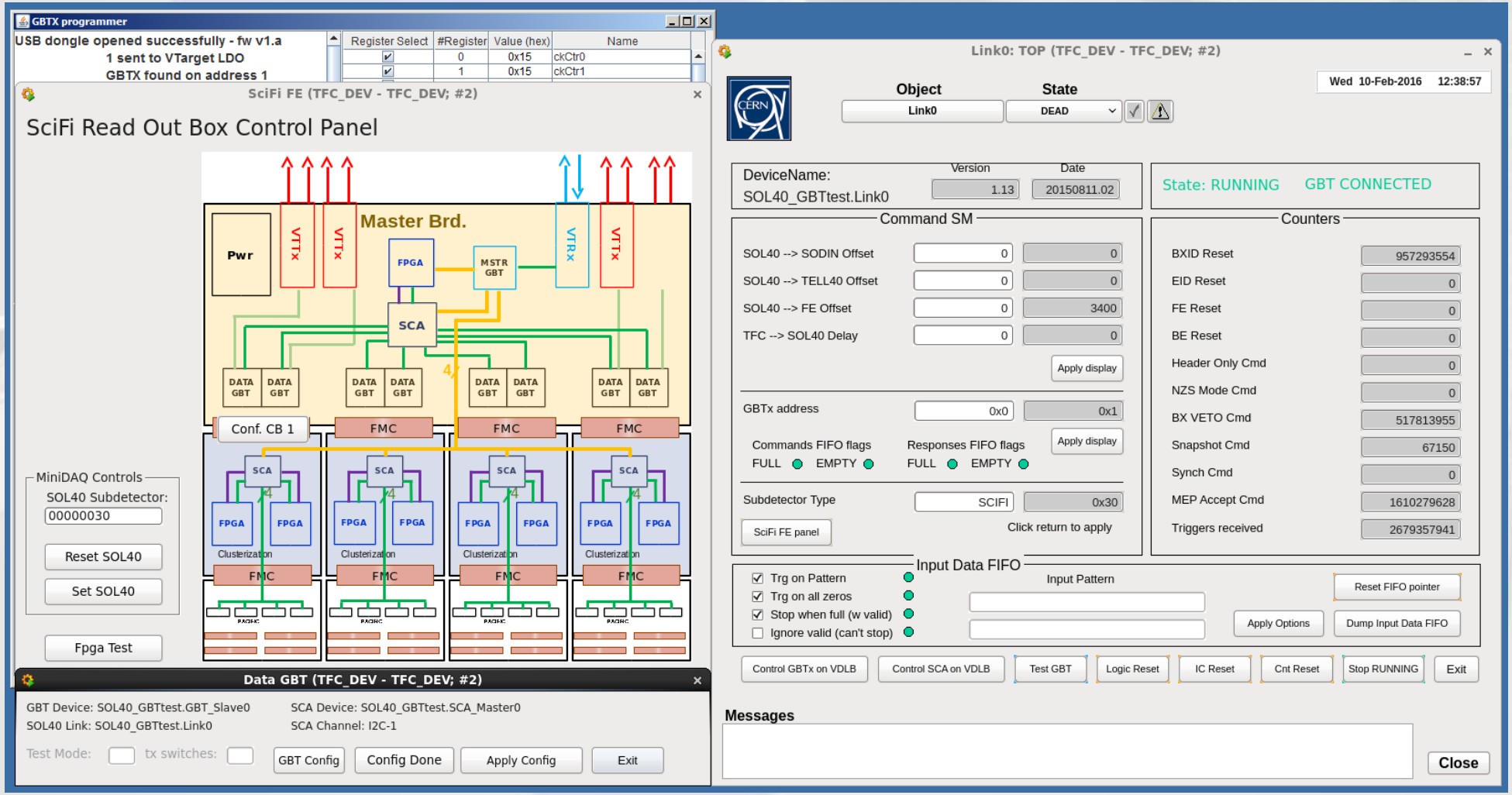
Long-distance fiber tests

Setup in SG8

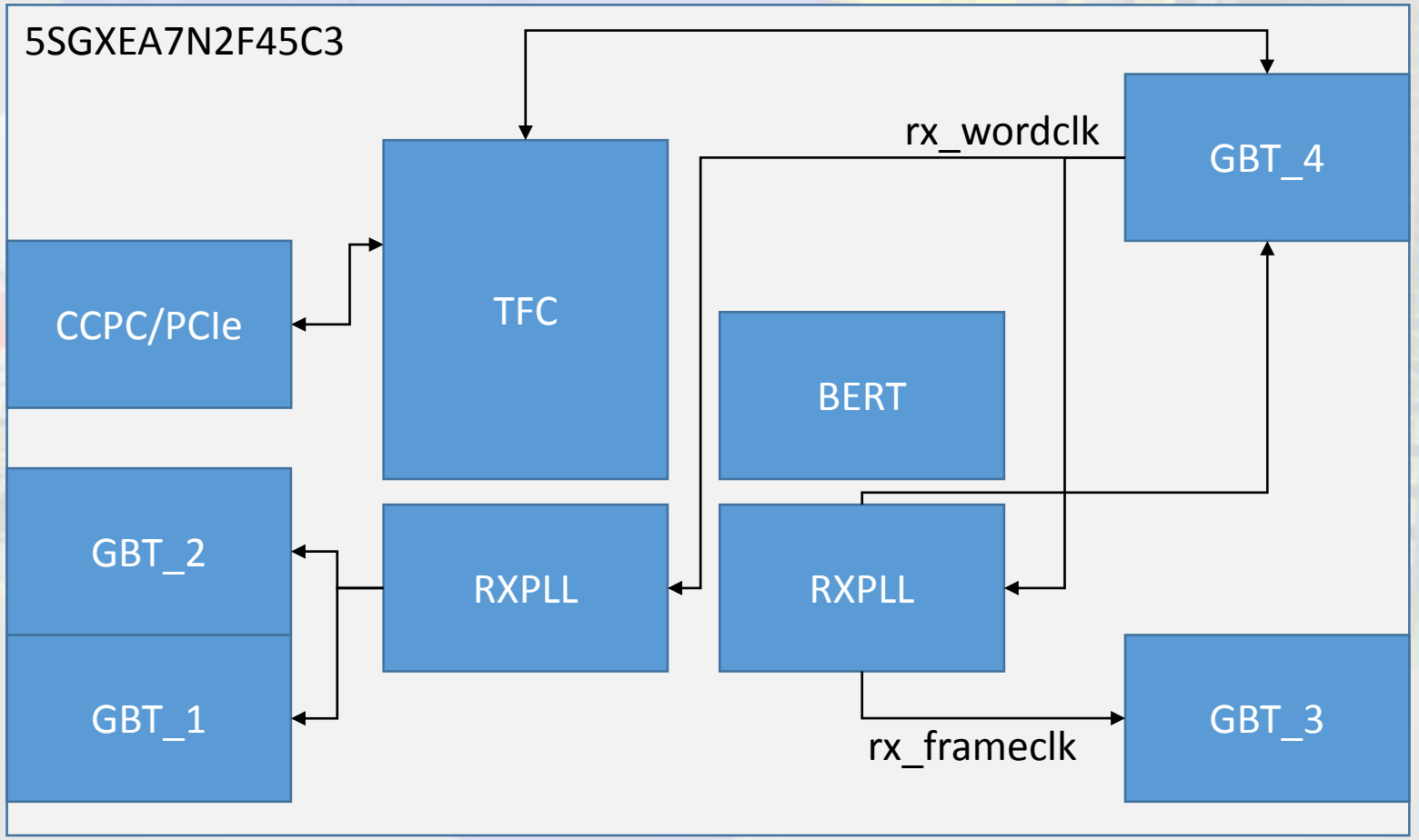


- 2 fiber trunks
  - EN-EL (“B”)
  - Transfibres (“C”)
- 1 SciFi board
  - Thanks to NIKHEF
- 4 VTTXs
  - Thanks to EP-ESE
- 1 AMC40
  - Thanks to CPPM
- PVSS panels
  - Thanks to Wilco & Federico
- Dedicated firmware
- Windows VM, clock, power…

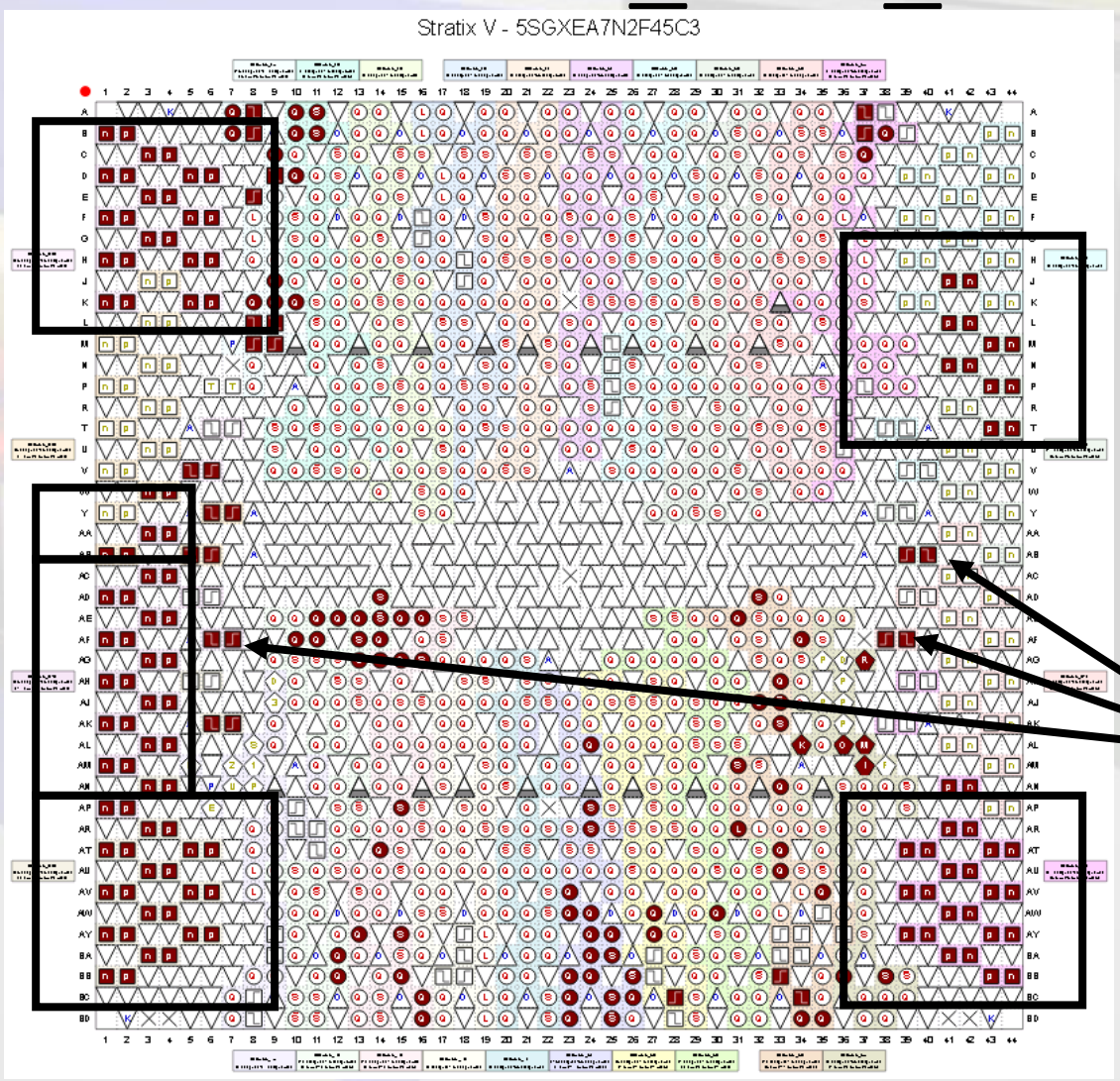
Control system



Firmware diagram: amc40_bert_versatile



Firmware pinout: amc40_bert_versatile



LEFT MPO: N/A

CCPC PCIe

LEFT MPO:
GBT_2, GBT_1 (WBUSx6)

MIDDLE MPO: N/A

RIGHT MPO: GBT_4 (TFC)

GBT_REFCLK (120MHz)

MIDDLE MPO:
GBT_3 (WBUSx3), others N/A

Firmware config: amc40_bert_versatile

- Configure number and type of banks ⇨
  - Using STANDARD optimization atm
- Configure distribution of links among front-panel connectors
  - Constrained by P&R errors!
- Configure allocation of RXPLLs
  - One per side (left/right)

```
constant DAQ_NUM_BANKS : natural := 3;
constant TFC_NUM_BANKS : natural := 1;

constant DAQ_NUM_LINKS : natural := DAQ_NUM_BANKS * MAX_NUM_GBT_LINK;
constant TFC_NUM_LINKS : natural := TFC_NUM_BANKS * MAX_NUM_GBT_LINK;

constant GBT_NUM_BANKS : integer := DAQ_NUM_BANKS + TFC_NUM_BANKS;
constant GBT_NUM_LINKS : natural := GBT_NUM_BANKS * MAX_NUM_GBT_LINK;
constant GBT_BANKS_USER_SETUP : gbt_bank_user_setup_R_A(1 to GBT_NUM_BANKS) := (
  1 to DAQ_NUM_BANKS => (
    NUM_LINKS        => MAX_NUM_GBT_LINK,
    TX_OPTIMIZATION  => STANDARD,
    RX_OPTIMIZATION  => STANDARD,
    TX_ENCODING      => WIDE_BUS,
    RX_ENCODING      => WIDE_BUS),
  DAQ_NUM_BANKS + 1 to DAQ_NUM_BANKS + TFC_NUM_BANKS => (
    NUM_LINKS        => MAX_NUM_GBT_LINK,
    TX_OPTIMIZATION  => STANDARD,
    RX_OPTIMIZATION  => STANDARD,
    TX_ENCODING      => GBT_FRAME,
    RX_ENCODING      => GBT_FRAME)
);
```

Firmware report: amc40_bert_versatile

- Resource utilization:
  - 58% ALMs
  - 5% Memory
    - BERT code from ESE modified not to instantiate RAM
  - HSSI PMA TX Serializers: 13
  - HSSI PMA RX Deserializers: 13
  - PLLs: 28
- Compilation time:

  ~35m

- Resource breakdown:
  - SOL40: 47%
  - BERT: 33%
  - GBT: 8%
  - SODIN: 4%
  - QSYS: 2%
  - Signaltap: ~6%

Issue: number of banks

- Even after refactoring PLLs, we cannot instantiate more than 4 banks:
- Error (175001): The Fitter cannot place 1 LC_PLL_CHANNEL_CLUSTER, which is within Stratix V Transceiver PLL alt_sv_gx_txpll.
- Error (175020): The Fitter cannot place logic Receiver channel that is part of Stratix V Transceiver Native PHY alt_sv_gx_std_x3 in region (210, 58) to (210, 60), to which it is constrained, because there are no valid locations in the region for logic of this type.
- Error (175007): Could not find uncongested path between source HSSI reference clock input and the LC_PLL_CHANNEL_CLUSTER
- Proposed approach(by Manoel): make gbt bank size = xvcr bank size on fpga (6 channels)

Issue: clock routing to top-left IO banks

- Error (14566): The Fitter cannot place 2 periphery component(s) due to conflicts with existing constraints (2 HSSI PMA Aux. block(s)). Fix the errors described in the submessages, and then rerun the Fitter. The Altera Knowledge Database may also contain articles with information on how to resolve this periphery placement failure. Review the errors and then visit the Knowledge Database at https://www.altera.com/support/support-resources/knowledge-base/search.html and search for this specific error message number.
- Error (175020): The Fitter cannot place logic HSSI PMA Aux. block that is part of Avalon-MM Stratix V Hard IP for PCI Express altpcie_sv_hip_avmm_hwtcl in region (210, 105) to (210, 105), to which it is constrained, because there are no valid locations in the region for logic of this type.
- Info (14596): Information about the failing component(s):
- **Info (175028): The HSSI PMA Aux. block name(s): sys_amc40:system_0|sys_amc40_ecs_0:ecs_0|altpcie_sv_hip_avmm_hwtcl:pcie_0**|altpcie_sv_hip_ast_hwtcl:altera_s5_a2p|altpcie_hip_256_pipen1b:altpcie_hip_256_pipen1b|sv_xcvr_pipe_native:g_xcvr.sv_xcvr_pipe_native|sv_xcvr_native:inst_sv_xcvr_native|sv_pma:inst_sv_pma|sv_tx_pma:tx_pma.sv_tx_pma_inst|sv_tx_pma_ch:tx_pma_insts[0].sv_tx_pma_ch_inst|tx_pma_ch.tx_pma_buf.tx_pma_aux
- Info (175013): The HSSI PMA Aux. block is constrained to the region (210, 105) to (210, 105) due to related logic
- Info (175015): The I/O pad o_serial_data_PCIe is constrained to the location PIN_W4 due to: User Location Constraints (PIN_W4)
- Info (14709): The constrained I/O pad is driven by this HSSI PMA Aux. block
- Error (11238): The following 1 HSSI PMA Aux. block locations are already occupied, and the Fitter cannot merge the previously placed nodes with these instances. The nodes may have incompatible inputs or parameters.
- Error (17932): Location HSSIPMAAUX_X210_Y105_N93 is already occupied by 6 HSSI PMA Aux. blocks
- **Info (11237): Already placed at this location: gbt_fpga_top:gbt_fpga|gbt_fpga_3_1_1_sv**:\gen_gbt_fpga:4:gbt_fpga|gbt_bank:bank|multi_gigabit_transceivers:mgt|mgt_std:\mgtStd_gen:mgtStd|alt_sv_gx_std_x3:\gxStd_x3_gen:gxStd_x3|altera_xcvr_native_sv:alt_sv_gx_std_x3_inst|sv_xcvr_native:gen_native_inst.xcvr_native_insts[0].gen_bonded_group_native.xcvr_native_inst|sv_pma:inst_sv_pma|sv_tx_pma:tx_pma.sv_tx_pma_inst|sv_tx_pma_ch:tx_pma_insts[0].sv_tx_pma_ch_inst|tx_pma_ch.tx_pma_buf.tx_pma_aux

Issue: new year's glitch

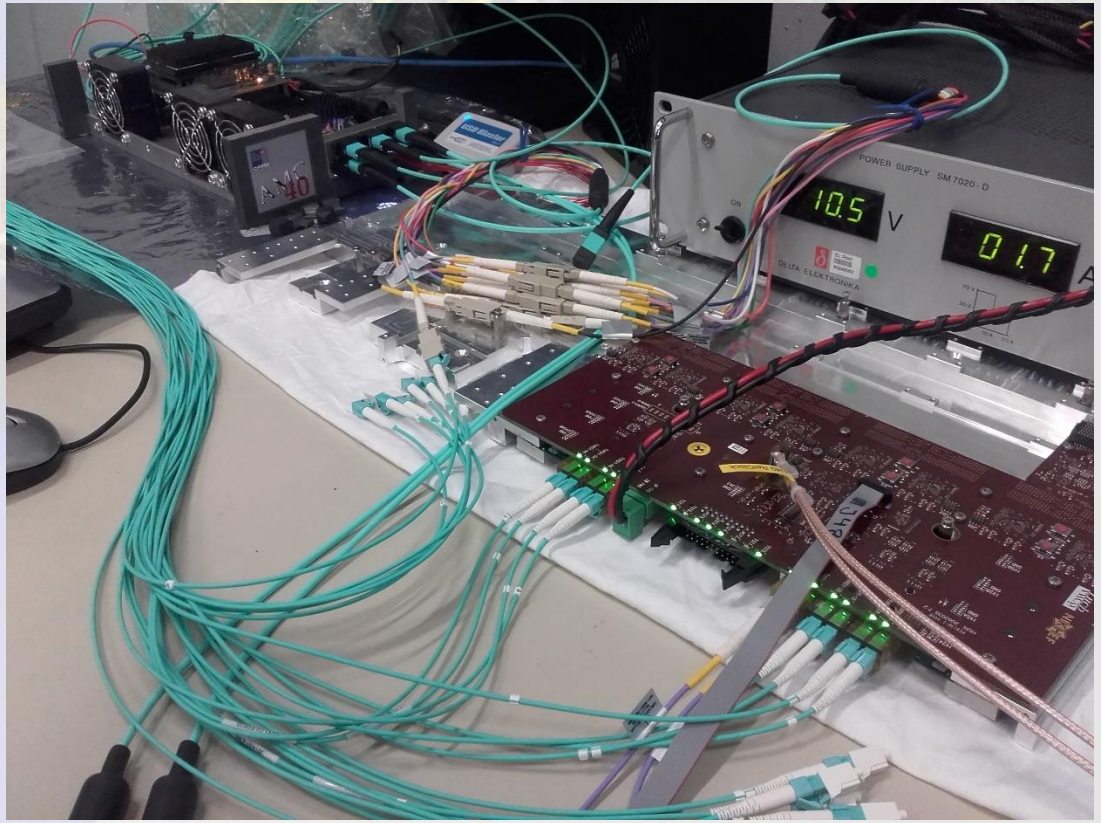
- Tests at the pit started on Dec 18th and ran continuously through until the end of the year with no errors
- 2 channels (original VTTx)
- On Jan 1st or 2nd there were some power cuts and the program making backups of the test log file crashed
- Access to log file restored on Jan 4th, showing one error had occurred on one of the two fibers sometime after Jan 1st
- However this was before cleaning the connectors, and the second fiber remained at zero errors during the entire period
- Tested $1.5*10^{16}$ bits over that period (until new power cut on Jan 7th)

Issue: loss of lock with SciFi board

- SYMPTOM:
  - Master RXRDY led: OFF
  - Master TXRDY & DV leds: ON but no data
  - All slave VTTXs: OFF
- CAUSE:
  - Not understood, timing is random and uncorrelated with other activities in the building (e.g.: 02/07 (Sunday) – 13h31, 02/08 – 23h03, etc…)
- EFFECT:
  - Frequent trips to the pit to physically reset the board ☹ (once every 24/48 hours)
- NOTES:
  - When using just 2 channels over xmas, board was running for weeks without issues

Test setup interconnect matrix

MPO	Trunk	Bank	BERT	Fiber	VTTx	I2C
Middle	B	gbt_1	bert_3	9	2A	I2C-2
Left	C		bert_2	1	4A	I2C-6
Left	C		bert_1	2	3A	I2C-4
Left	C	gbt_2	bert_6	11	2B	I2C-3
Left	C		bert_5	9	3B	I2C-5
Left	C		bert_4	7	4B	I2C-7
Middle	B	gbt_3	bert_9	7	1A	I2C-0
Left	C		bert_8	12	MPOD	N/A
Middle	B		bert_7	12	1B	I2C-1
Right	N/A	gbt_4	N/A	10	TFC	N/A



BERT results (after new VTTXs & cleaning)

- SciFi board populated with 4 VTTXs (8 channels)
- Additional loopbacks installed in PZ85
- Cleaning of all connectors
- Manual intervention on board every time link lock is lost

- Number of bits tested (as of Wednesday night 10pm)
  - **1.09283E+16** without errors

Conclusions

- A lot of work was required to create a firmware for this test
- Firmware is still fully compatible with the PVSS control system
- A lot of work was required to find an I/O configuration that would make the fitter happy
- This is the first time the AMC40 is actively using so many GBT links over long periods
- 8+1 DAQ links sufficient for current setup but more needed if we get to populate an entire SciFi readout box
- Need to solve SciFi link stability issue to improve test deadtime