Upgrade of the Read-out and Trigger System

A. Kluge, March 1, 2016

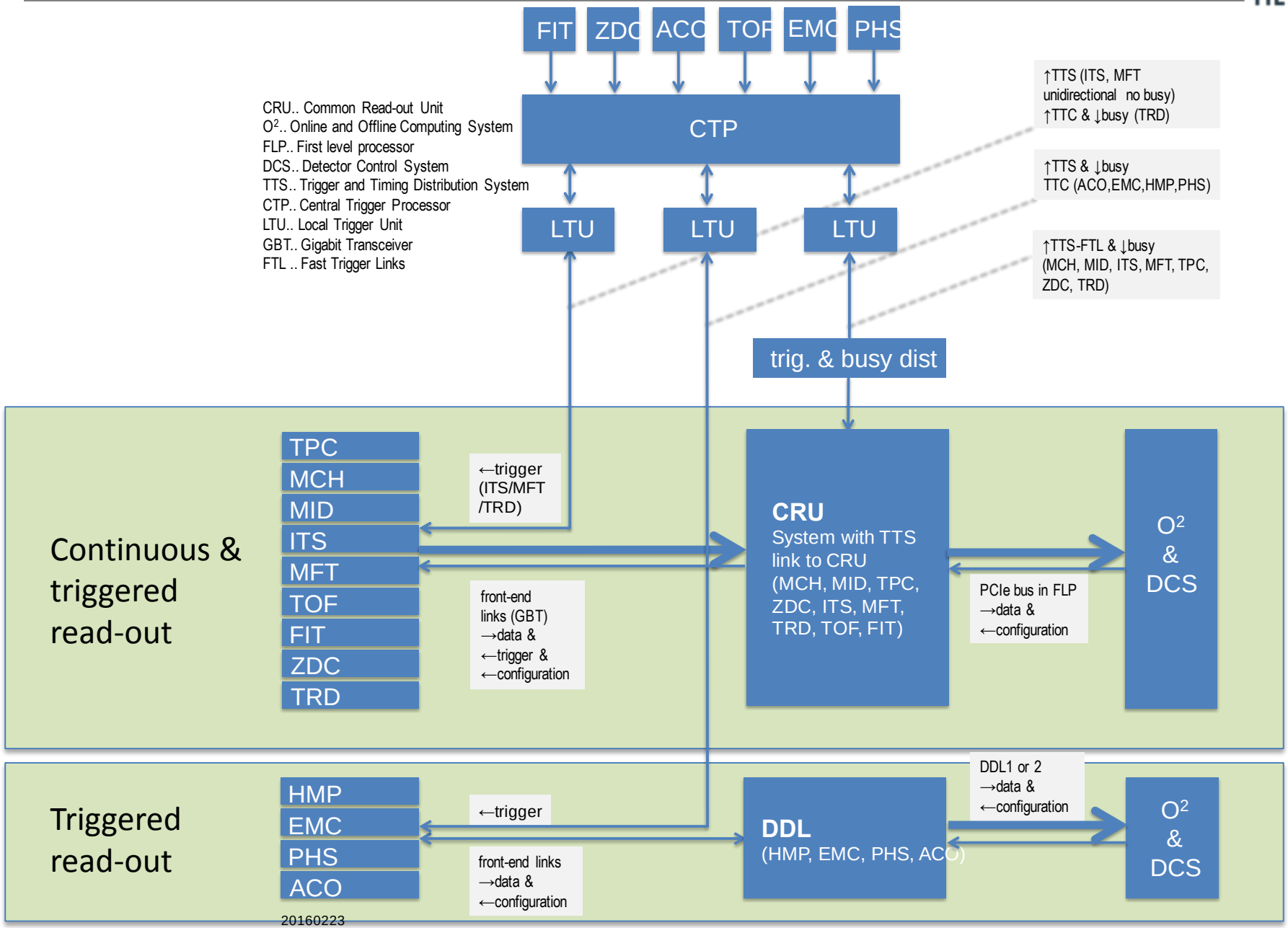
Outline

- Upgrade architecture & TPC overview
- CRU - Common read-out Unit
- CTP – Central Trigger Processor
- SAMPA -TPC/MCH read-out ASIC
- FIT - Fast interaction trigger
- TOF - Time of flight detector
- MCH - Muon Chamber
- MID - Muon Identifier

Reviews

- **Review page:**
  - https://twiki.cern.ch/twiki/bin/viewauth/ALICE/Reviews
- **CTP DR: 2016 01**
- **ITS pixel chip EDR: 2015 10**
- **MID FE EDR: 2015 03**
- **MID RO EDR: 2015 06**
- **SAMPA MPW2 DR: 2015 01 – 2016 01**
- **TPC architecture review: 2015**

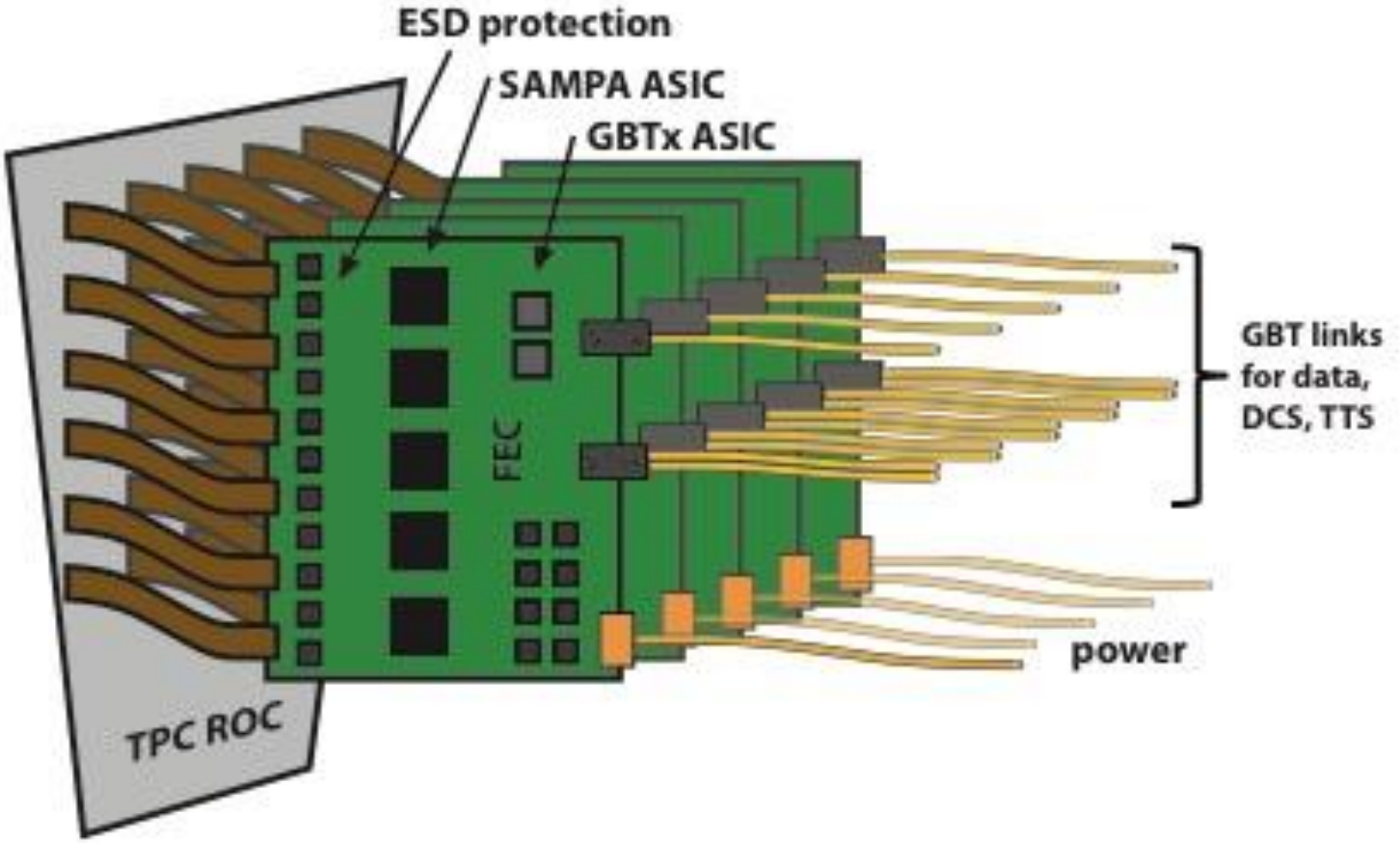
Upgrade architecture overview



TPC architecture

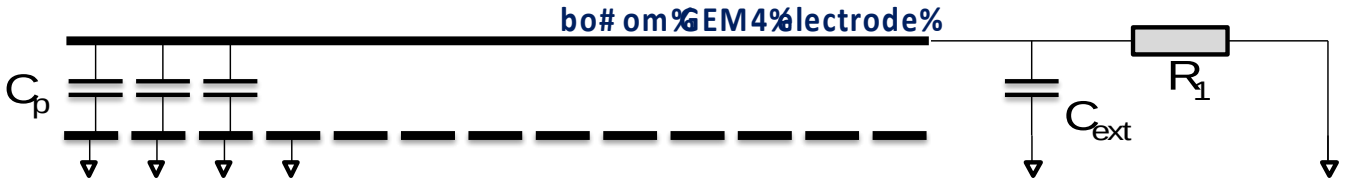
TPC-UCG architecture

- ALICE: continuous read-out with online data compression
  - 2 GBT → 6.4-9 Gb/s
  - 5 Sampa raw data → 16 Gb/s + formatting
- Data reduction via: Zero suppression or Hufmann encoding

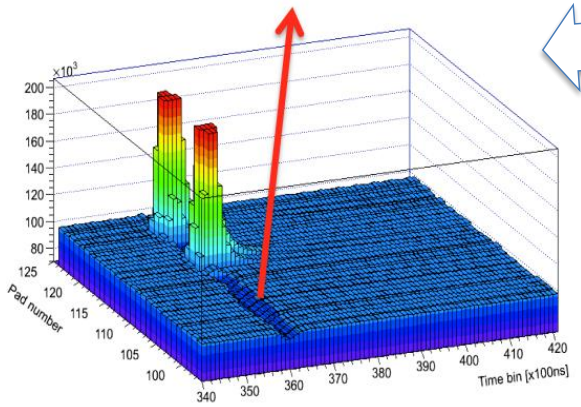


TPC: common mode effect

- Common mode effect: Baseline shift and "noise" due to capacitive coupling of electrodes in readout structure

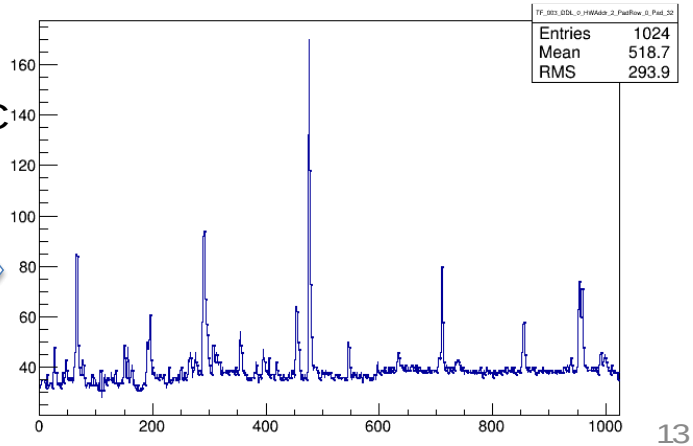


Common mode signal



Measurement in current TPC

Simulation of the effect at large occupancies



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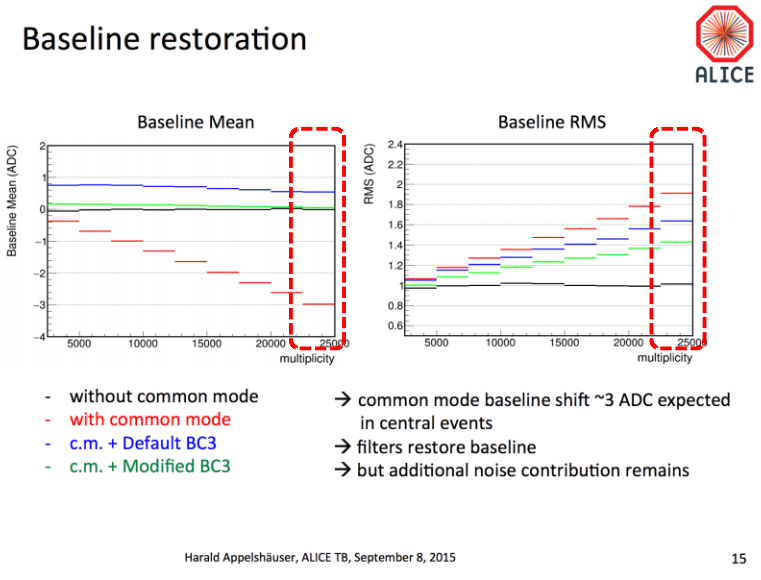
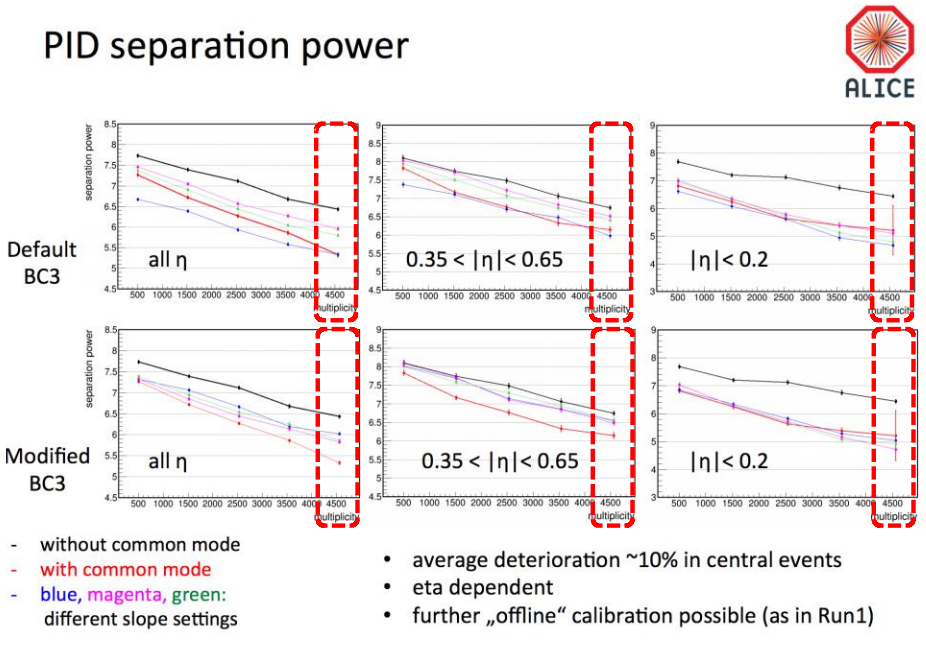
- SAMPA ASIC zero suppression and base line filters
- SAMPA Huffman compression & CRU base line filters

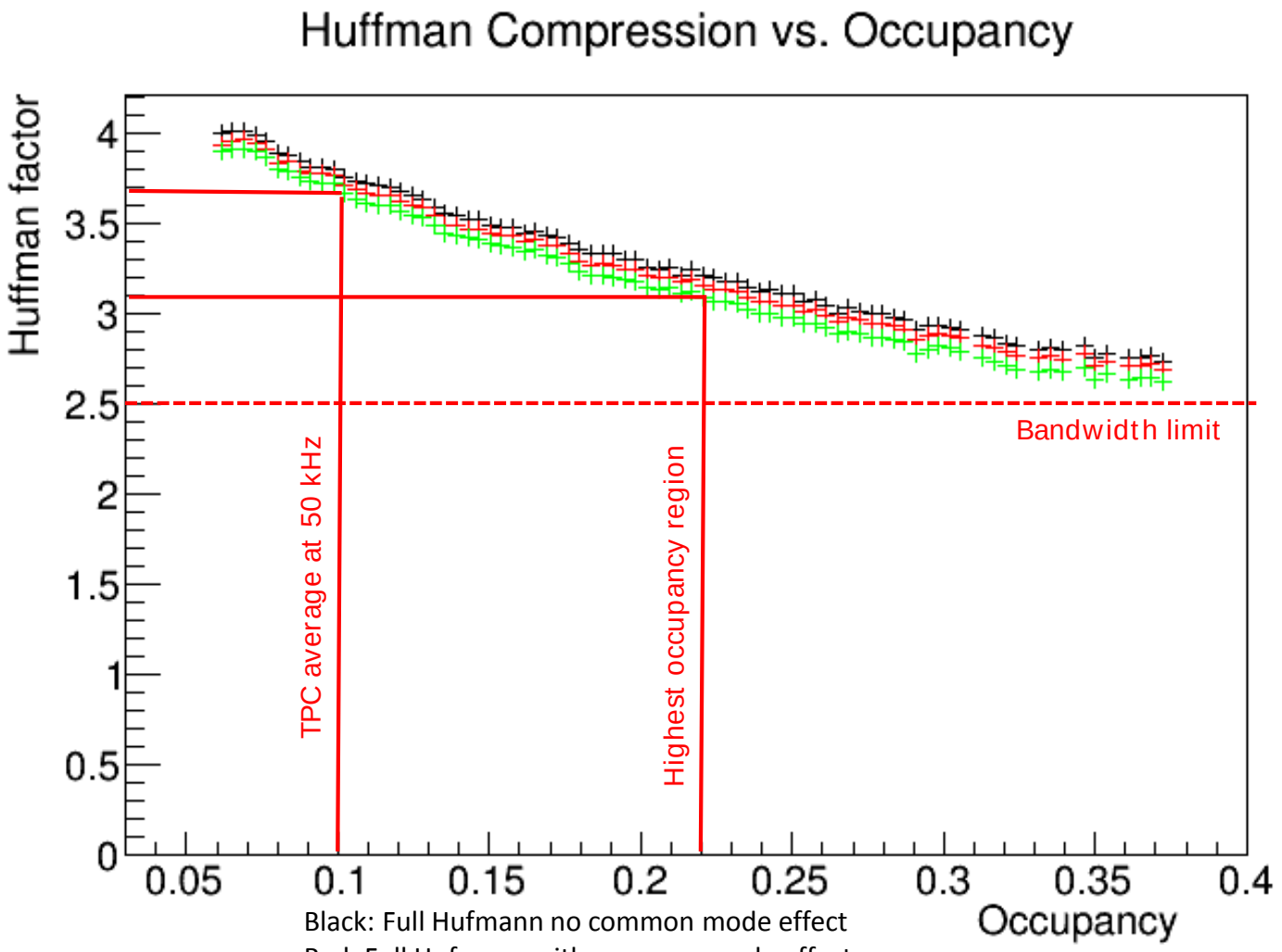
BC3 performance





- Filter (BC3) performance studies:
  - Base line mean: 3 ADC → 0.2 ADC
  - Base line RMS: 1.9 ADC → 1.4 ADC
  - PID: Filter can limit deterioration to ~10 % (depending on eta)

Hufmann performance



Black: Full Hufmann no common mode effect
Red: Full Hufmann with common mode effect
Green: Truncated Hufmann with common mode effect

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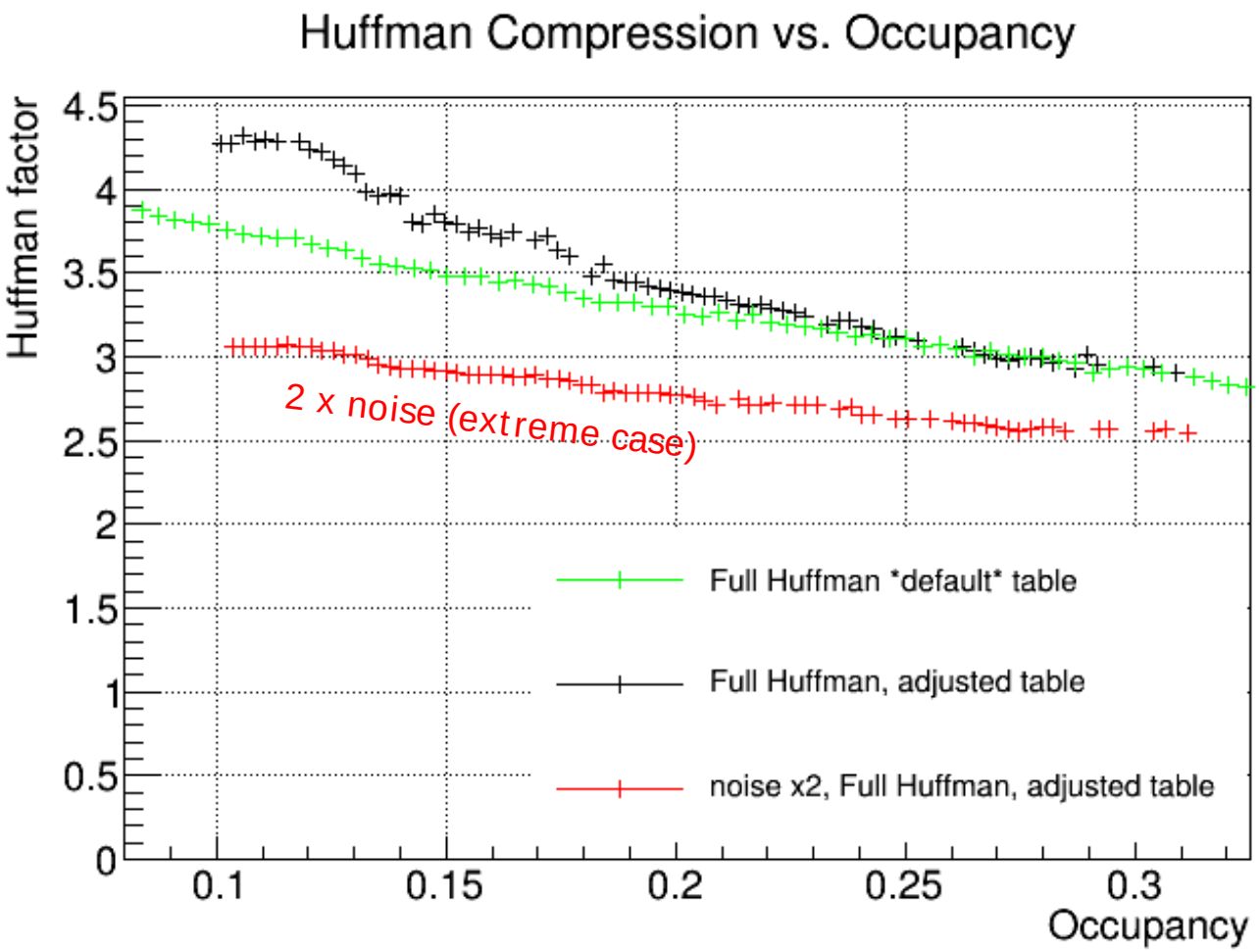
M. Richter

Hufmann performance



M. Richter

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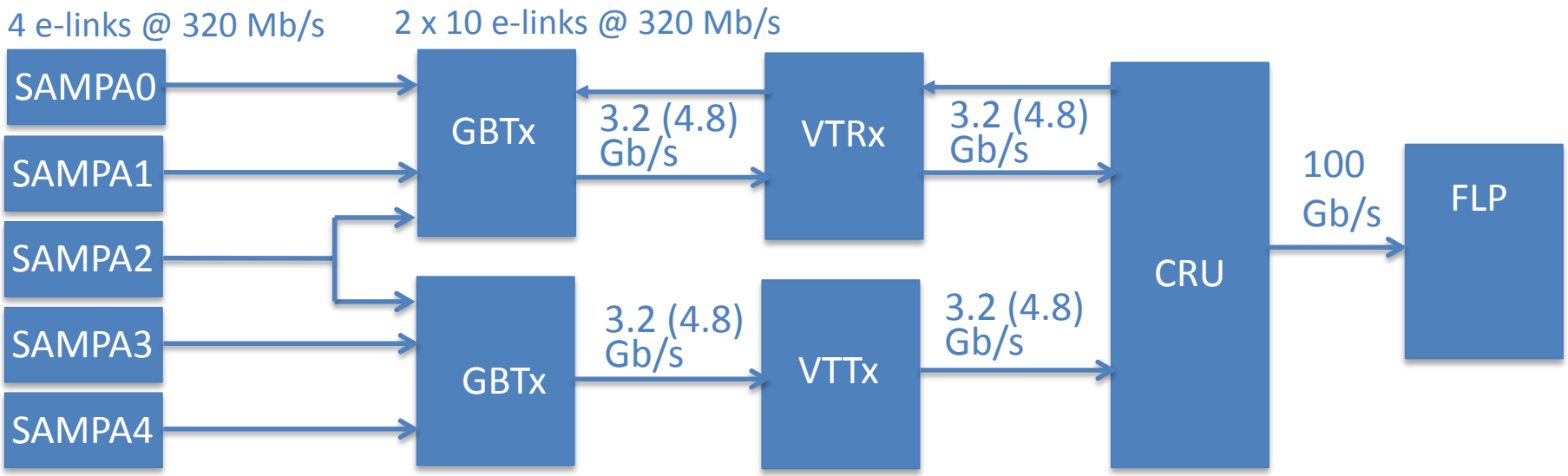
Architecture review conclusion

- Zero suppression/base line correction/compression
  - seems possible online/on-detector (SAMPA) in nominal conditions with acceptable performance loss
- However,
  - remaining common mode noise, insufficient robustness against non ideal baseline stability, insufficient flexibility to adapt to unforeseen operating conditions
- As a result, the architecture was adapted
  - to minimize performance loss risk AND reduce man power need

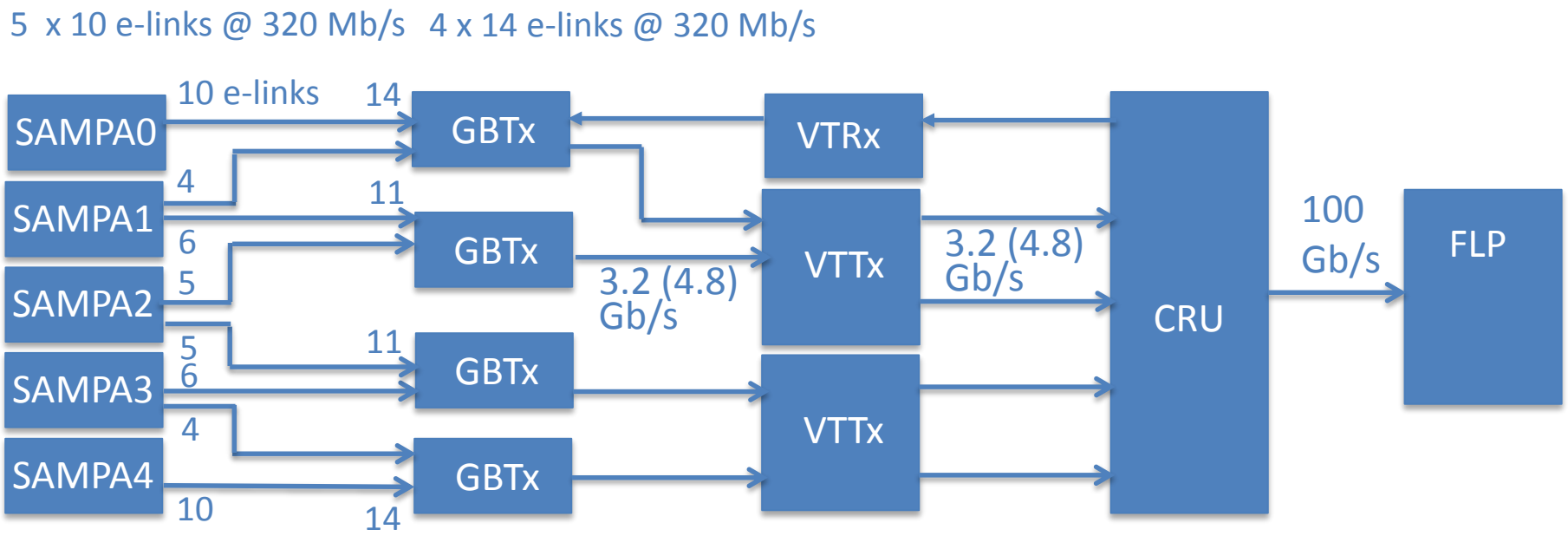
TPC Read-out architecture optimisation

TDR scheme

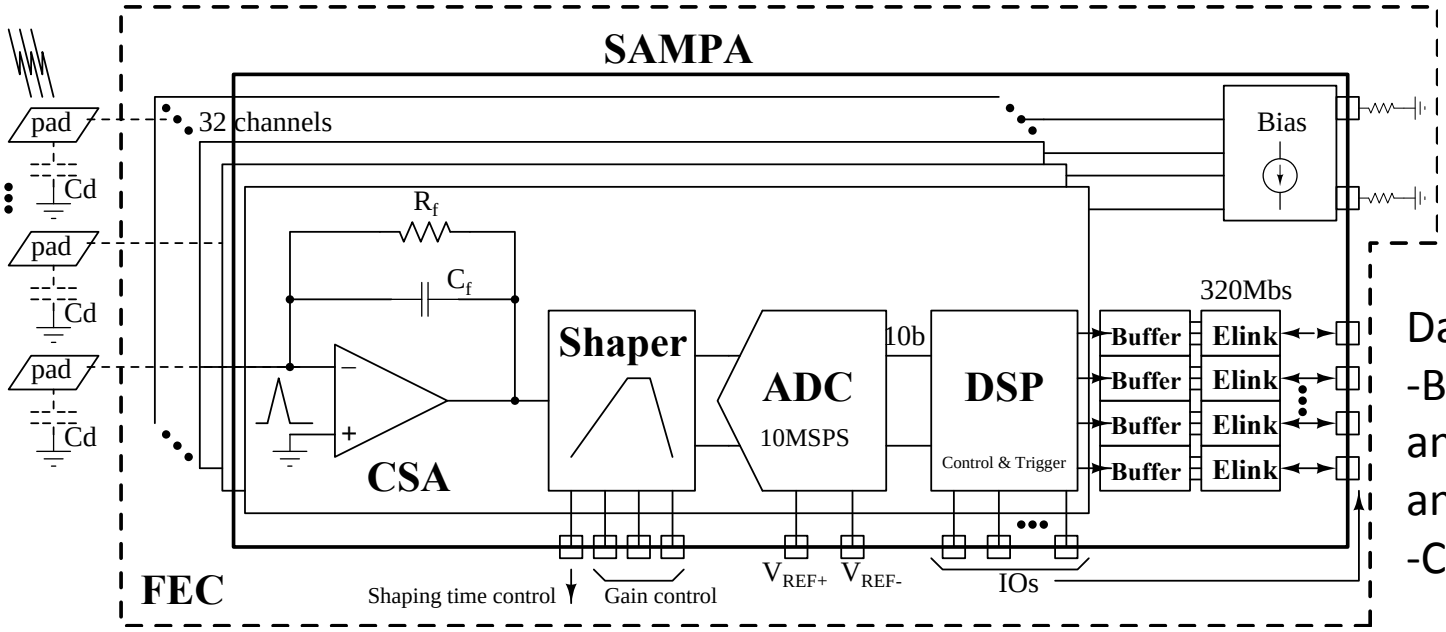

4 e-links @ 320 Mb/s
2 x 10 e-links @ 320 Mb/s
SAMPA0
SAMPA1
SAMPA2
SAMPA3
SAMPA4
GBTx
GBTx
3.2 (4.8) Gb/s
3.2 (4.8) Gb/s
VTRx
VTTx
3.2 (4.8) Gb/s
3.2 (4.8) Gb/s
CRU
100 Gb/s
FLP

Full read-out with 4 GBTs

- **SAMPA direct read out mode – 2 x 5 bit words**
  - GBT wide bus mode 4.48 Gb/s

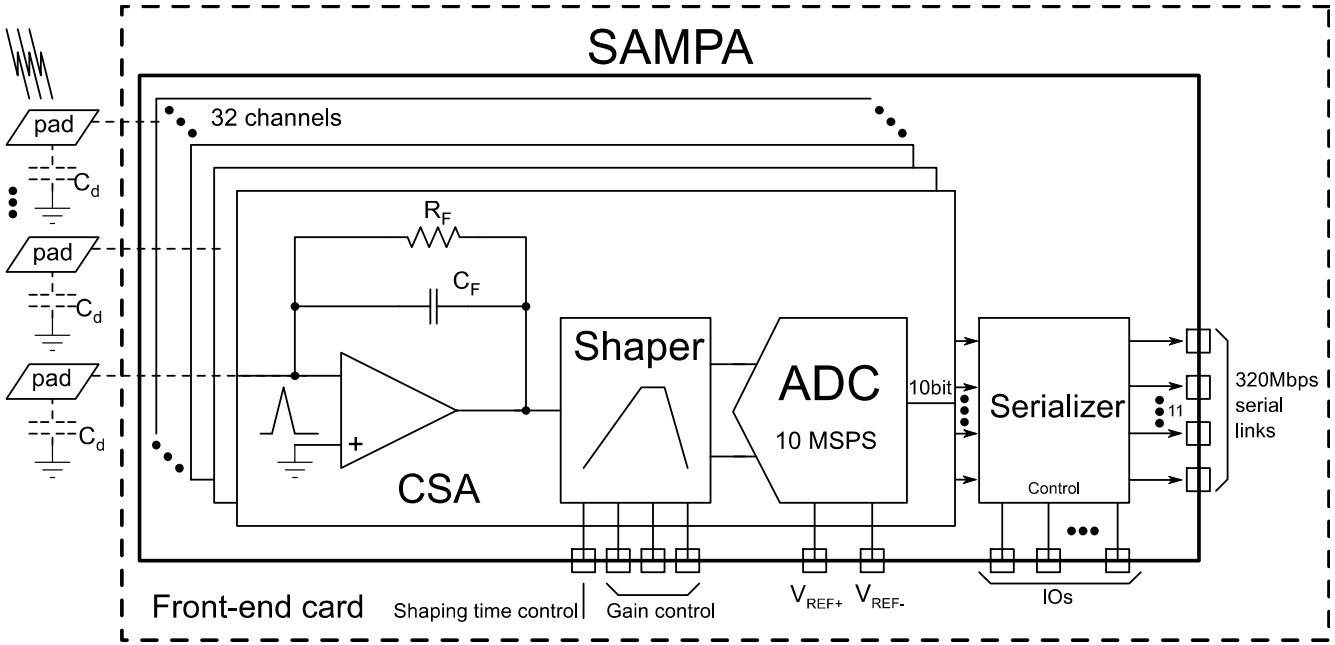


SAMPA: read-out mode 1



Data processed by DSP
-Baseline correction and ZeroSuppression and/or
-Compression

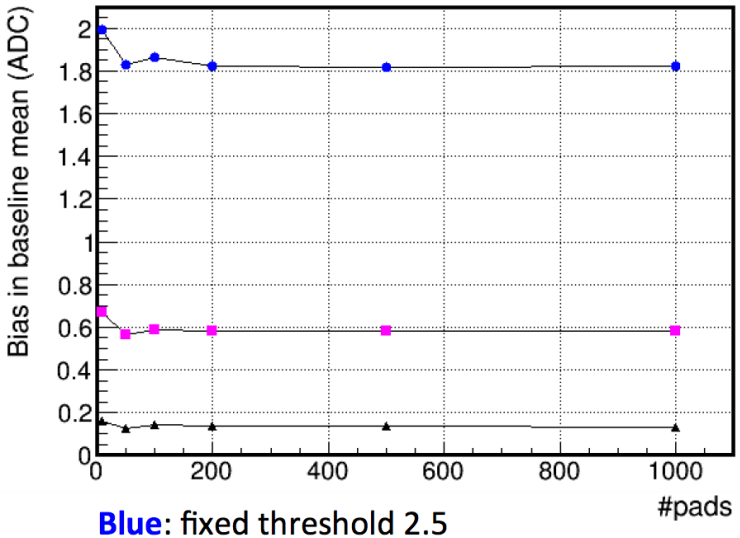
SAMPA: read-out mode 2

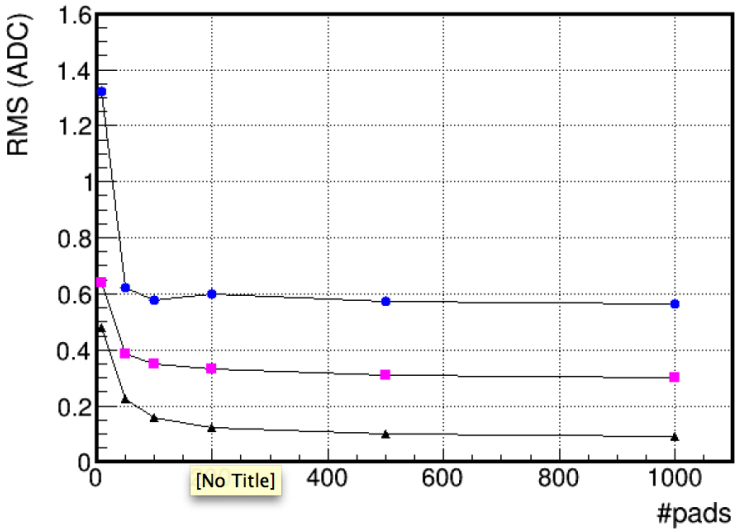


Direct serialization:
all data via 10 e-links
(DSP bypassed)

Base line correction in CRU

Baseline treatment in CRU (4)

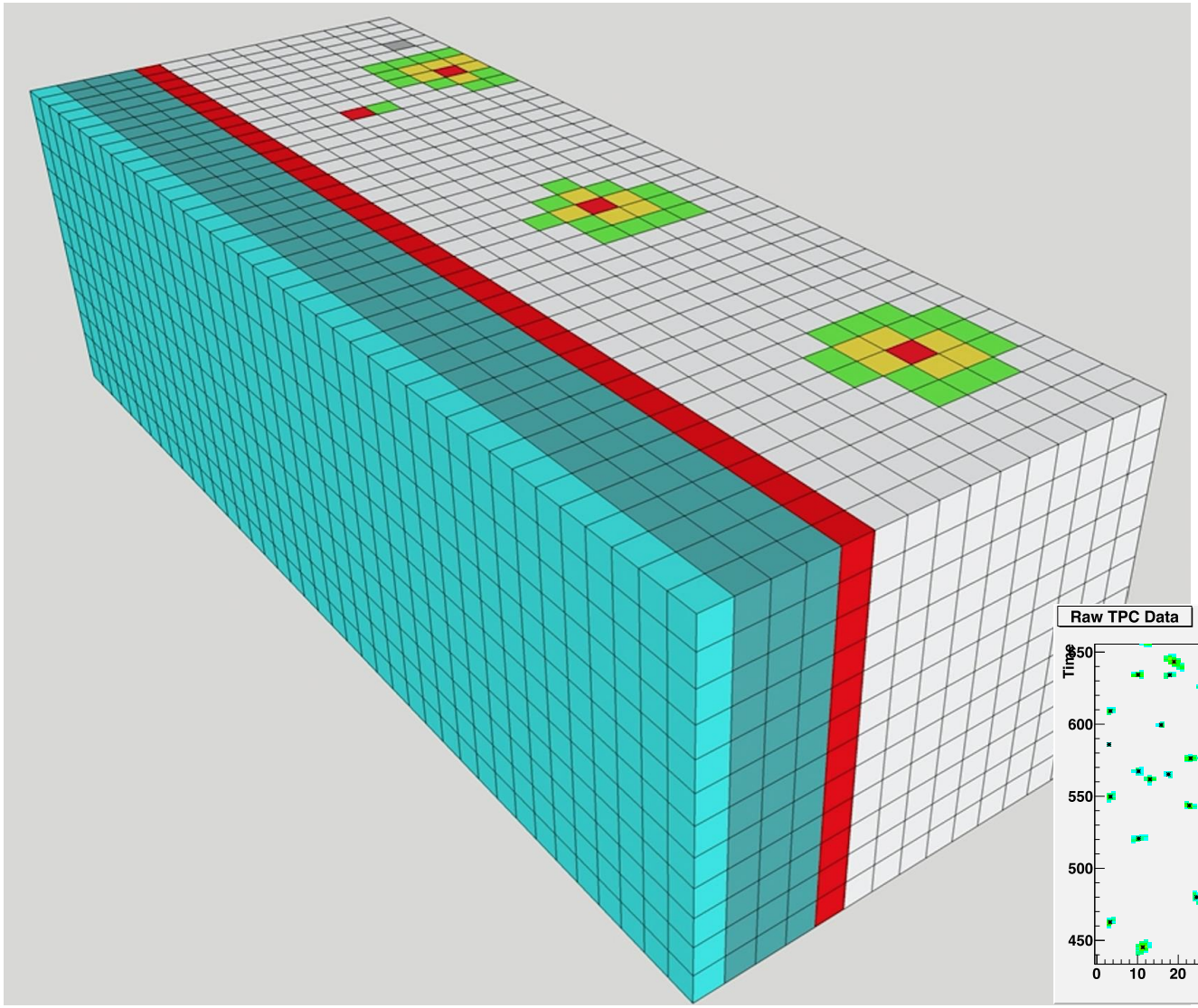




Blue: fixed threshold 2.5
Magenta: last value kept inside detected signal
Black: detected signal region excluded from mean calculation

- average over 100 signal pads with signal exclusion gives almost perfect baseline estimate with negligible residual noise.
- further improvement using median instead of mean

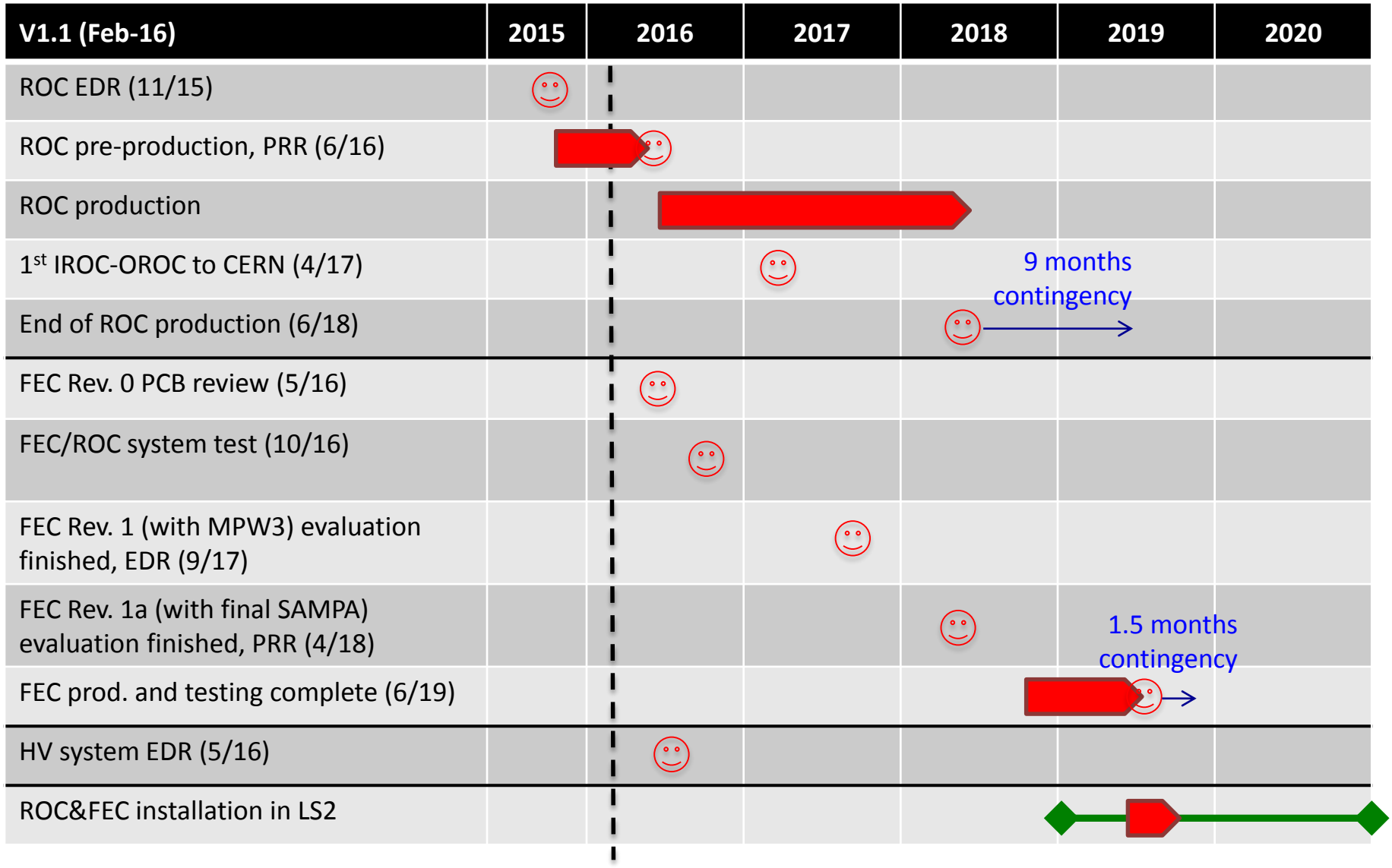
CRU processing



TPC Architecture

- **Stream out all raw ADC values to CRU**
- **Perform data processing in CRU**
  - Optimisation in FPGA
  - Allows SAMPA design to continue
- **Data arriving synchronously, simpler implementation in CRU**
- **With 10 MHz ADC sampling frequency**
  - 40 CRU input fibers
  - Additional cost
- **5 MHz sampling under investigation**
- **No additional on-detector development or qualification needed**

TPC


V1.1 (Feb-16)
2015
2016
2017
2018
2019
2020
ROC EDR (11/15)
ROC pre-production, PRR (6/16)
ROC production
1st IROC-OROC to CERN (4/17)
9 months contingency
End of ROC production (6/18)
FEC Rev. 0 PCB review (5/16)
FEC/ROC system test (10/16)
FEC Rev. 1 (with MPW3) evaluation finished, EDR (9/17)
FEC Rev. 1a (with final SAMPA) evaluation finished, PRR (4/18)
1.5 months contingency
FEC prod. and testing complete (6/19)
HV system EDR (5/16)
ROC&FEC installation in LS2

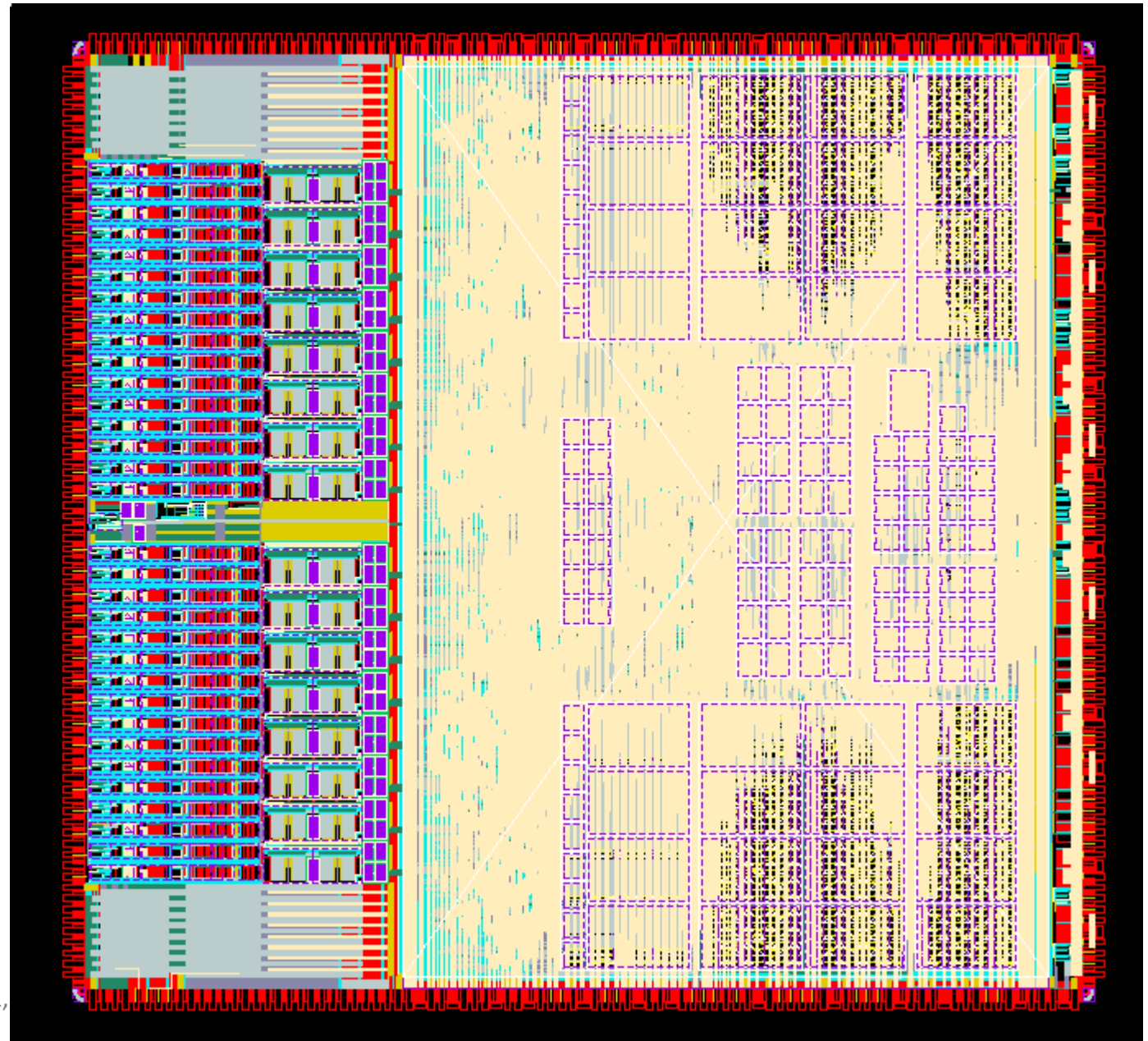
SAMPA

M. Munhoz

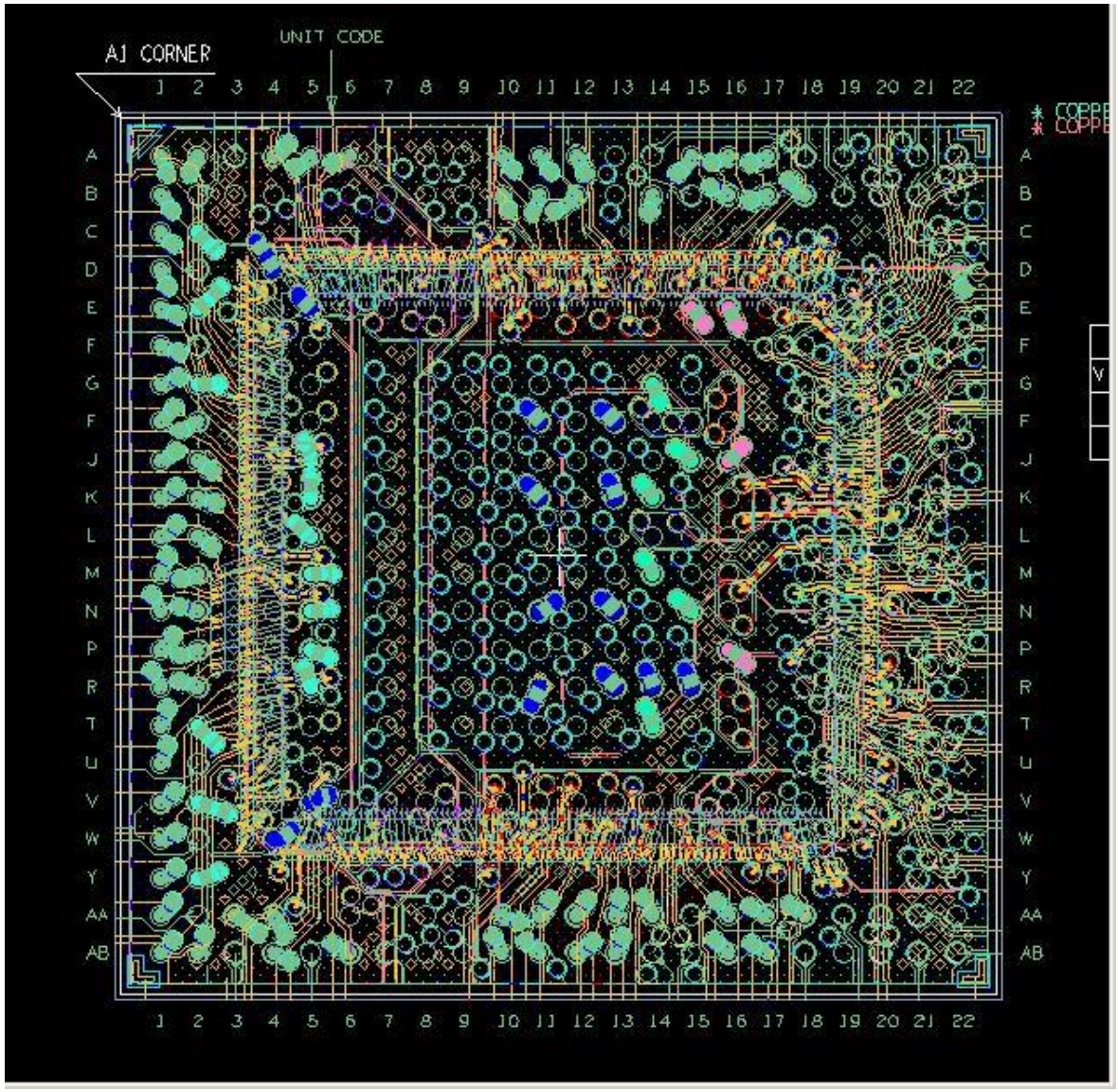
SAMPA: TPC & MCH (TSMC CMOS 130 nm)

- **MPW1:**
  - SAMPA Building blocks tested
    - by SAMPA/TPC/MCH/NICA
- **Full size MPW2 with all channels**
  (32 ch, FE+ADC+DSP+eLinks)
  - December 2015: Design review
  - January 2016: sign-off review
  - February 2016: Submitted
  - Die Size: 9.575 x 8.985 mm^2
  - Engineering run (cheaper): 10 wafers, >1500 pieces
- **Packaging: BGA (custom 15x15 mm^2, 372 balls)**
  - 1000 chip (MOC)

SAMPA

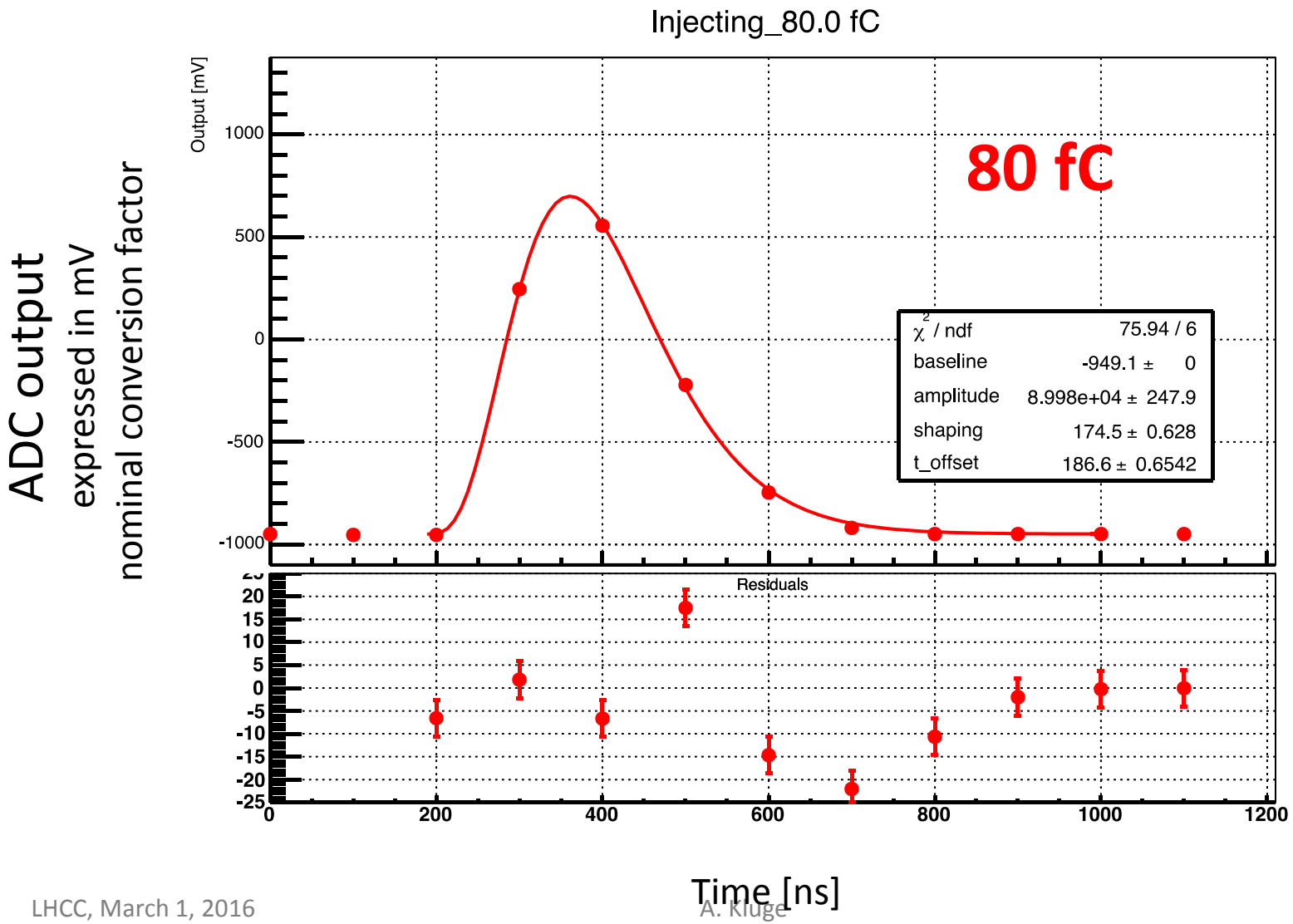


BGA substrate (by ASE)



Simulation 8 ch. FE + ADC: response 20mV/fC neg

ADC ENOB simulation: 9.6 bit



SAMPA

V1.1 (Feb-16)	2015	2016	2017	2018	2019	2020
MPW2 submitted (2/16)						
MPW3 EDR (10/16)						
MPW3 submitted (1/17), EDR						
SAMPA PRR (9/17), engineering submission						
Delivery Engineering Run (1/18)						
Mass production						
SAMPA chip tested and ready for mounting (11/18)						
LS2						

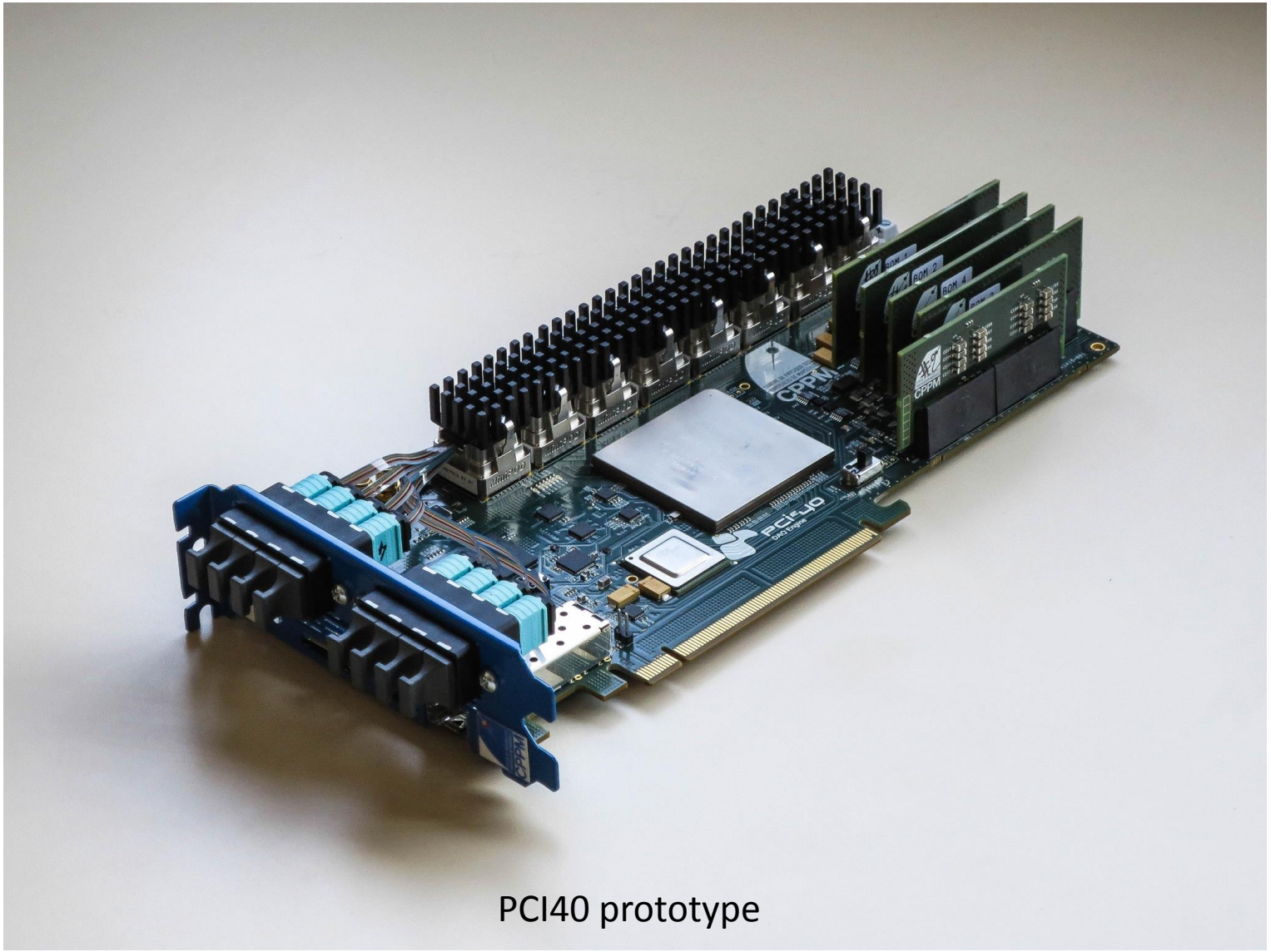
CRU – common read-out unit

PL: Tivadar Kiss

CRU

- **ALICE reviews:**
  - 13 Jan ’15
  - 4 Feb ’15
  - 18 Feb ’15
  - **Mar ’16**
- **EDR Apr ‘16**

Common read-out unit – PCI40

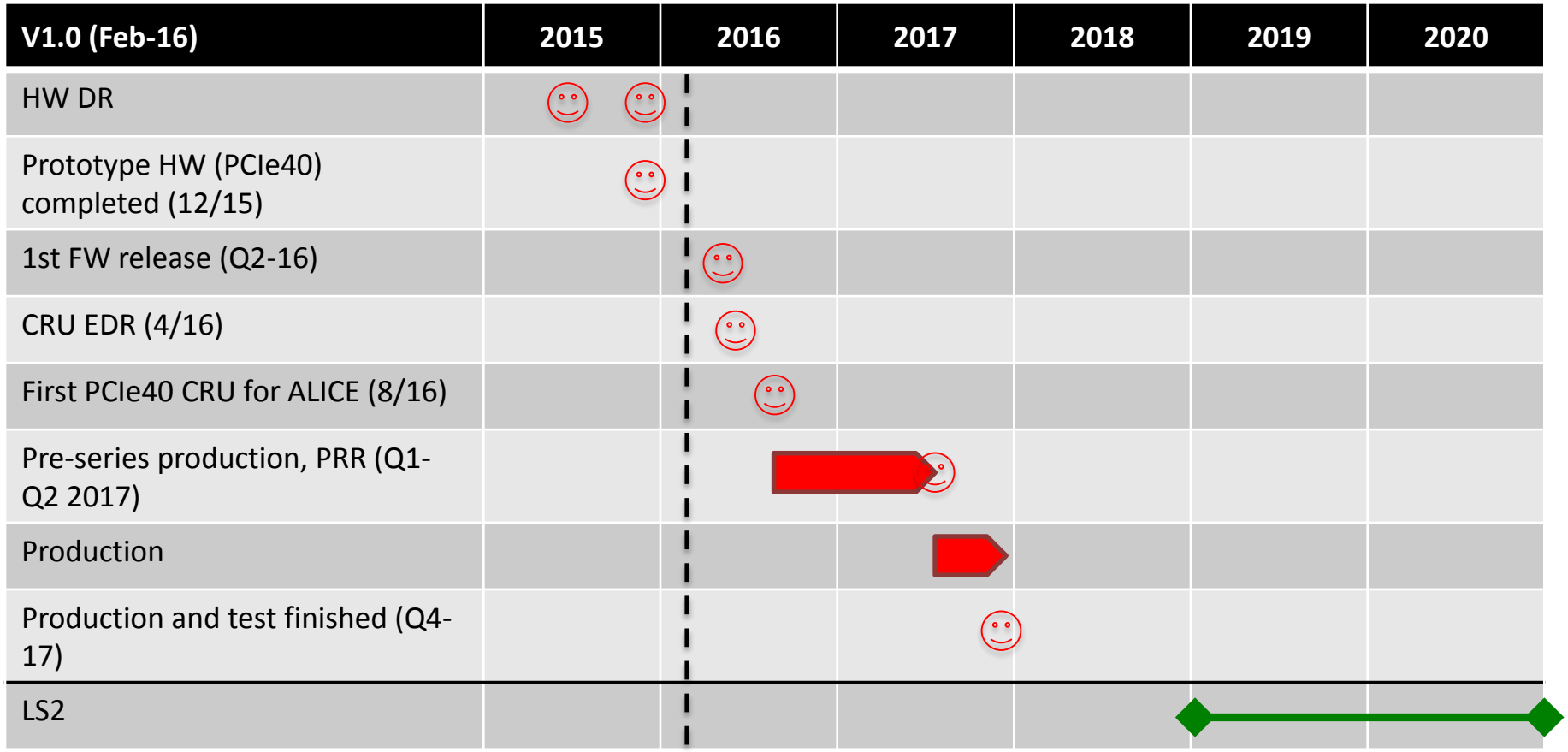


PCI40 prototype

CRU

- **PCI40 prototype exists**
  - Main functionality tested
    by LHCb and ALICE
- **Pre series production March 2016**
  - Date adapted to delivery of next FPGA release
- **ALICE Development kit available**
  - based on DDL (C-RORC)

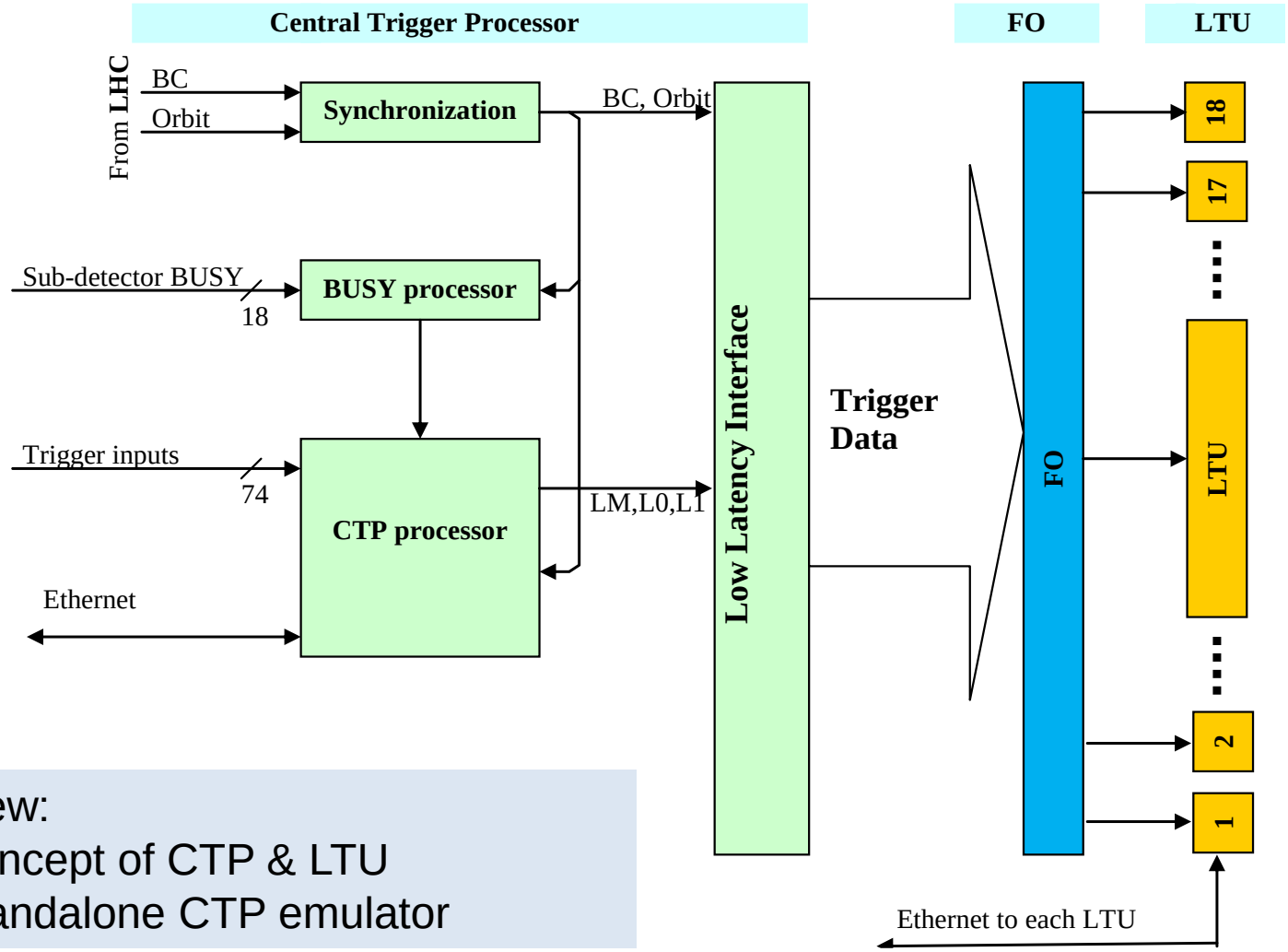
CRU


V1.0 (Feb-16)
2015
2016
2017
2018
2019
2020
HW DR
Prototype HW (PCIe40) completed (12/15)
1st FW release (Q2-16)
CRU EDR (4/16)
First PCIe40 CRU for ALICE (8/16)
Pre-series production, PRR (Q1-Q2 2017)
Production
Production and test finished (Q4-17)
LS2

CTP – Central Trigger processor

D. Evans

Trigger Block Diagram



Design review:
Keep the concept of CTP & LTU
LTU as a standalone CTP emulator

CTP board (LM board)

Scope A,B outputs

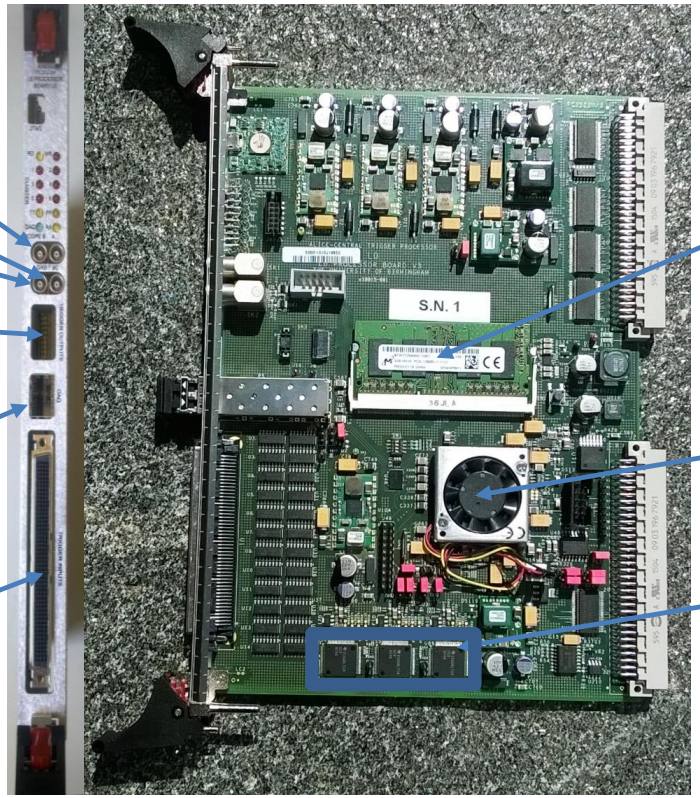
BC input (ECL)

ORBIT input (ECL)

SAMTEC FireFly cable
- 12 diff. link
- Connection to LTUs via Fan-out board

SFP+
- IP bus (optical or electrical Ethernet link)

96 LVDS I/O
- Trigger inputs
- BUSY inputs
- LM output

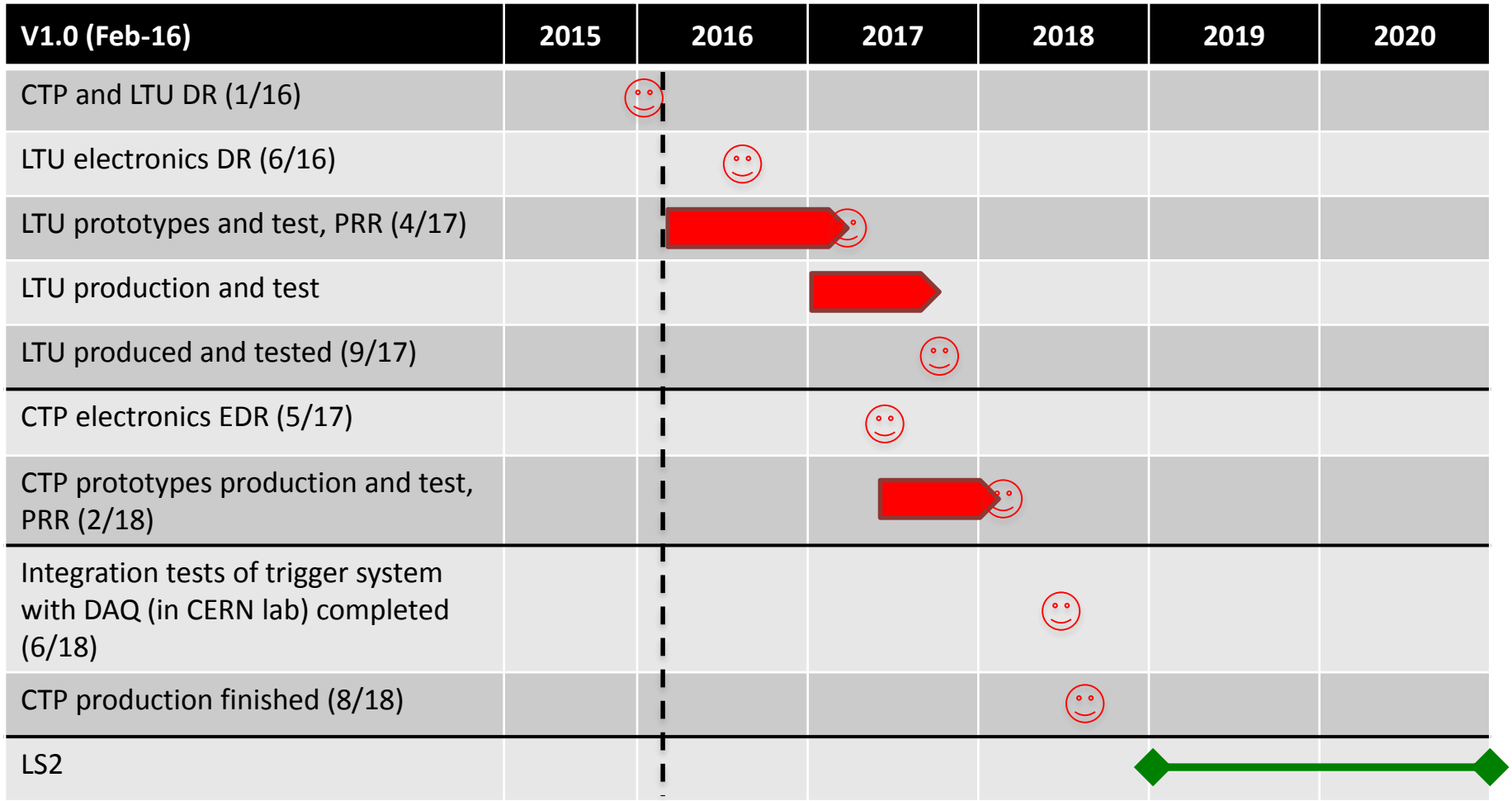


2 GB DDR3 SODIMM memory

XILINX Kintex-7 FPGA XC7K325T-2FFG900C

Power controllers

CTP

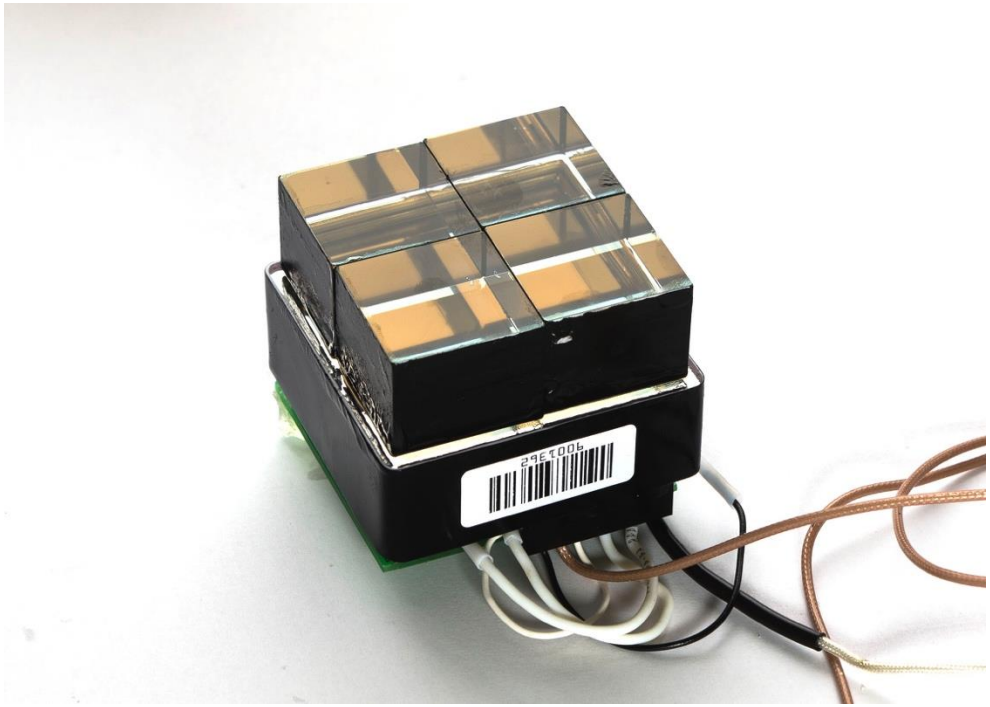

V1.0 (Feb-16)
2015
2016
2017
2018
2019
2020
CTP and LTU DR (1/16)
LTU electronics DR (6/16)
LTU prototypes and test, PRR (4/17)
LTU production and test
LTU produced and tested (9/17)
CTP electronics EDR (5/17)
CTP prototypes production and test, PRR (2/18)
Integration tests of trigger system with DAQ (in CERN lab) completed (6/18)
CTP production finished (8/18)
LS2

FIT – Fast interaction trigger

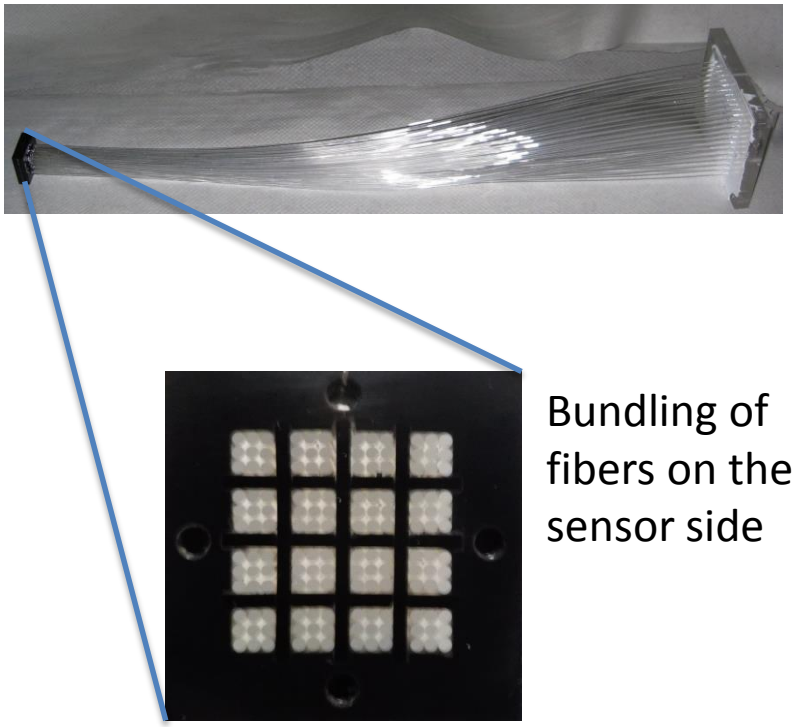
W. Trzaska

FIT-T0/V0

- T0



V0

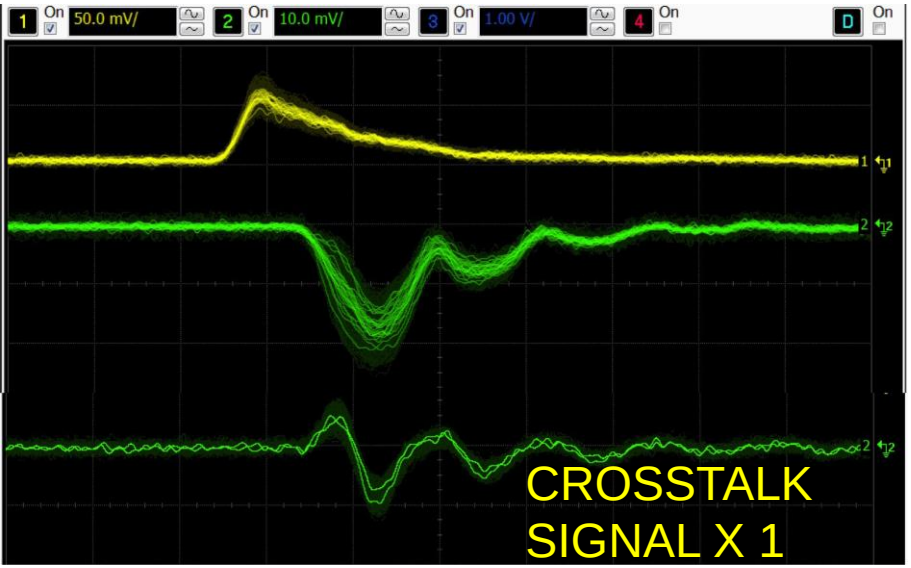


Bundling of fibers on the sensor side

Laser tests of the modified PLANACON

Three quadrants are open to laser pulses. One quadrant is covered.

Standard XP85012 Modified

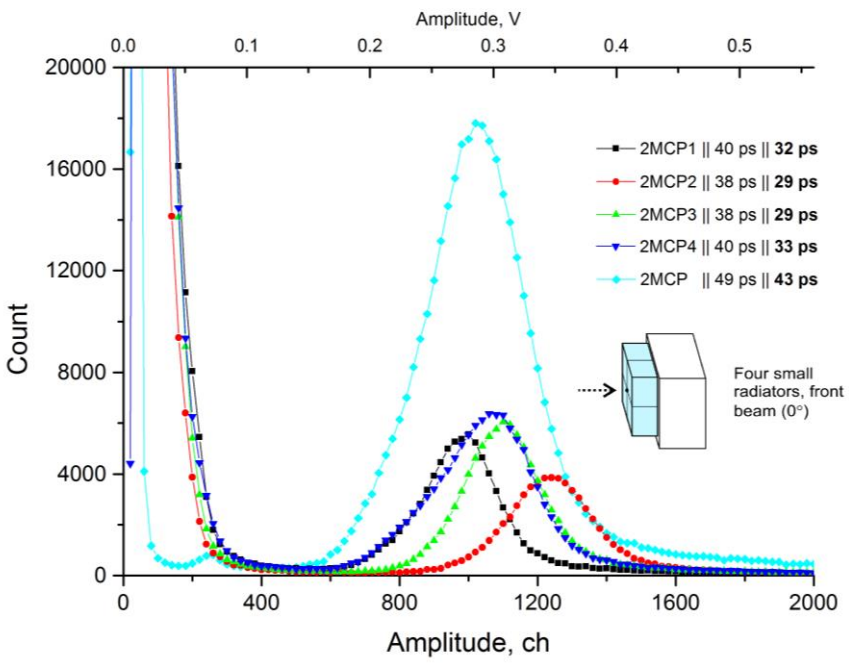


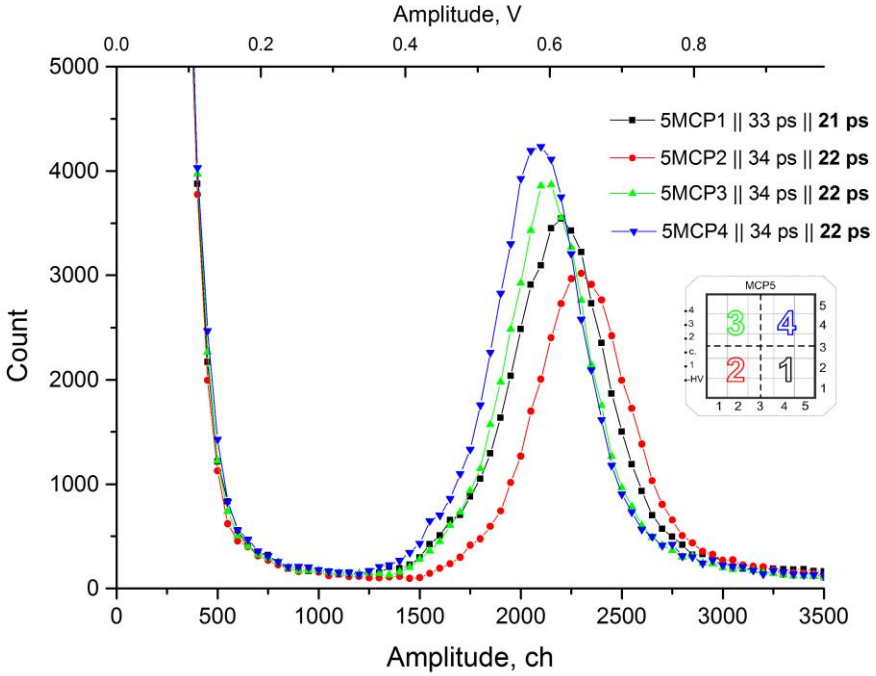
The leading edge is unstable, depends on charge distribution between individual anodes of the three illuminated quadrants. Oscillation on the trailing edge can be seen. The crosstalk signal is large.

Signals from the 3 illuminated quadrants are stable and without oscillations. The crosstalk signal (on the darkened quadrant) is now ~5x smaller and has only a negative component. There is no time shift. The trailing edge is 1.5x shorter.

Beam tests of the modified PLANACON

Standard XP85012 Modified





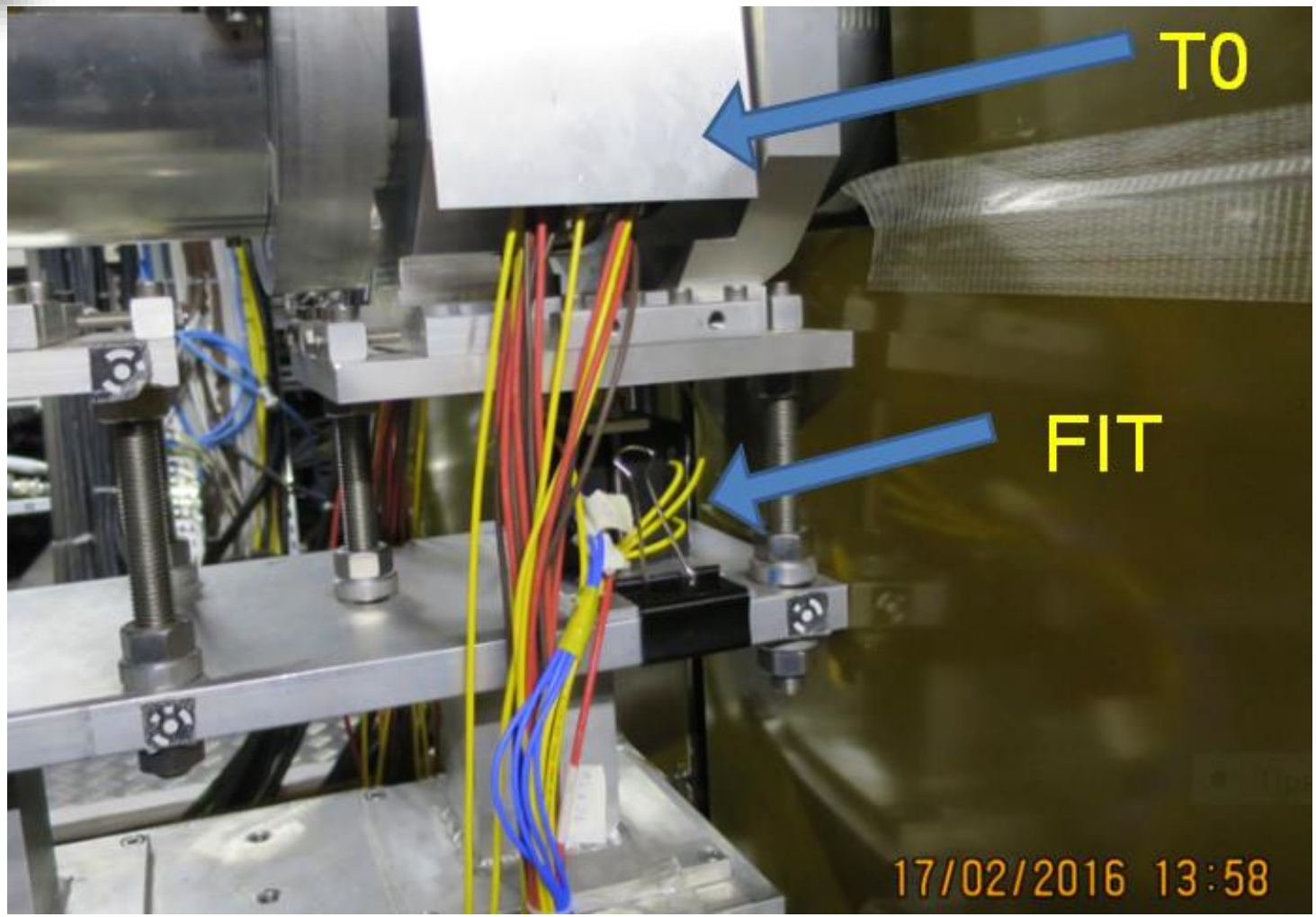
As measured in **June 2015**
Standard XP85012

- MCP amplification 10^6
- Amplitude ~1100 channels
- Time resolution ~**30 ps**

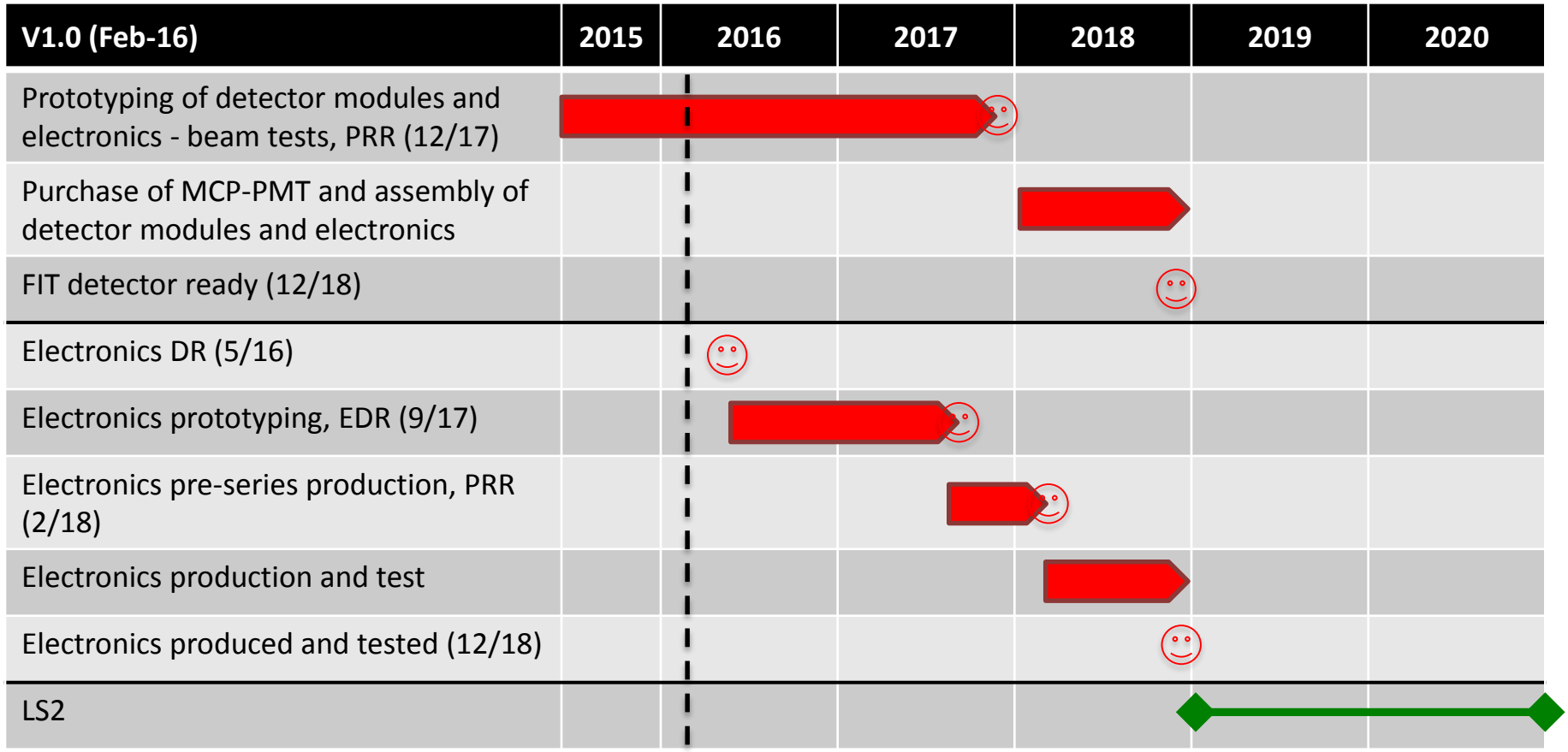
As measured in **October 2015**
Modified XP85012

- MCP amplification 10^6
- Amplitude ~2100 channels
- Time resolution **~22 ps**

Feb 2016: FIT module installed in ALICE



FIT


V1.0 (Feb-16)
2015
2016
2017
2018
2019
2020
Prototyping of detector modules and electronics - beam tests, PRR (12/17)
Purchase of MCP-PMT and assembly of detector modules and electronics
FIT detector ready (12/18)
Electronics DR (5/16)
Electronics prototyping, EDR (9/17)
Electronics pre-series production, PRR (2/18)
Electronics production and test
Electronics produced and tested (12/18)
LS2

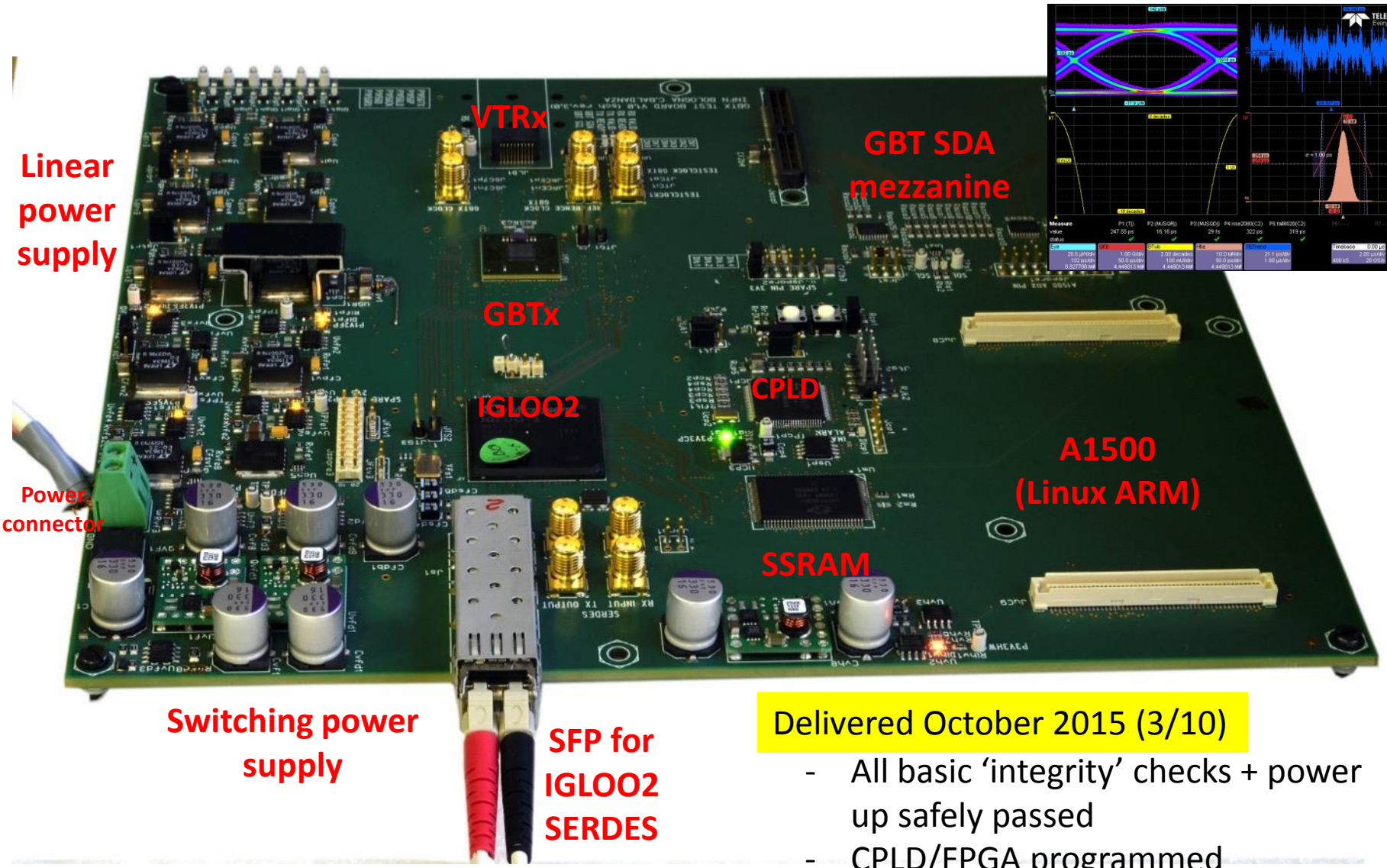
TOF

P. Antonioli

TOF

- Move to continuous readout (1 MHz pp)
- Replacement of the readout card (DRM) in TOF VME crates (72 crates)
- Engineering design review March 2, 2016
- Design of 5 DRM2

TOF GBTX Test Board

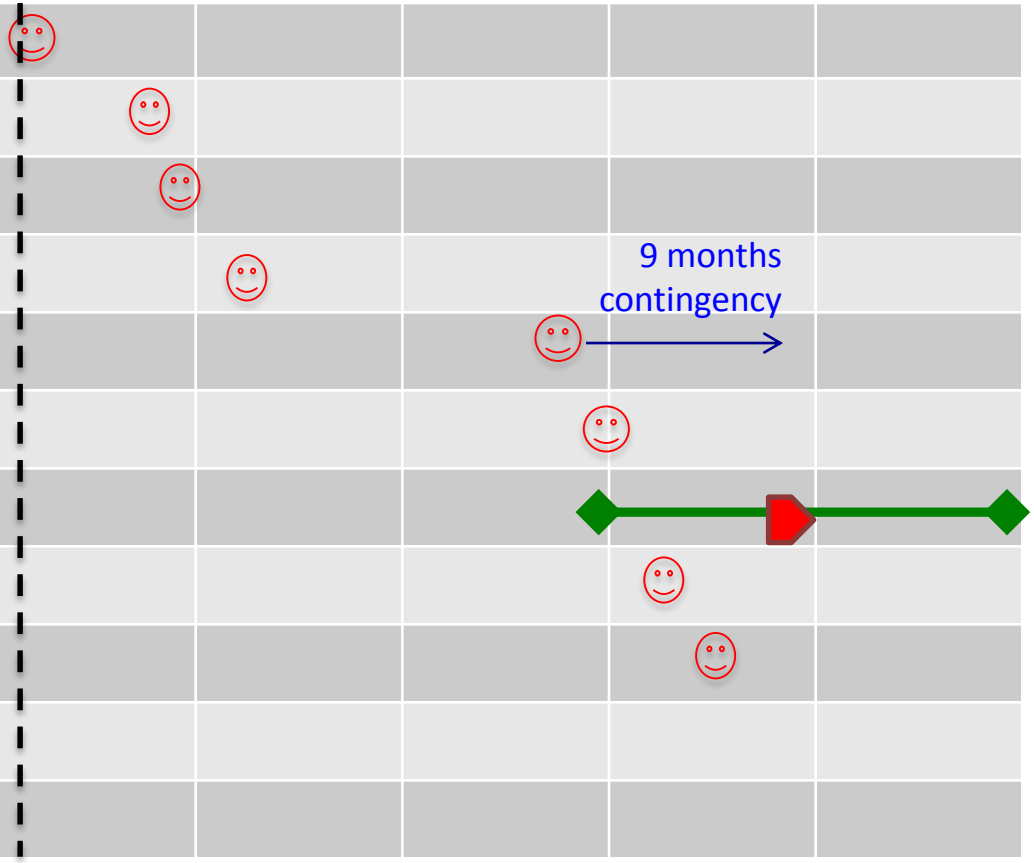


Delivered October 2015 (3/10)

- All basic 'integrity' checks + power up safely passed
- CPLD/FPGA programmed

TOF

V1.0 (Feb-16)	2015	2016	2017	2018	2019	2020
DRM2 prototype EDR (3/16)						
Radiation tests						
DRM2 PRR						
DRM2 tendering						
DRM2 production complete (9/18)						
DRM2 production: te						
DRM2 installation in LS2						
(a) DRM1 extraction						
(b) A1500 from DRM1 in DRM2						
(c) DRM2 installation (*)						
(d) DRM2 commissioning (*)						



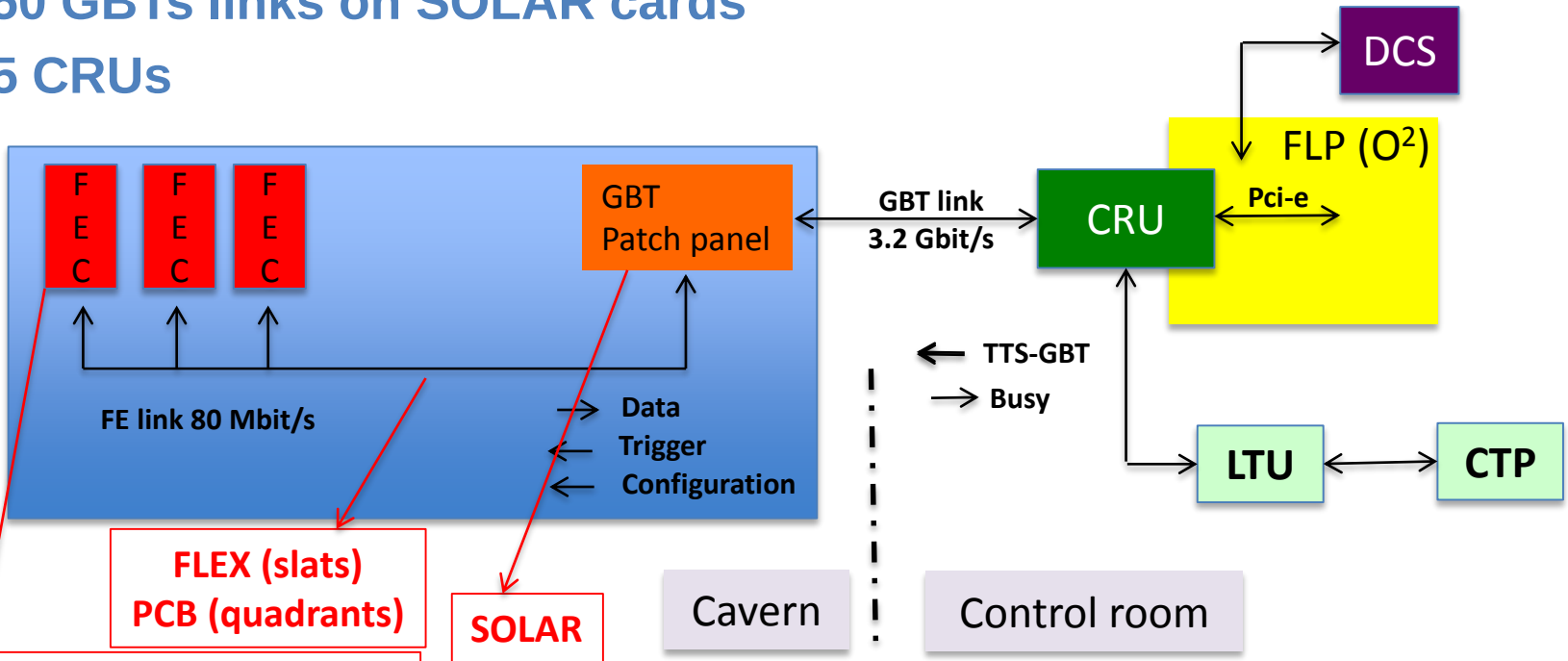
(*) exact timing for (c) and (d) depending on fiber installation schedule

MCH

H. Borel

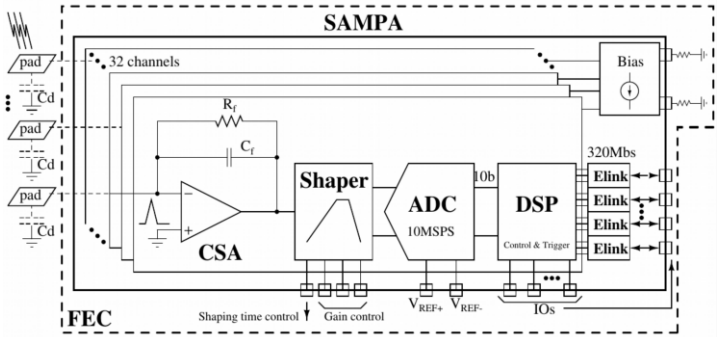
MCH

- 17.000 FE cards (64 ch.) with 2 SAMPA ASIC each=> 1M channels
- 34.000 SAMPA ASIC (32 ch.)
- 550 GBTs links on SOLAR cards
- 25 CRUs



1 FEC = 2 SAMPA = DualSAMPA

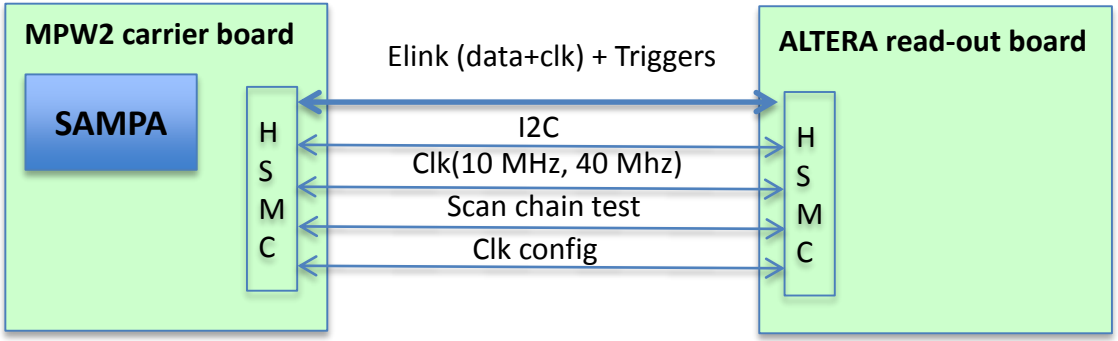
SAMPA = analog + digital



- FEC: Orsay
- FLEX: Cagliari
- GBT board: Saclay
- CRU: India

MCH in SAMPA MPW2 (32 ch) & DualSAMPA tests

- **SAMPA MPW2 (32 ch)**
  - **MPW2 tests:**
  - **Carrier boards for qualification tests in Orsay**

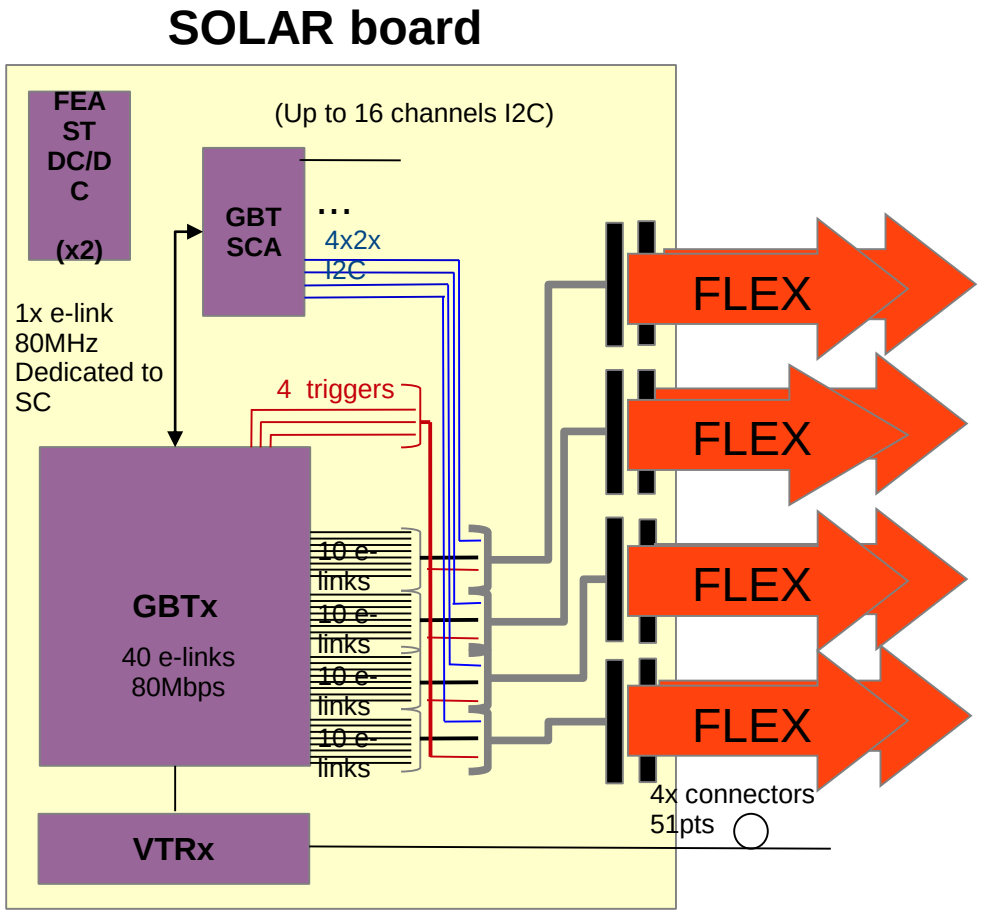


NCCA: 20 boards needed for ALTERA read-out
PCCA: 28 boards needed for ALTERA read-out
PCCV: 11 for VLDB read-out

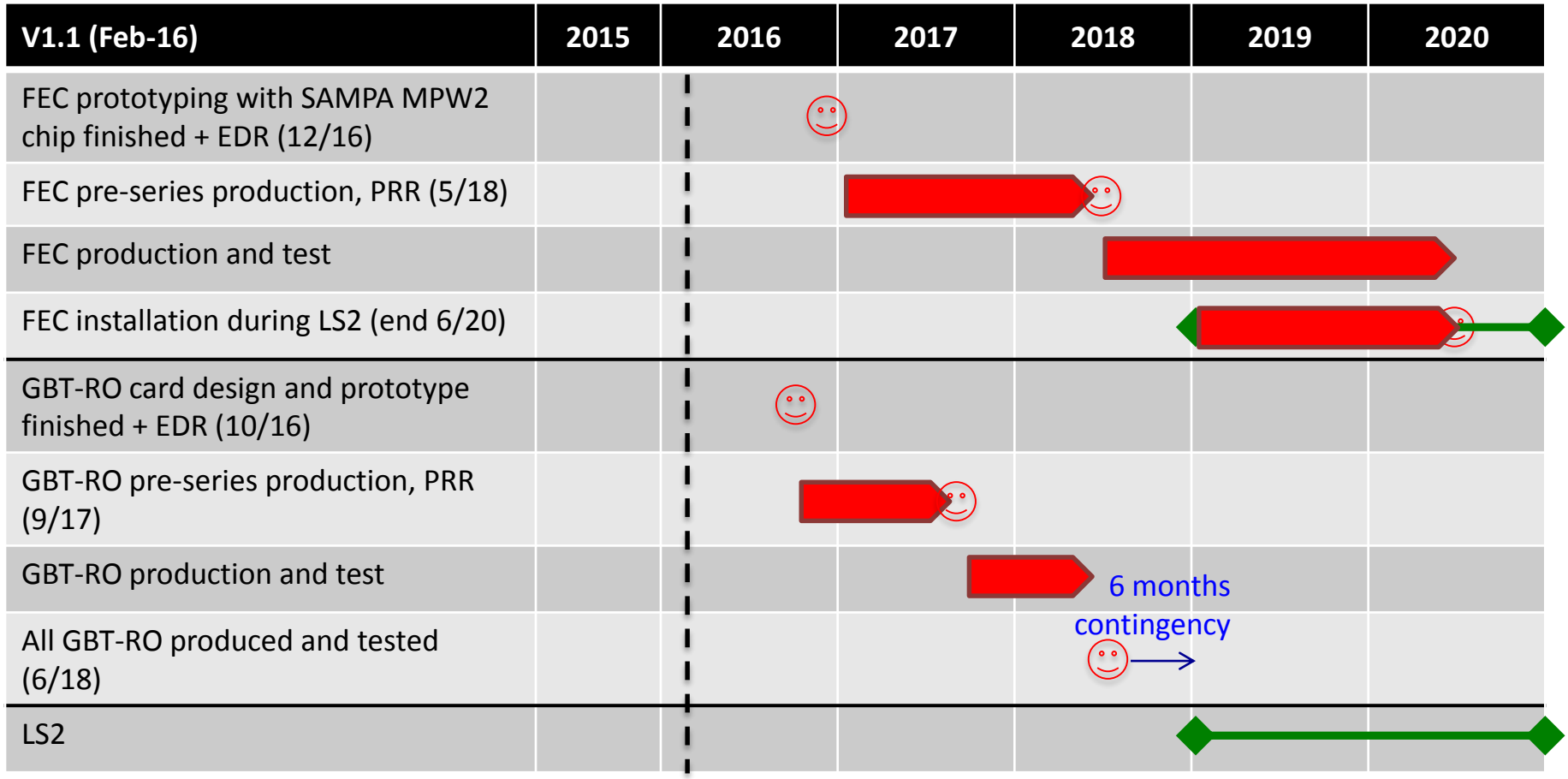
- **DualSAMPA (2 chained SAMPA)**
  - **Design started at Orsay – work in parallel with SAMPA MPW2**
  - **Qualification with test bench (carrier board needed for read-out with ALTERA board)**
  - **Test with detectors: cosmic bench @ Orsay + testbeam (PS: Sep-Oct ; SPS: Oct 2016)**

SOLAR board

- Design by February
- Routing March
- Prototype: May
- SOLAR “standalone” tests: May-June
- Chain read-out tests in lab
- DualSAMPA + FLEX + SOLAR prototypes : Summer
- DualSAMPA + Chain read-out tests
- on detector
- Cosmic bench
- Testbeam
- (PS: Sep-Oct + SPS: end Oct 2016)



MCH

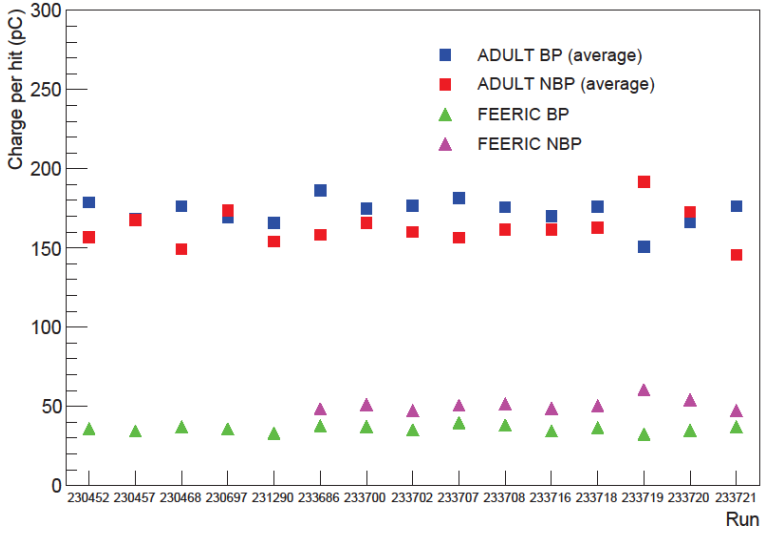

V1.1 (Feb-16)
2015
2016
2017
2018
2019
2020
FEC prototyping with SAMPA MPW2 chip finished + EDR (12/16)
FEC pre-series production, PRR (5/18)
FEC production and test
FEC installation during LS2 (end 6/20)
GBT-RO card design and prototype finished + EDR (10/16)
GBT-RO pre-series production, PRR (9/17)
GBT-RO production and test
6 months contingency
All GBT-RO produced and tested (6/18)
LS2

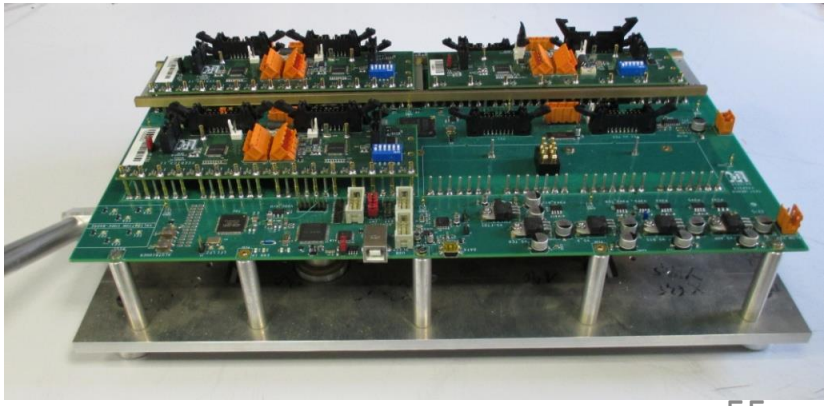
MID

P. Dupieux

MID: front-end

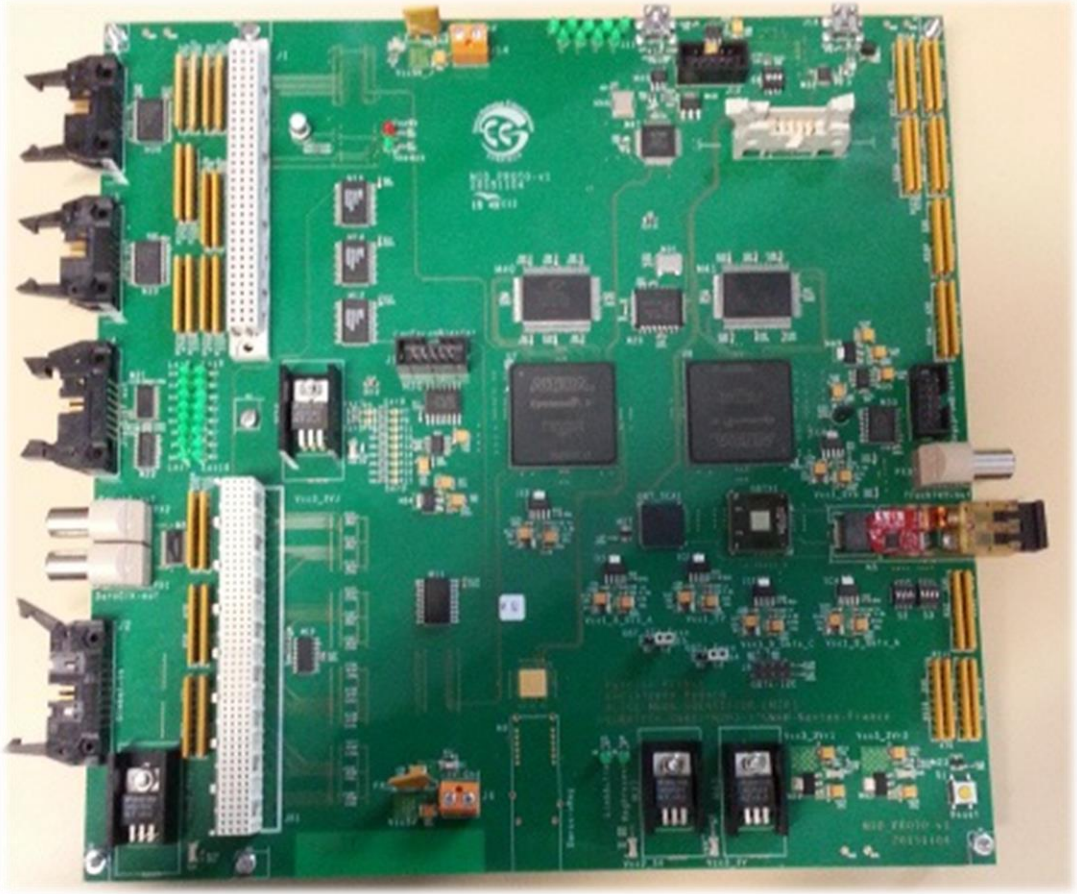
- **Goal: slow down RPC aging after LS2**
- **2384 FE cards (+spares)**
  - Present ASIC ADULT: no amplification
  - Future ASIC FEERIC (0.35 µm CMOS) with amplification
- **FEERIC card pre-series on 1 (/72) RPC in cavern since Feb. 2015**
  - Very satisfactory performance and stability
  - Factor 4 less charge released in the RPC gas with FEERIC (right plot)=> reduced aging
- **Production test bench ready**
  - Up to 4 FEERIC cards tested in parallel
  - Test of ASIC-alone prod. (x4000) early 2016



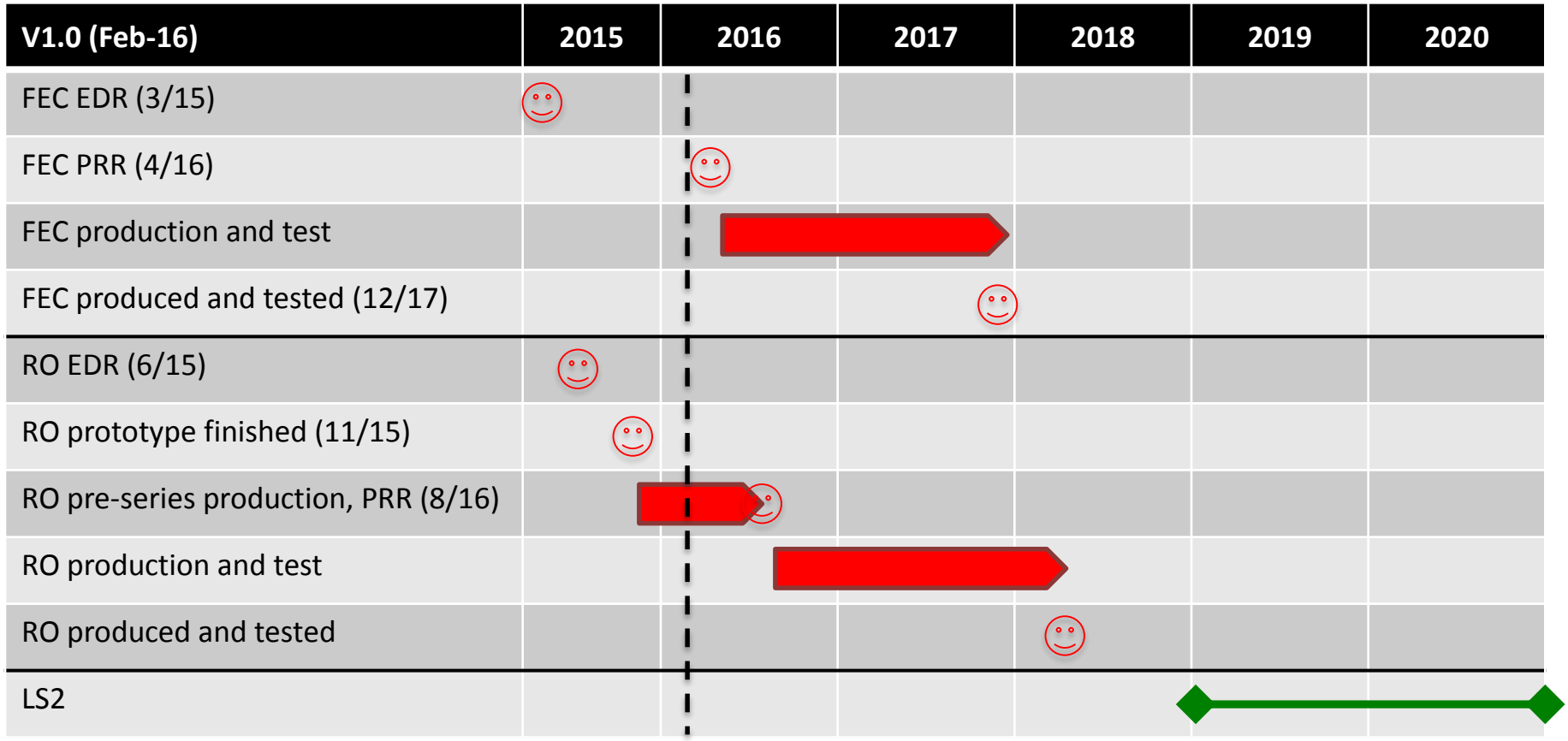


MID: Read-out Electronics

- Continuous read-out
- Replacement of 234 LOCAL and 16 REGIONAL cards presently in operation
- Readout card prototype ready
- EDR June 2015



MID


V1.0 (Feb-16)
2015
2016
2017
2018
2019
2020
FEC EDR (3/15)
FEC PRR (4/16)
FEC production and test
FEC produced and tested (12/17)
RO EDR (6/15)
RO prototype finished (11/15)
RO pre-series production, PRR (8/16)
RO production and test
RO produced and tested
LS2

Summary

- Architecture stream lined
  - all upgraded detectors use CRU
  - all upgraded detectors have continuous read-out capability
- TPC processing moved to CRU
- SAMPA MPW1 shows good results
- SAMPA MPW2 submitted
- FIT prototyping successful & continuous read-out
- TOF continuous read-out & read-out card prototype
- MCH read-out board design started
- MID installed pre-series good results
- MID read-out prototyping ready