A background image of a complex printed circuit board (PCB) with various electronic components, including integrated circuits, capacitors, and connectors. The board is populated with numerous components, and the text is overlaid on this image.

# The ATLAS Level-1 Calorimeter Trigger Preprocessor in Run-2

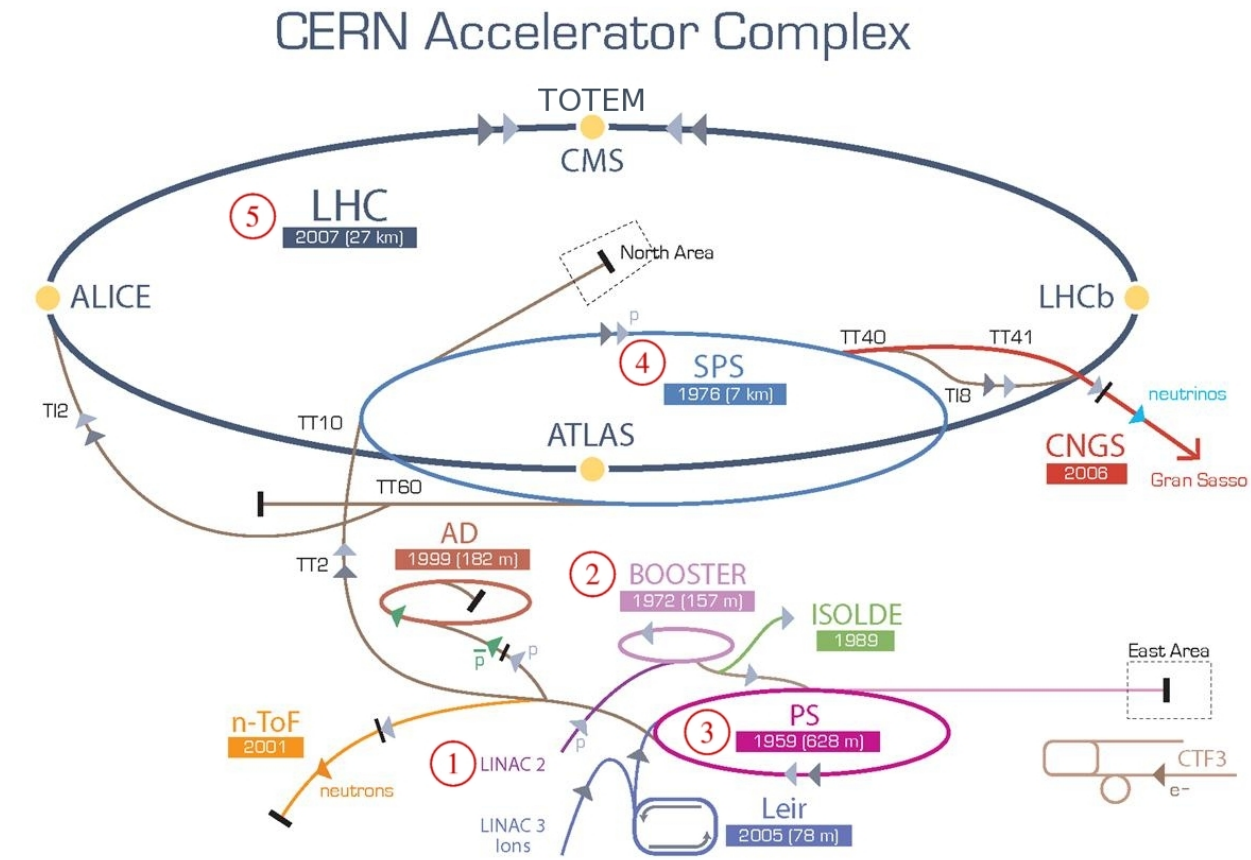
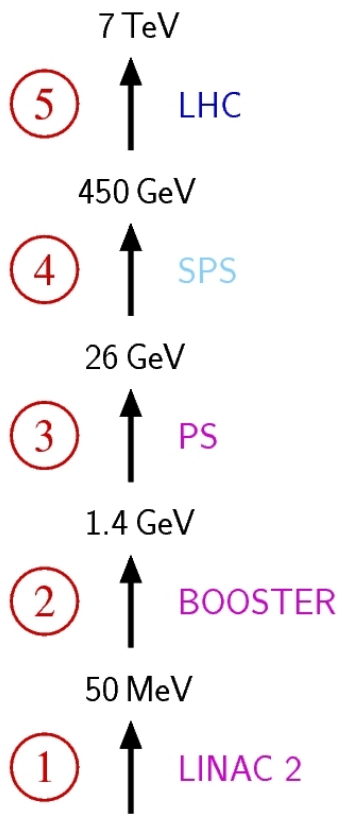
Jan Jongmanns  
HighRR Seminar

17.02.2016

# -Outline-

- LHC & ATLAS
- ATLAS Trigger
- L1Calo Preprocessor
- New Run-2 Features
- Summary

# -LHC & ATLAS- The LHC Accelerator



▶ p [proton] ▶ ion ▶ neutrons ▶  $\bar{p}$  [antiproton] ↔ proton/antiproton conversion ▶ neutrinos ▶ electron

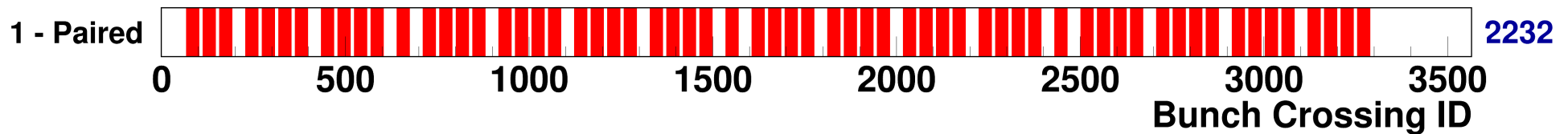
LHC Large Hadron Collider SPS Super Proton Synchrotron PS Proton Synchrotron

AD Antiproton Decelerator CTF3 Clic Test Facility CNGS Cern Neutrinos to Gran Sasso ISOLDE Isotope Separator OnLine DEvice

LEIR Low Energy Ion Ring LINAC LINear ACcelerator n-ToF Neutrons Time Of Flight

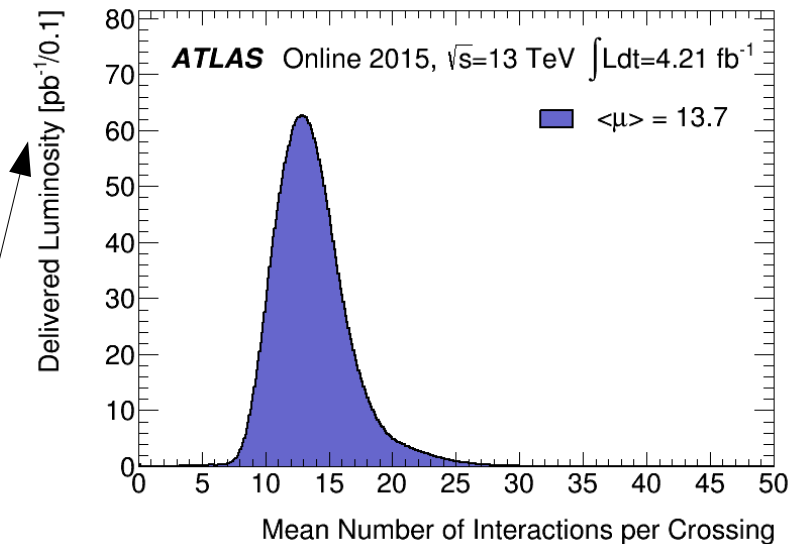
# -LHC & ATLAS- LHC Beam Setup

- LHC circulates protons in separated '**bunches**' of  $10^{11}$  particles
  - 3564 possible bunch slots, >2000 'filled' in good runs
  - Bunches collide at up to 40.08 MHz (25 ns 'bunch spacing')



- Each 'bunch crossing' (BC) produces several pp collisions
  - Typically few 'interesting' events rest -> '**pile-up**'

$1 \text{ pb}^{-1} \sim 10^{11} \text{ coll.}$



# -LHC & ATLAS- LHC Runs

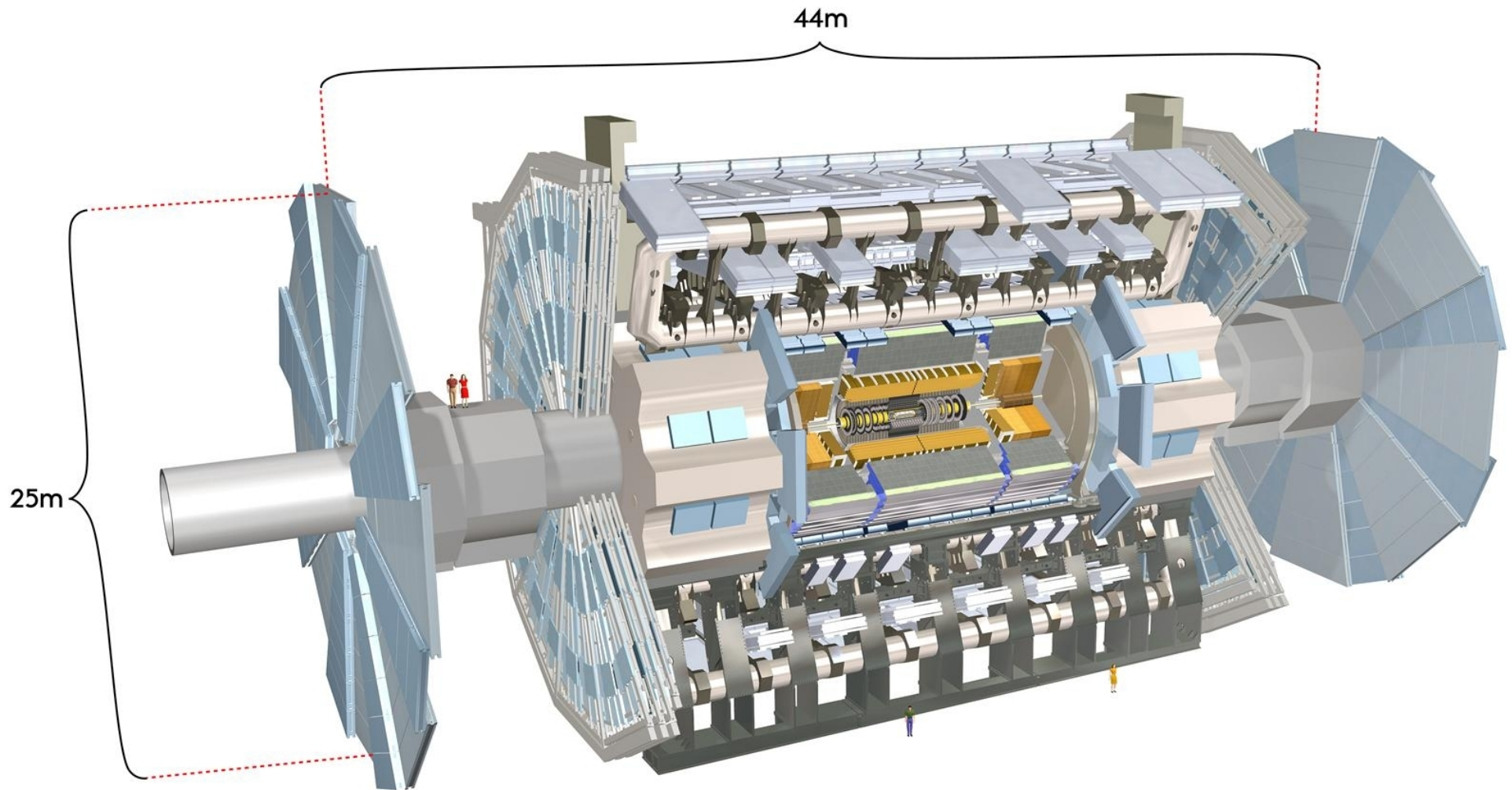
## **Run-1** (2009-2013)

- LHC parameters
  - $\sqrt{s} = 7\sim 8$  TeV
  - $L = \sim 7 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$
  - Bunch spacing 50 ns
- Physics results
  - Higgs discovery
  - Quark gluon plasma
  - New baryons, pentaquarks
  - Limits, limits, limits ...

## **Run-2** (2015-2018)

- LHC parameters
  - $\sqrt{s} = 13\sim 14$  TeV
  - $L = \sim 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
  - Bunch spacing 25 ns
- Physics goals
  - Higgs properties
  - Higher limits, ...
  - ???

# -LHC & ATLAS- ATLAS Detector

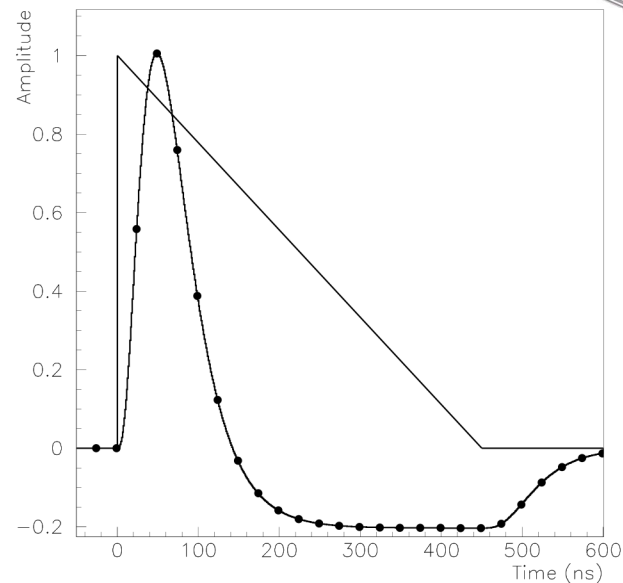
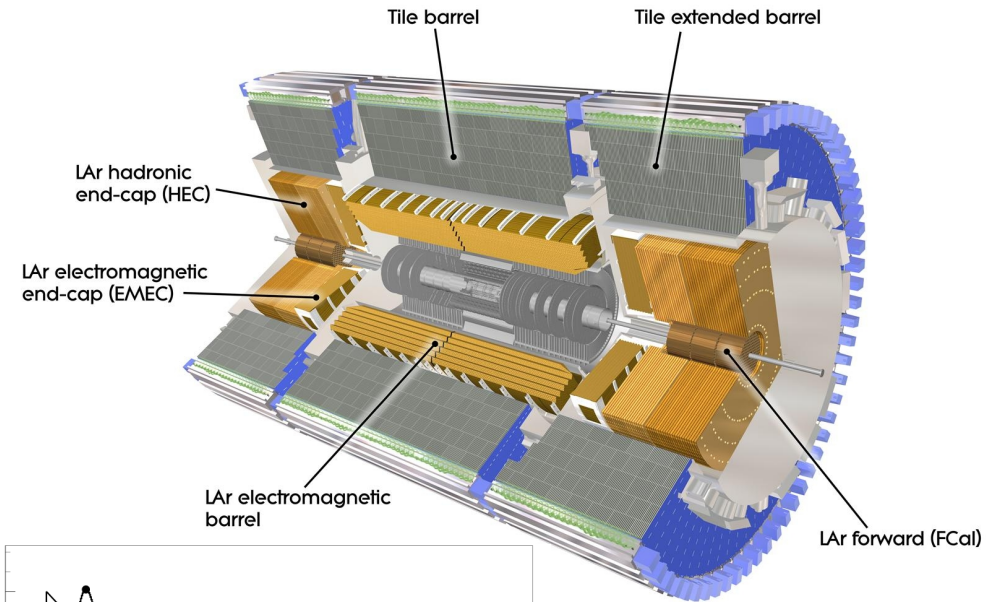


# -LHC & ATLAS- ATLAS Calorimeter

## Sampling calorimeter

- Active medium
  - Liquid argon
  - Scintillating tiles
- Absorber
  - Lead (Central LAr)
  - Copper (Forward LAr)
  - Stainless Steel (Tile)

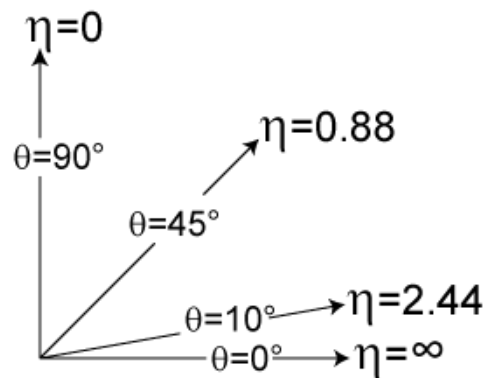
Front-end electronics  
produce bipolar pulsheshape



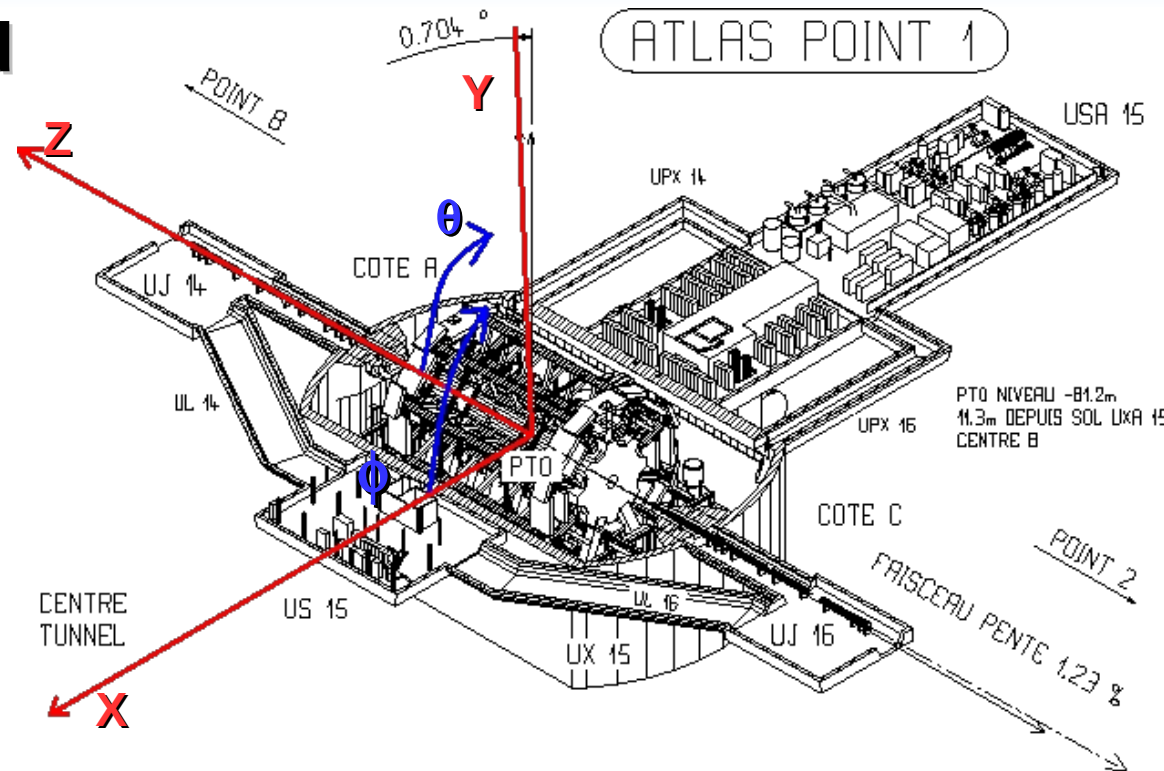
# -LHC & ATLAS- ATLAS Coordinates

ATLAS uses **right-handed polar coordinate system**

- Instead of polar angle  $\theta$ , use pseudorapidity  $\eta$
- $\eta = - \ln( \tan( \theta/2 ) )$



In relativistic limit,  $\eta = y$

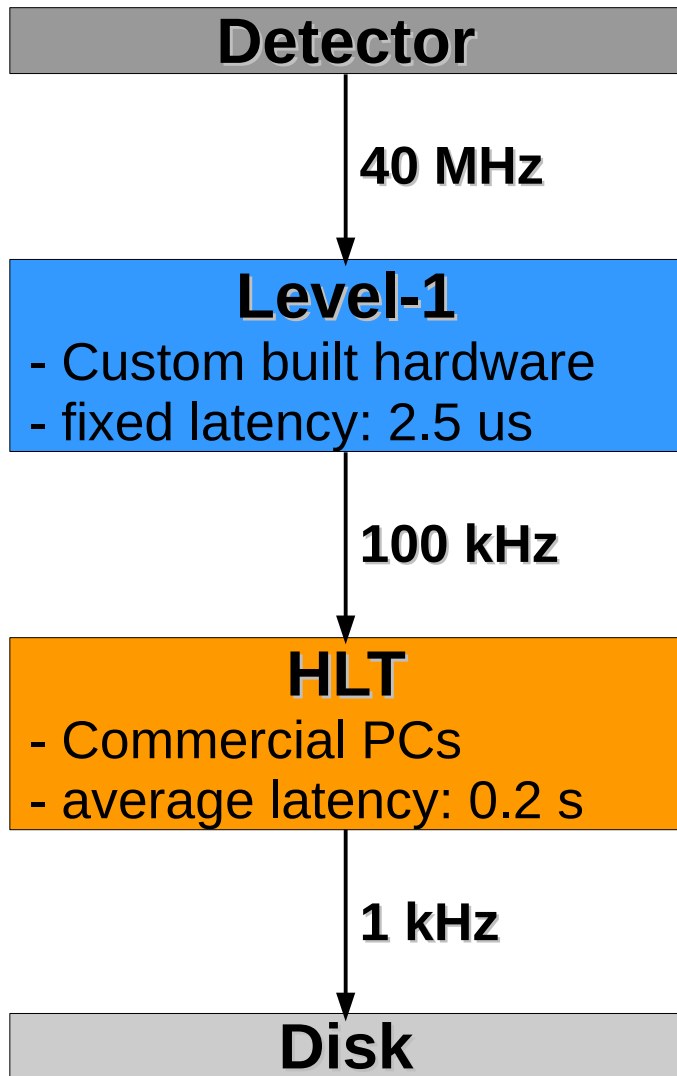


$$\text{Rapidity } y = \frac{1}{2} \ln( (E+p_L)/(E-p_L) )$$

- $\Delta y$  invariant under Lorentz transformation
- Particle flow  $\sim$  constant in  $y$



# -ATLAS Trigger- Overview



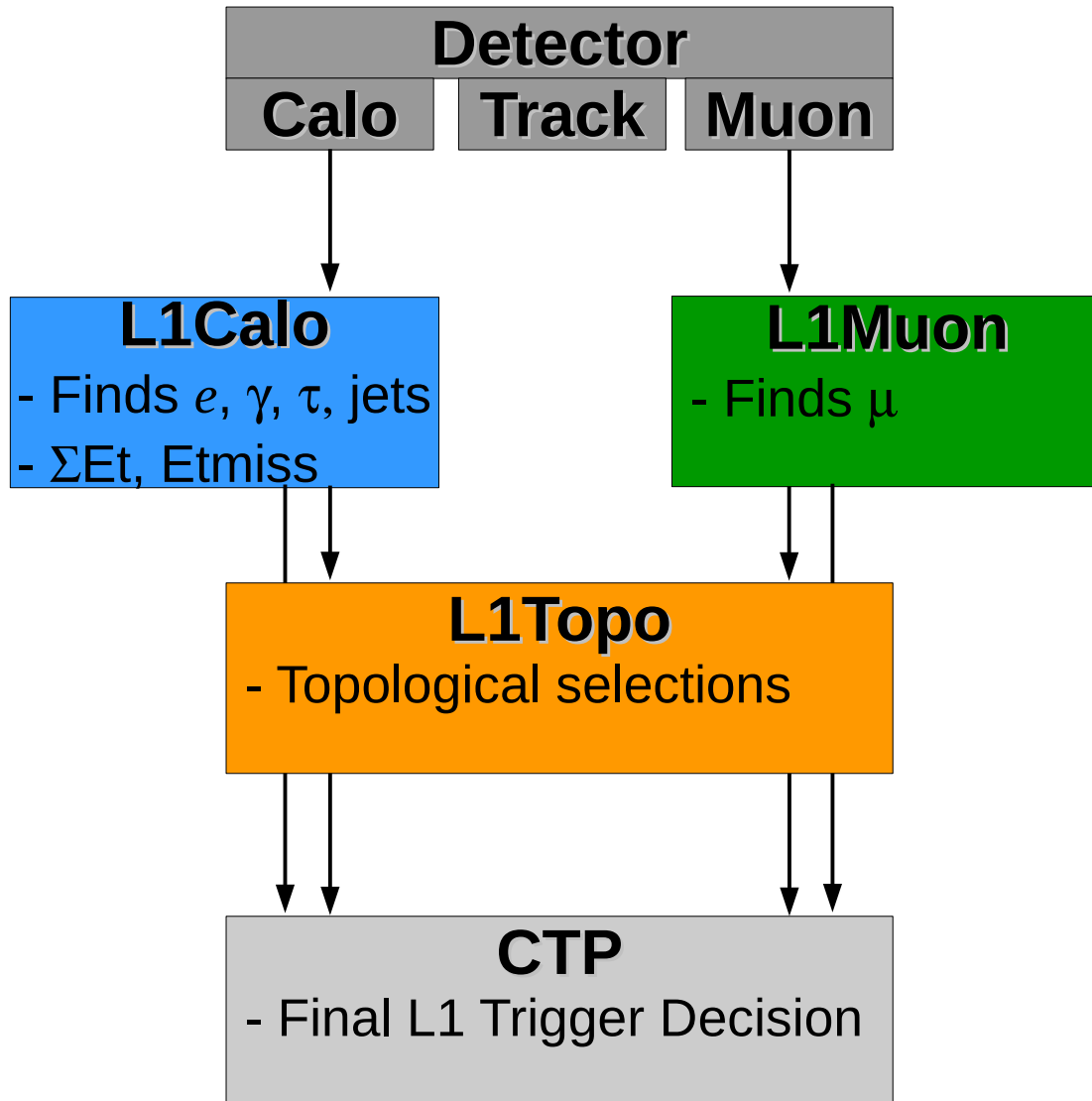
## Level-1

- Reduced granularity
- Calorimeter & muon only
- Triggers on object multiplicity
- Reduction factor: 400

## High-Level-Trigger

- Reconstructs full event
- Offline-like algorithms
- Reduction factor: 100

# -ATLAS Trigger- Level-1 Trigger



## L1 Trigger systems

- find object candidates  
(e.g.  $e > 10 \text{ GeV}$ )

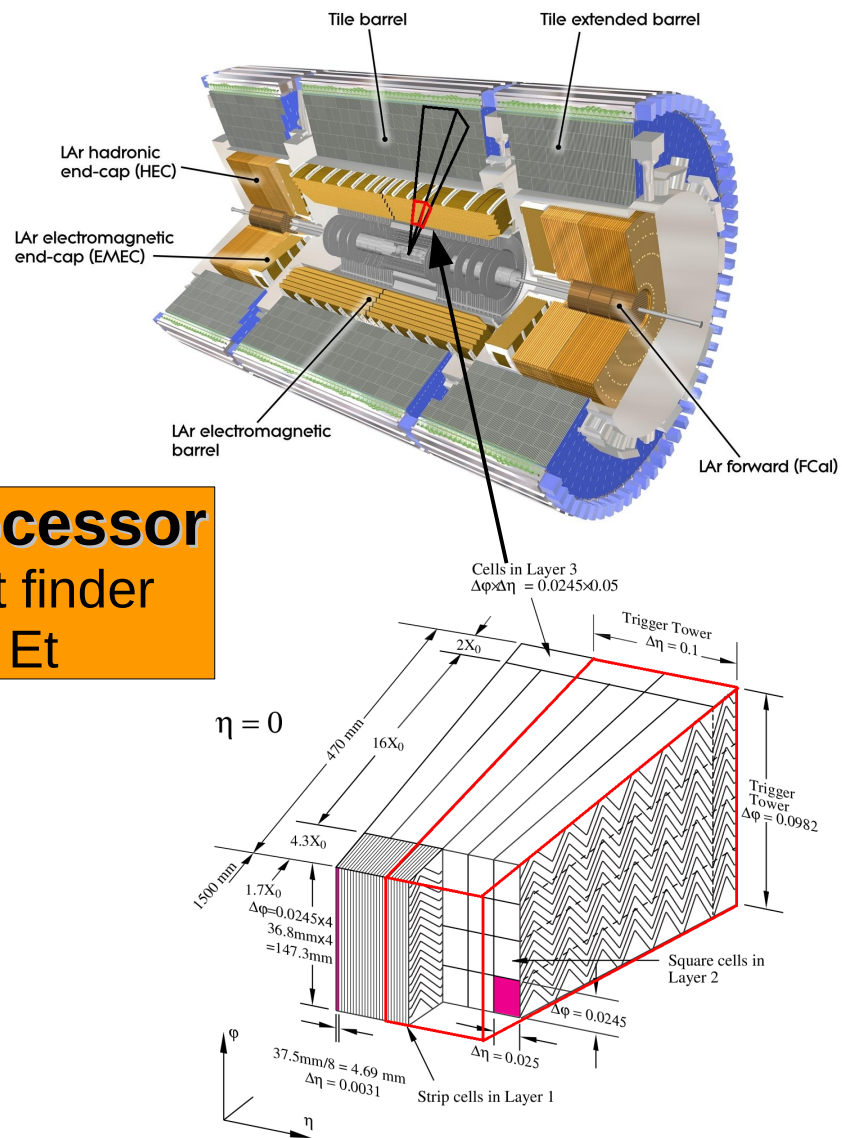
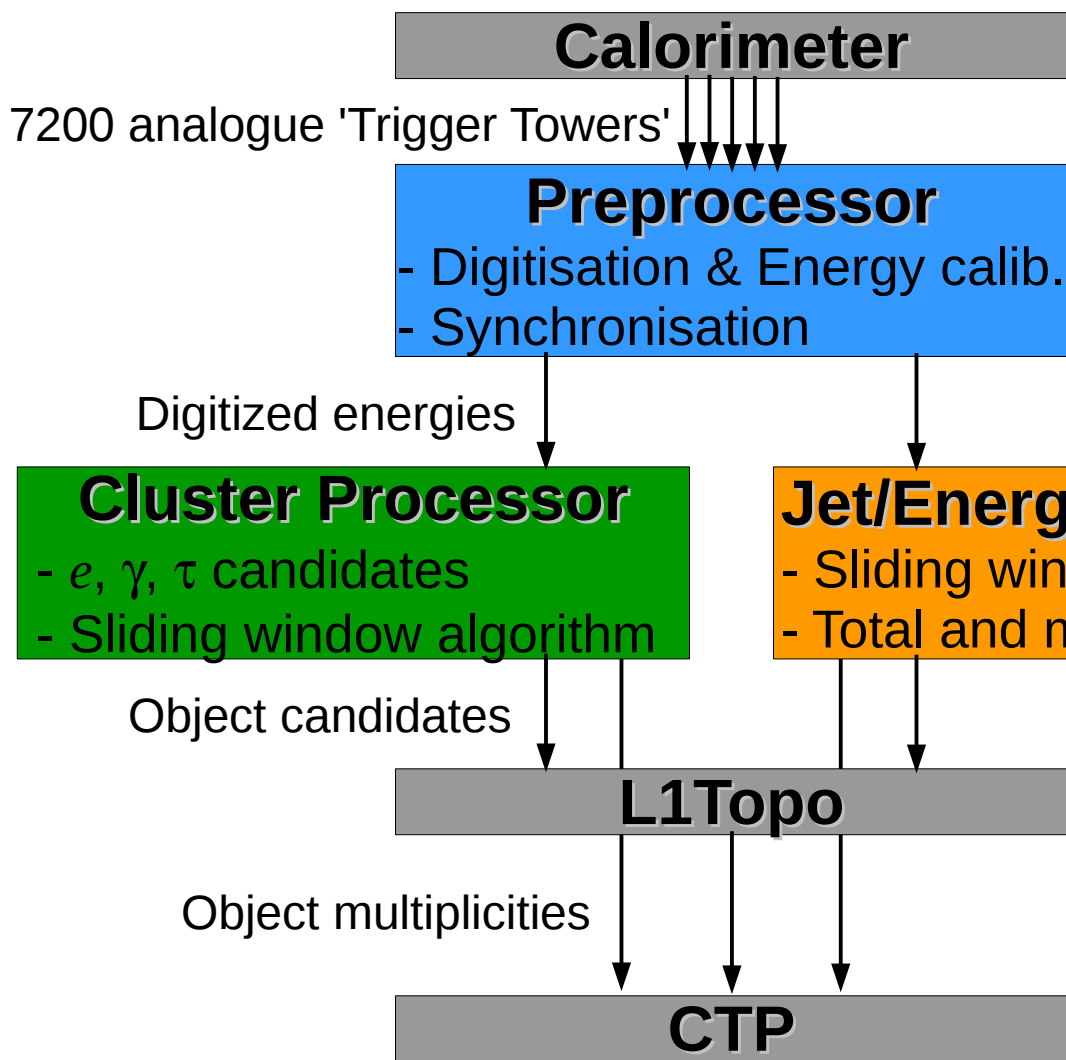
## Topological Processor

- sophisticated selections  
(e.g.  $m_{jj} > 50 \text{ GeV}$ )

## Central Trigger Processor

- Trigger based on object multiplicities  
(e.g. at least  $2 \mu > 30 \text{ GeV}$ )

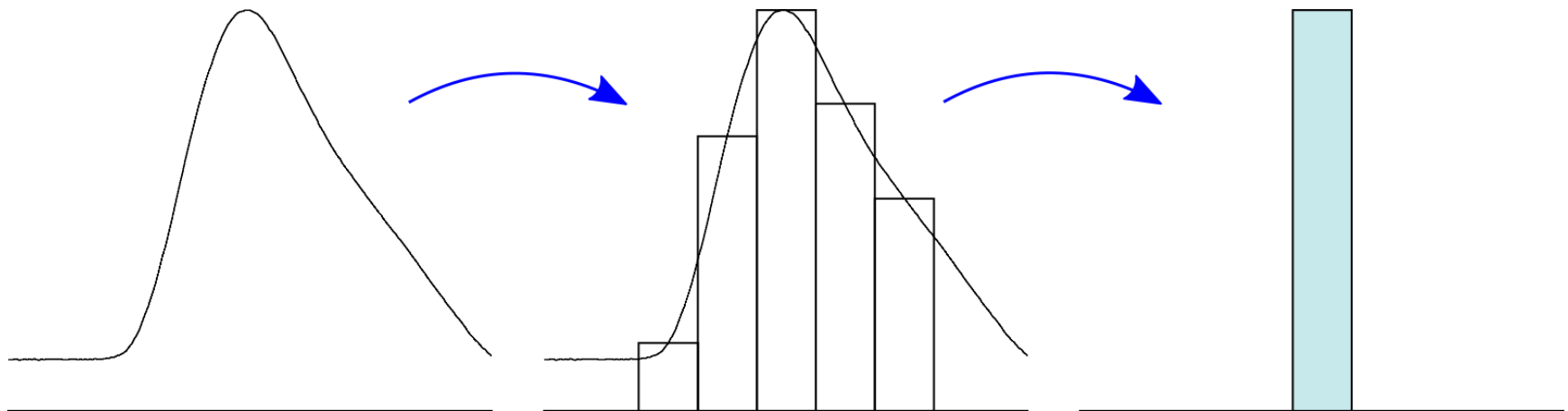
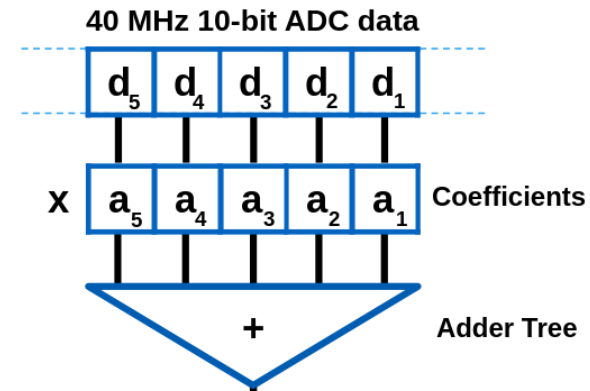
# -ATLAS Trigger- Level-1 Calorimeter Trigger



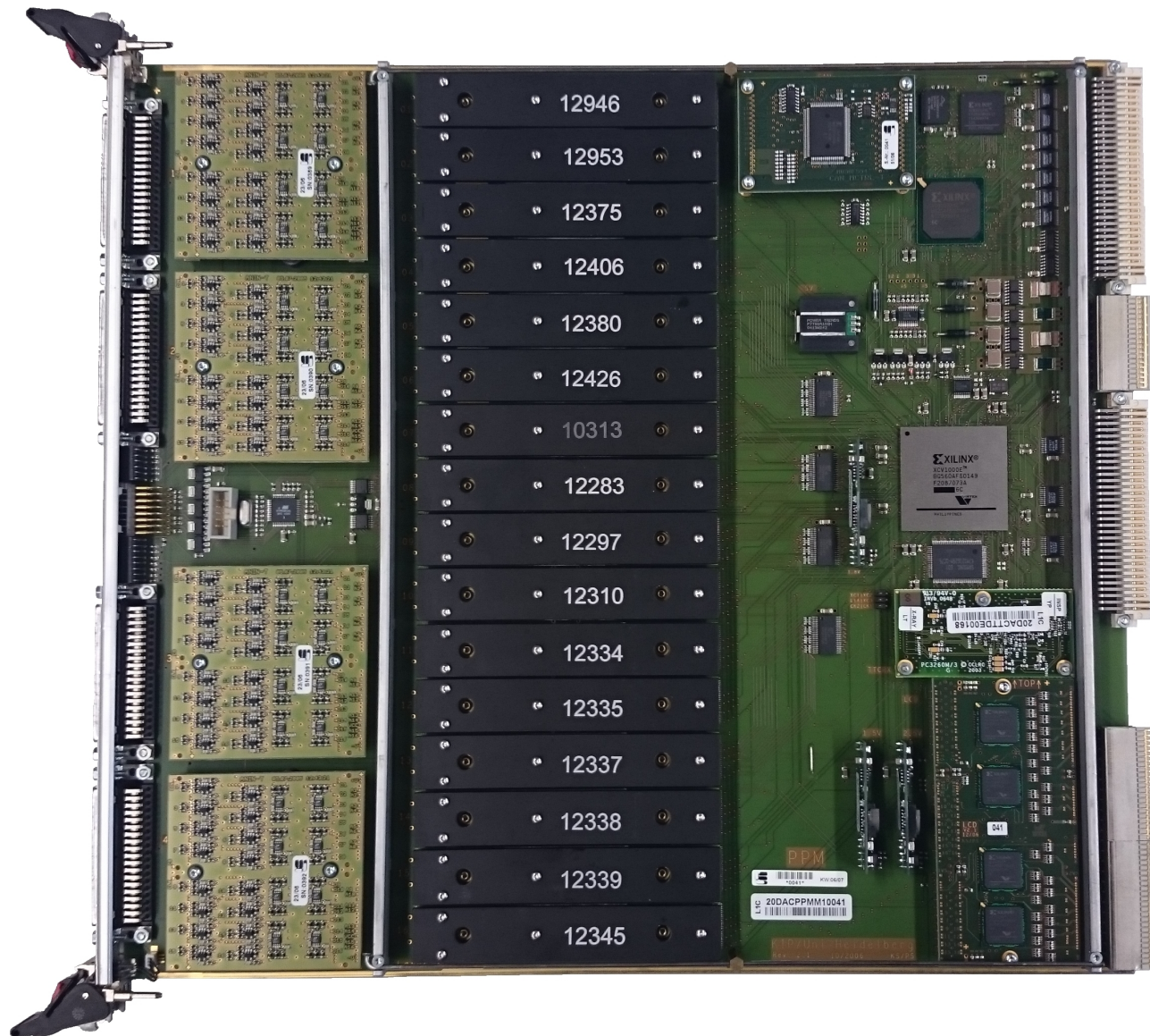
# -L1Calo Preprocessor- Functionality

Preprocessor prepares calorimeter signals for object finding

- Digitization of analogue calorimeter signals
- Synchronization of digital signals
- Digital filter to reduce noise
- Peak-Finding to identify energy deposition
- Calibration of signal amplitudes to GeV scale energies



# -L1Calo Preprocessor- Hardware Implementation



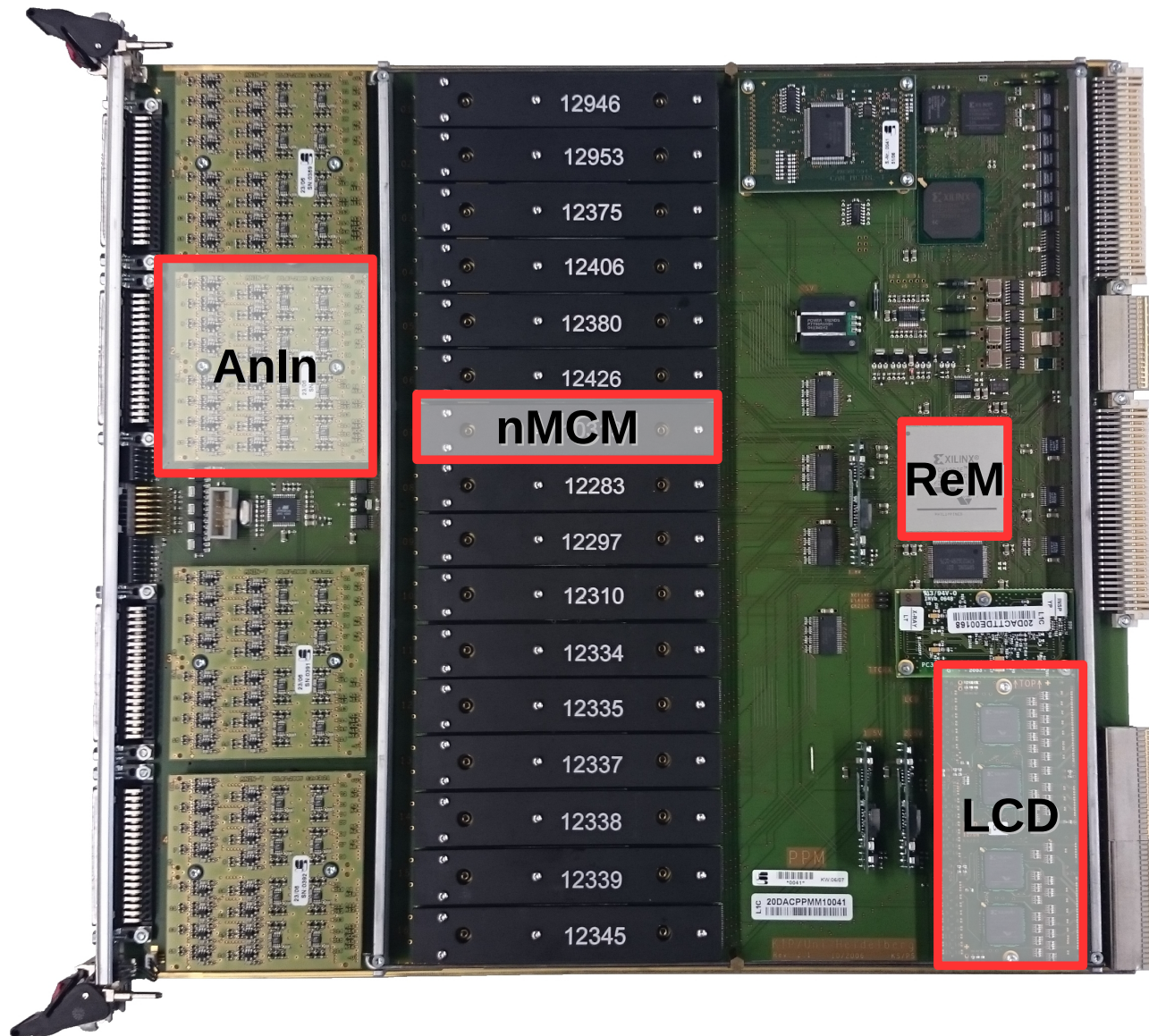
To handle 7200 channels

- Highly **parallel** ...
- ... **modular** system

## **Preprocessor Module**

- 128 Modules total
- 64 channels each

# -L1Calo Preprocessor- Preprocessor Module



## **Analogue Input Board**

- Signal Shaping

## **(new) Multichip Module**

- Main Processing Unit

## **Readout Merger**

- Readout & Config.

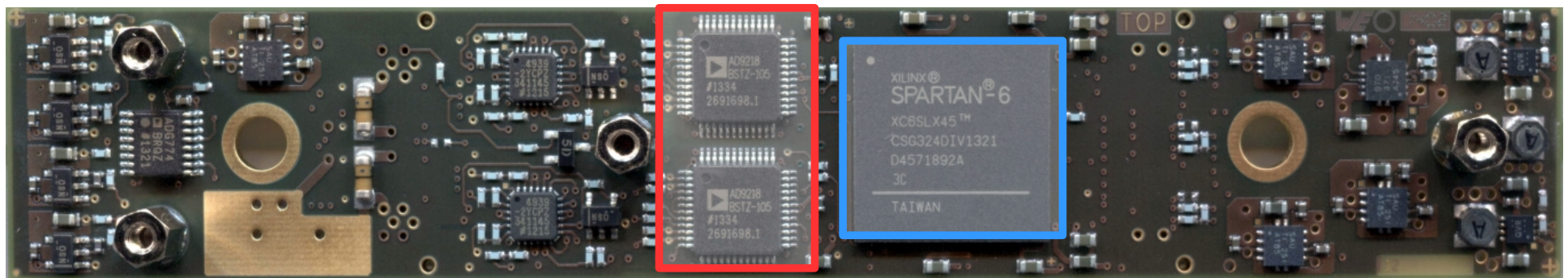
## **LVDS Cable Driver**

- Data to Processors

# -L1Calo Preprocessor- The new Multichip Module

16 nMCM / PPM (2048 total) - 4 channel / MCM

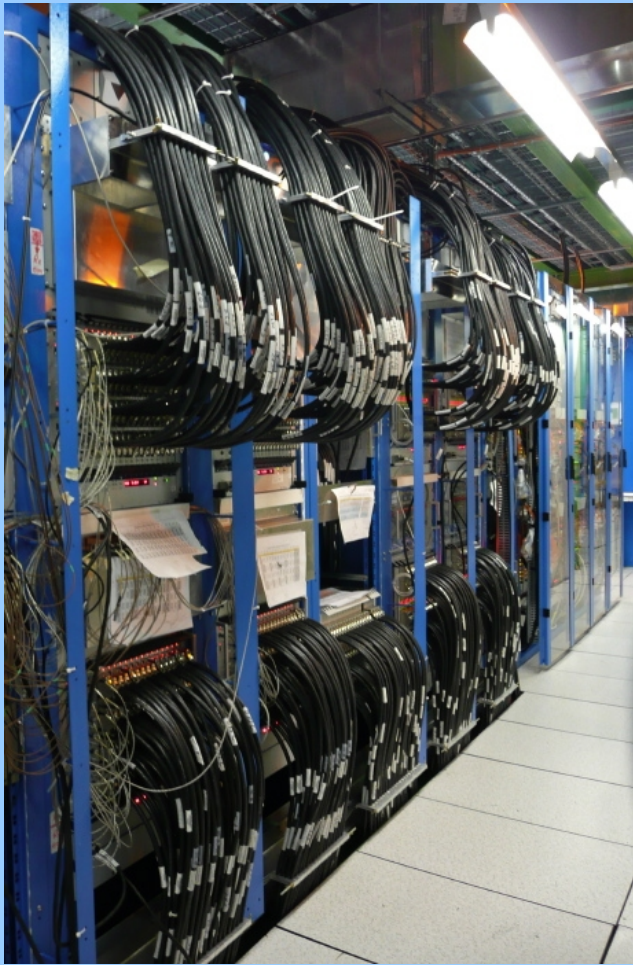
**2x dual-channel FADC**  
- 80 MHz, 10-bit



**'Calippr' FPGA** (CALorimeter Information PrePRocessor)

- Synchronization FIFOs for input signals
- Digital Filter to reduce thermal & pile-up noise
- Identification and measurement of energy deposition
- Stronger chip than Run-1, allows more advanced algorithms

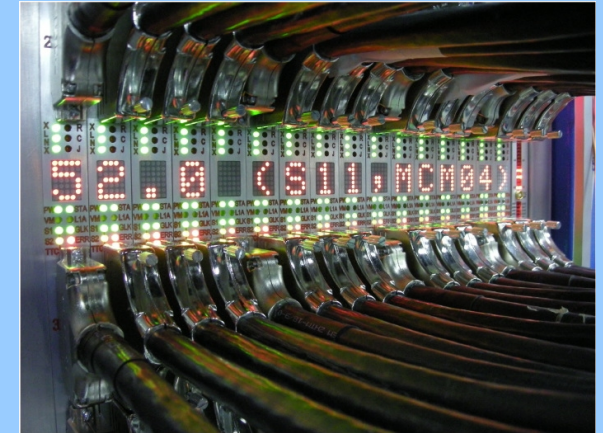
# -L1Calo Preprocessor- Impressions from the Cavern



Cables from calorimeter into  
Receivers and Preprocessor



LVDS cables to Processors  
on backside of Preprocessor



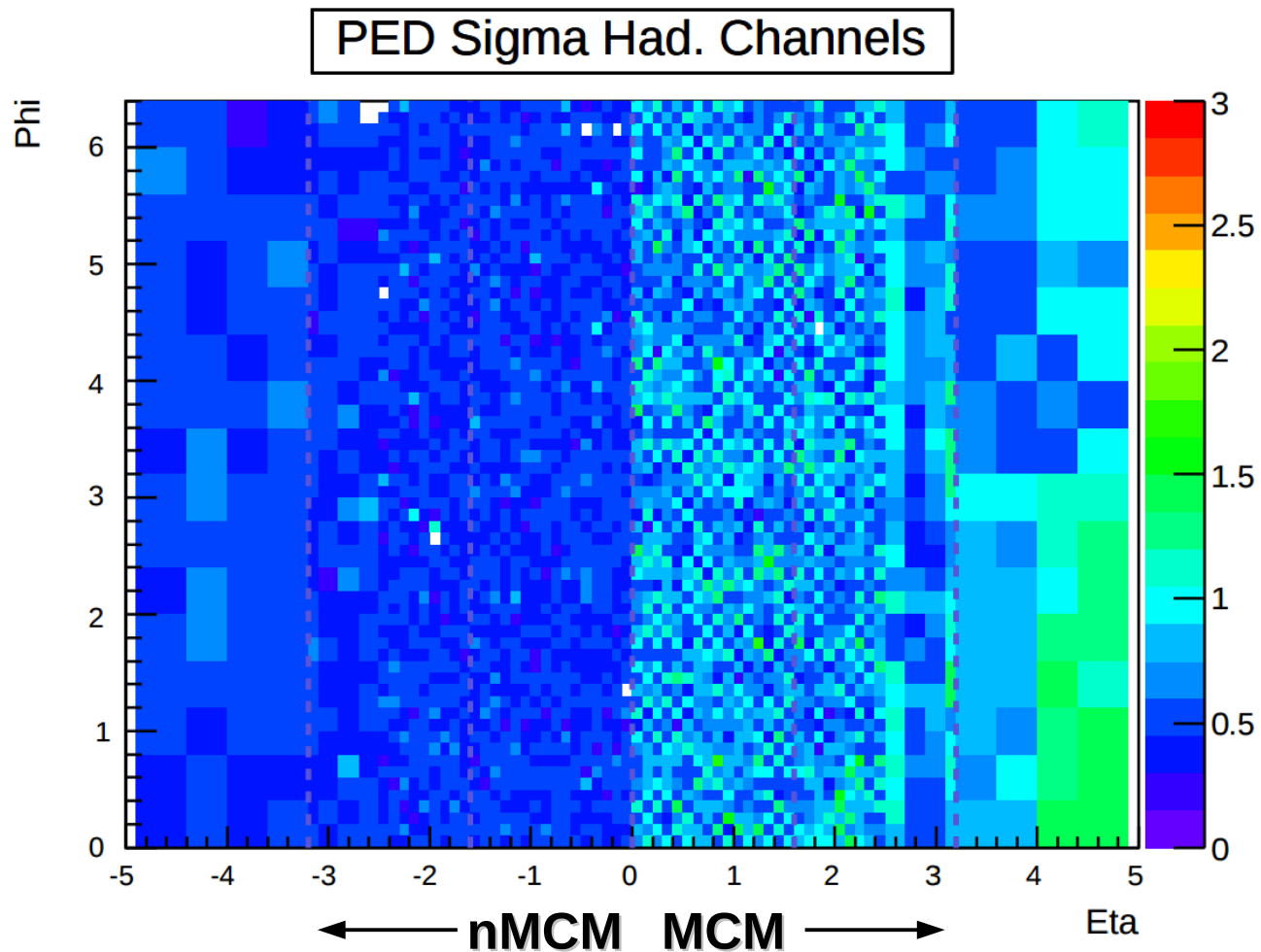
Preprocessor display shows  
temperature & position of  
hottest MCM



# -L1Calo Preprocessor- Run-2 Hardware Performance

Run-2 system outperforms Run-1 Hardware in many ways

- **Noise smaller & more homogeneous**, less fine timing effect on ADC, ...

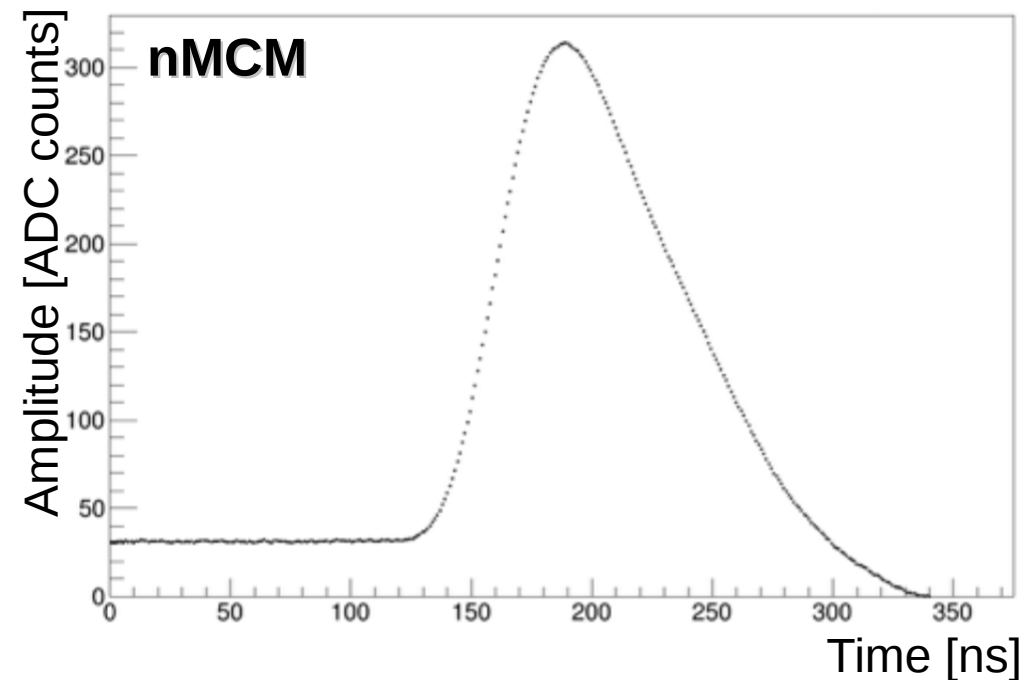
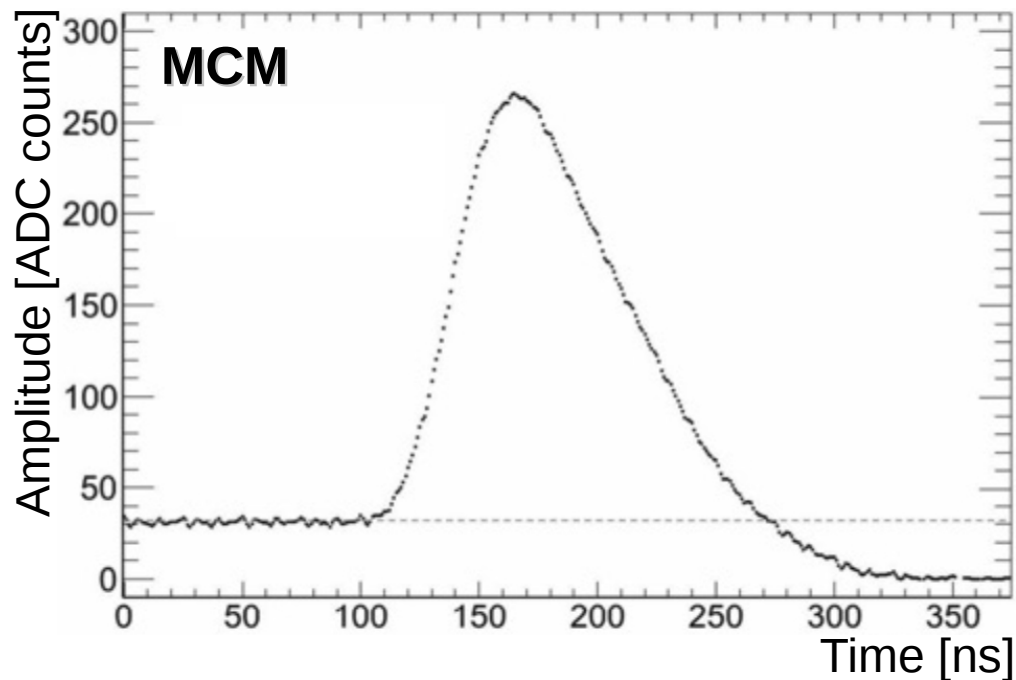


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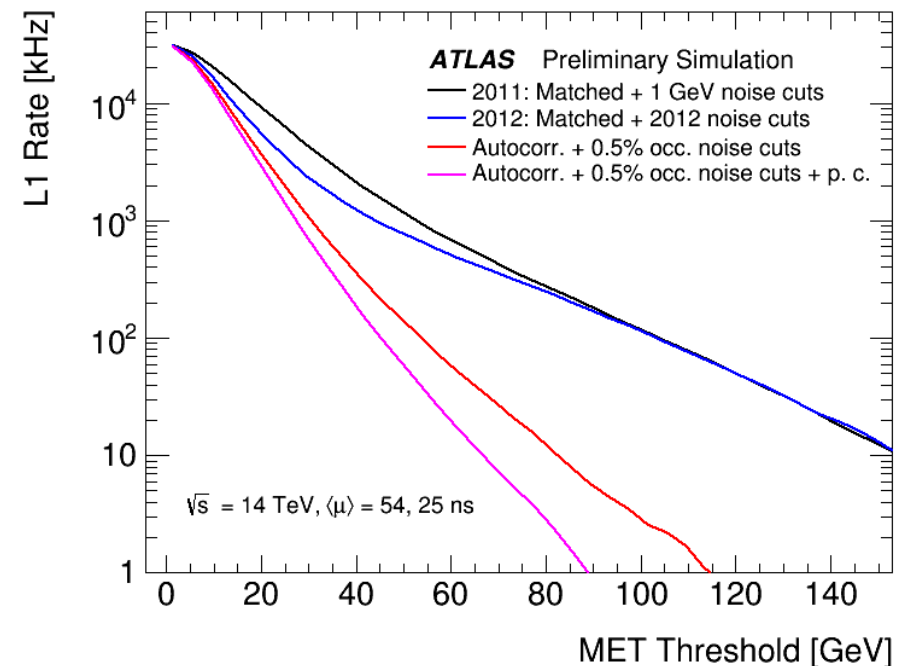
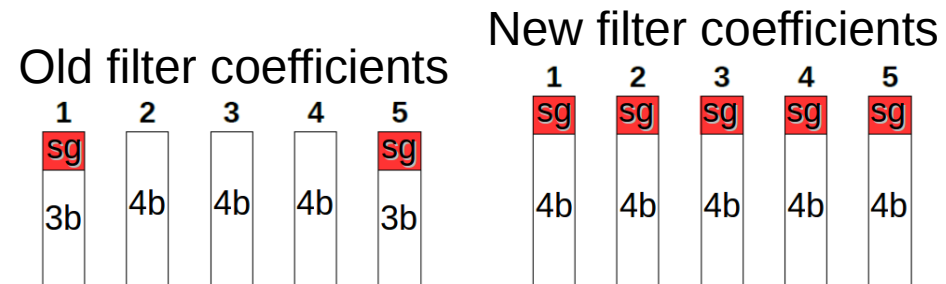
Reconstructed pulse shapes by scanning ADC strobe in 1 ns steps



# -New Run-2 Features- Overview

New MCM allows for many new & enhanced algorithms

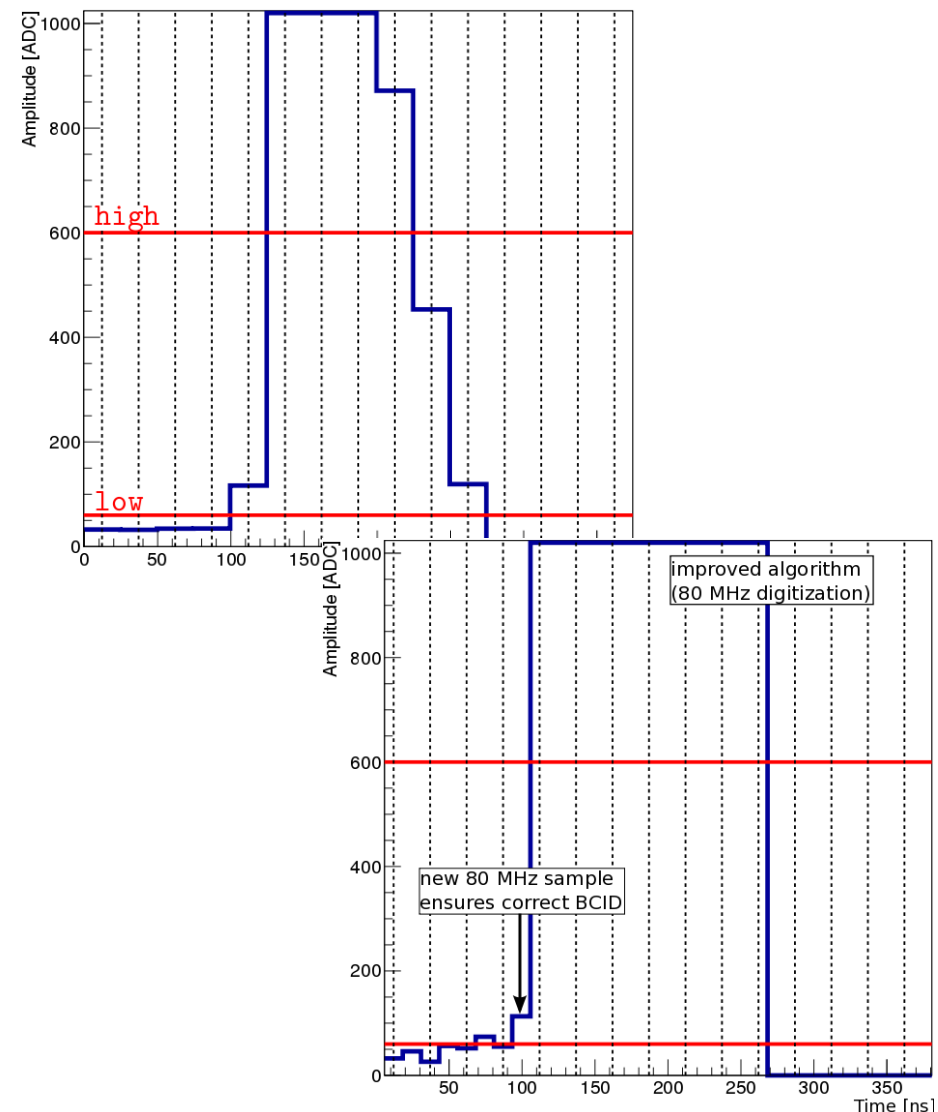
- **More flexible digital filters allow better pile-up noise treatment**
- Use 80 MHz digitisation to enhance processing of saturated signals
- Separate energy calibrations for CP and JEP systems
- Dynamic correction for pile-up induced fluctuations of baseline



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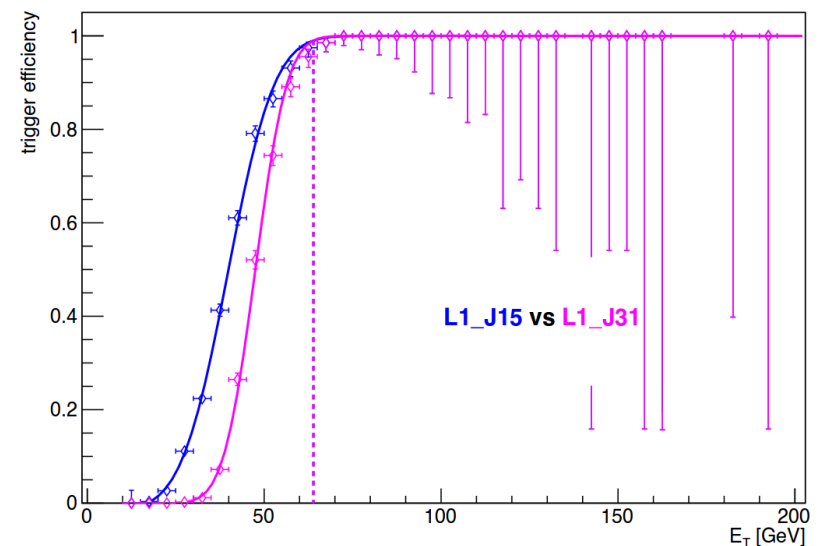
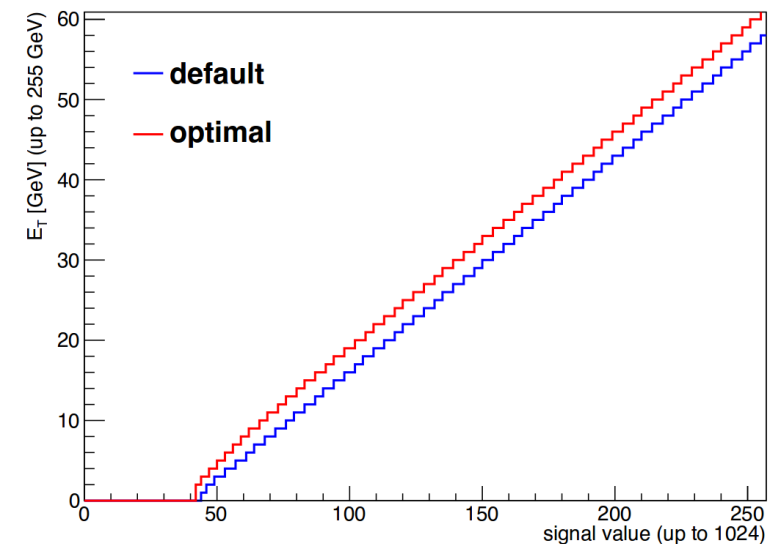
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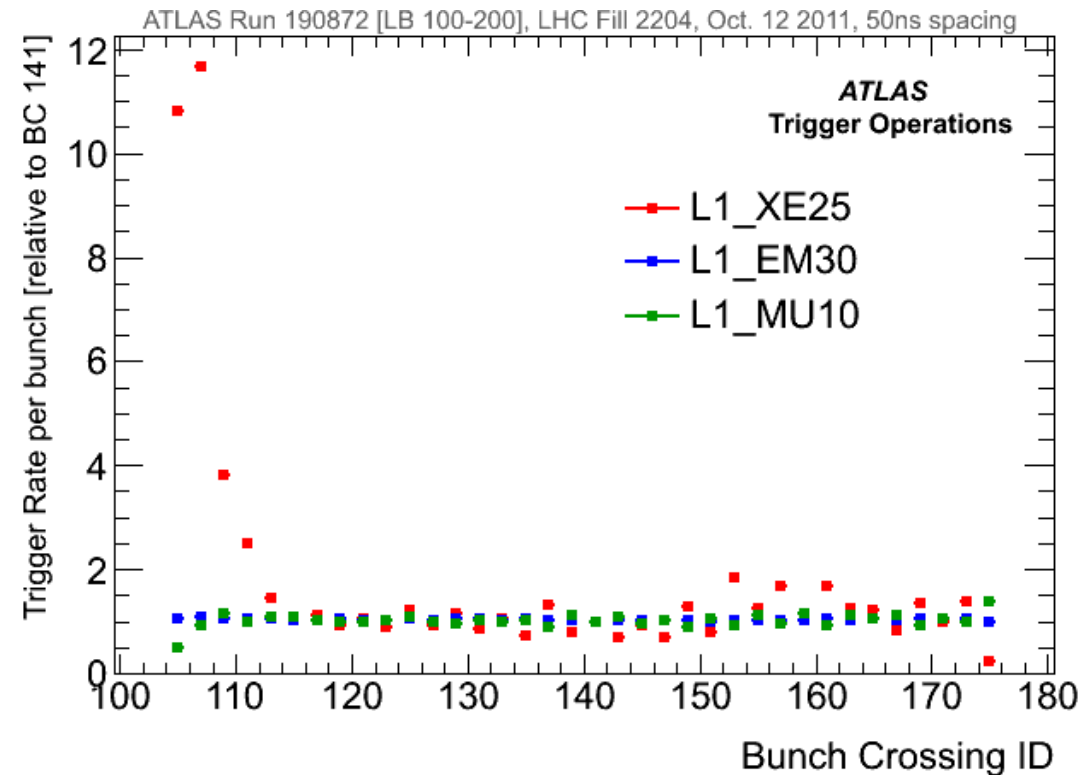
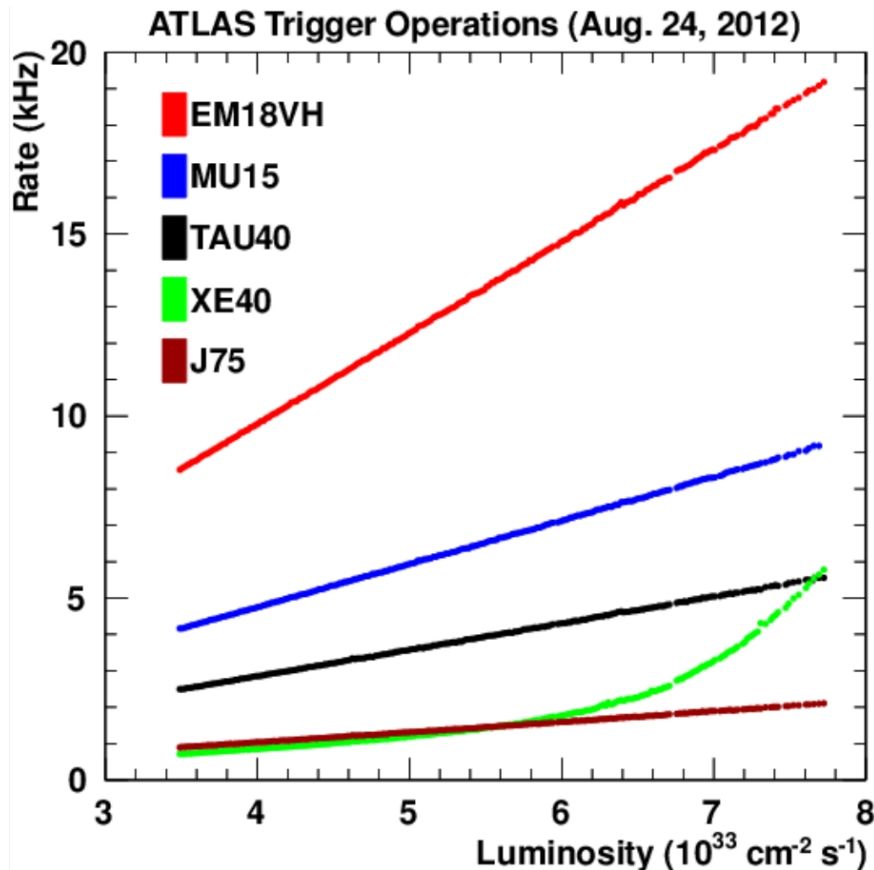
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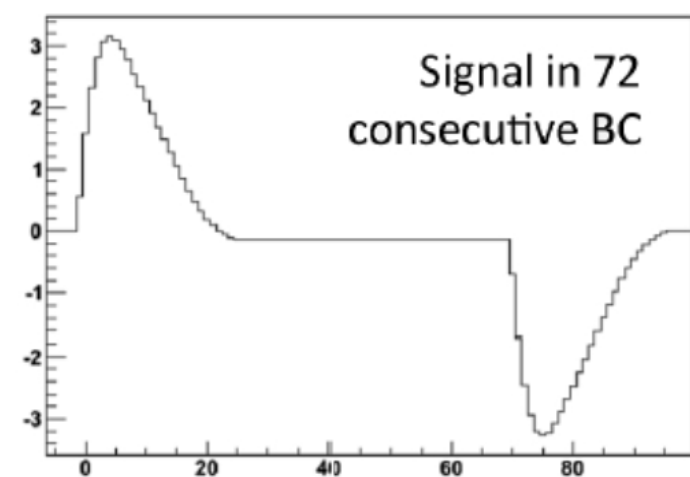
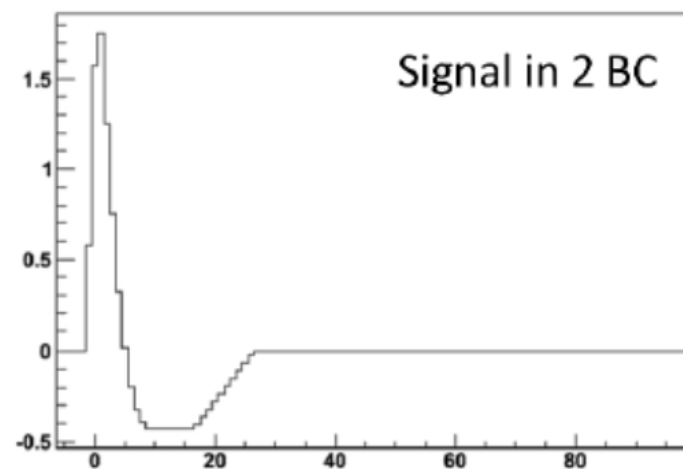
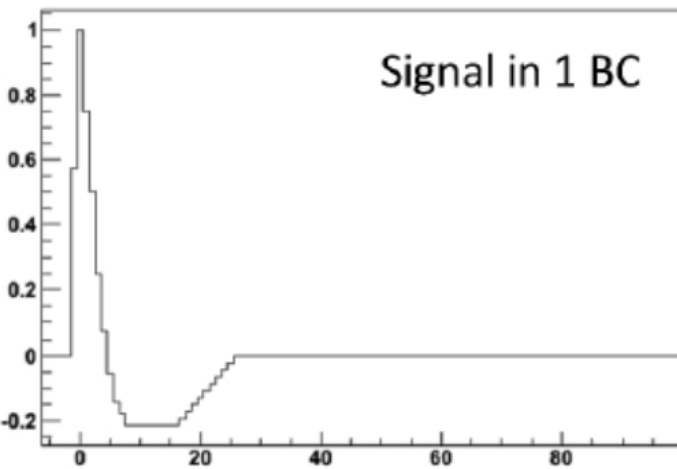
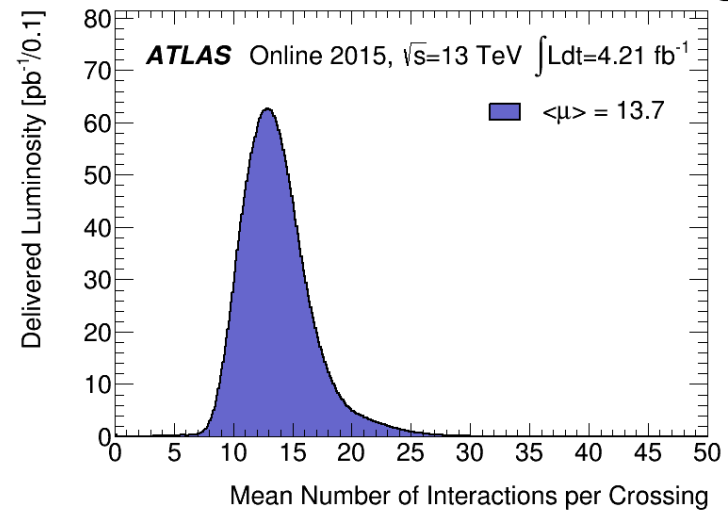
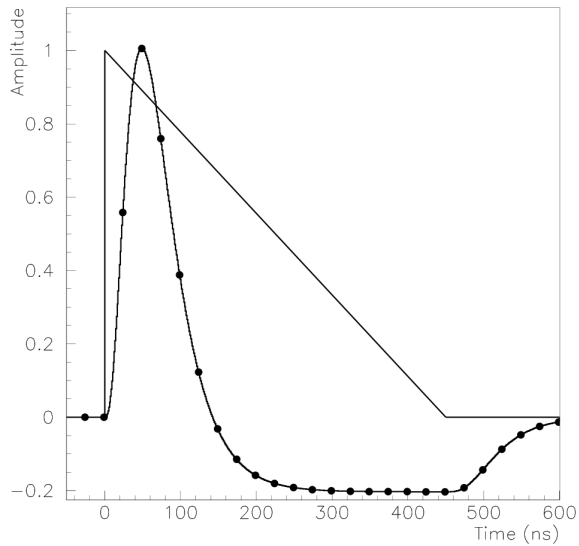
# -New Run-2 Features- Non-Linear Trigger Rates in Run-1

Trigger rates scale linearly with luminosity (  $N = L \times \sigma$  )

- In Run-1, multi-object triggers and Etmis clearly non-linear
- Run-2 luminosity is higher -> unphysical events fill bandwidth



# -New Run-2 Features- Pedestal Fluctuations



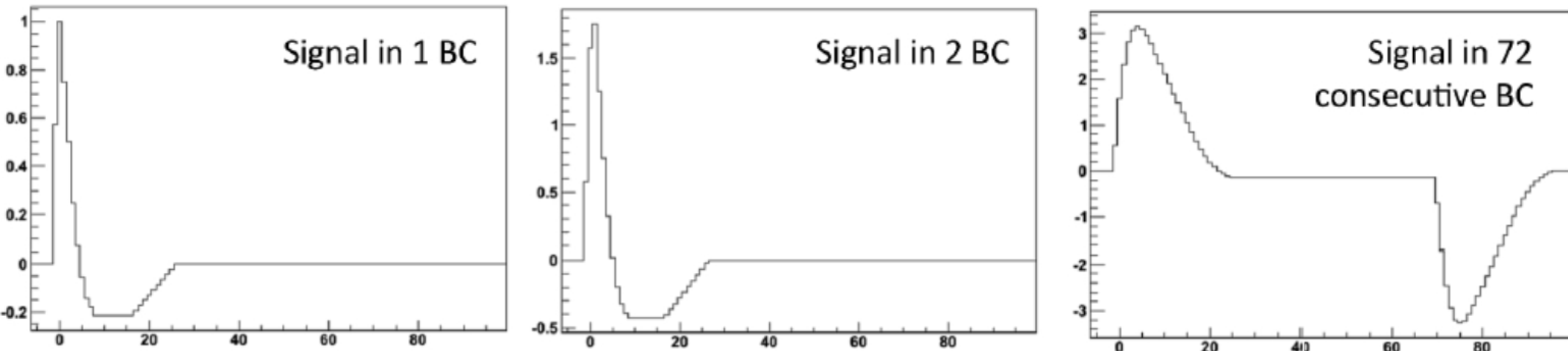
# -New Run-2 Features- Pedestal Fluctuations

Baseline increase **at beginning of each bunch-train**

- Effect **in all L1Calo input channels** at same time
- > Triggers which sum many channels strongly affected

Correct for this effect by **correcting the baseline**

- Independently **for each channel**
- Independently **for each BCID** (position along LHC orbit)





# -New Run-2 Features- Pedestal Correction

## Static vs Dynamic implementation

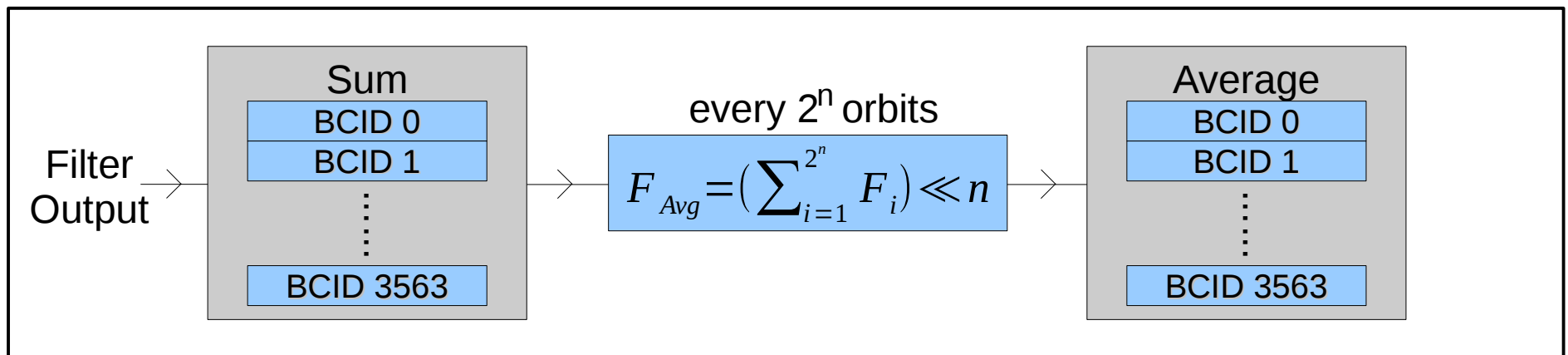
- **Static**: Load 3564 defined values during configuration
  - Change in LHC setup requires update
  - Luminosity falls during data-taking runs, affecting baseline shift
- **Dynamic**: Calculate values on-the-fly during the run
  - More complicated and resource intensive FW implementation

## Dynamic solution preferred due to ease of operation & flexibility

- Update frequently enough to follow luminosity trend
- Ability to recover from 'bad states' (e.g. bad calo signals)
- Stability of output under stable operating conditions

# -New Run-2 Features- Dynamic Pedestal Correction

- Calculate **average** of filter values **per BCID** for each channel
  - Each LHC orbit add one value to each BCIDs sum
  - Repeat for configured number of orbits ( $2^n$ , n configured)
  - Calculate averages by dividing sum by number of orbits ( $\gg n$ )



- Correct to configurable pedestal value by subtraction

$$F_{corr} = F - (F_{Avg} - Ped_{Cfg})$$

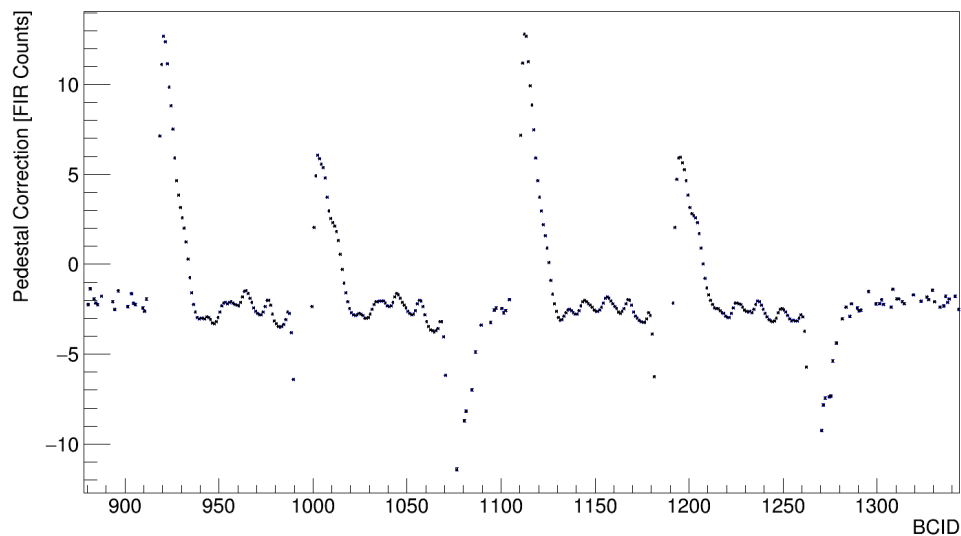
# -New Run-2 Features- Pedestal Correction Performance

Correction values are read out during operation for monitoring

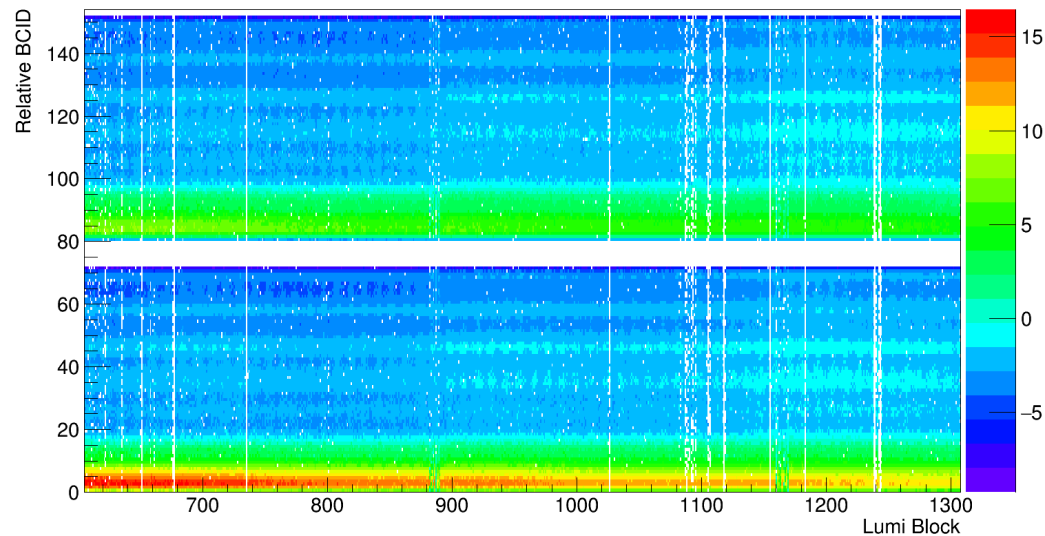
- To ensure operational stability
- Also allows study of performance



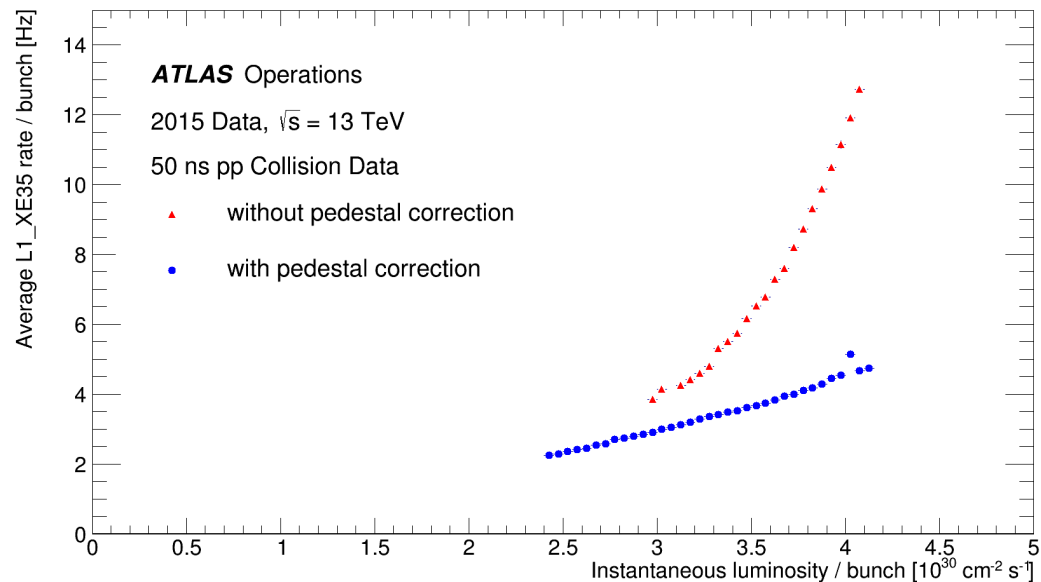
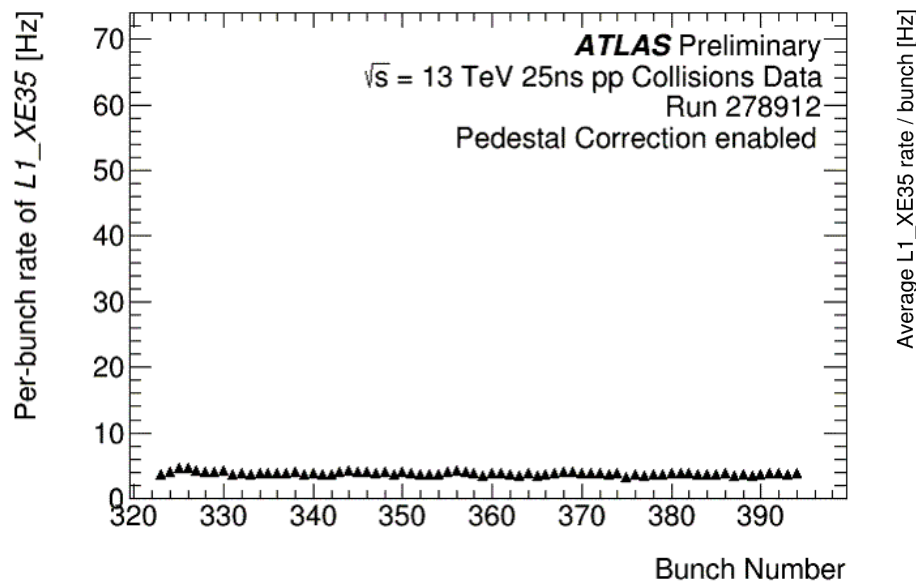
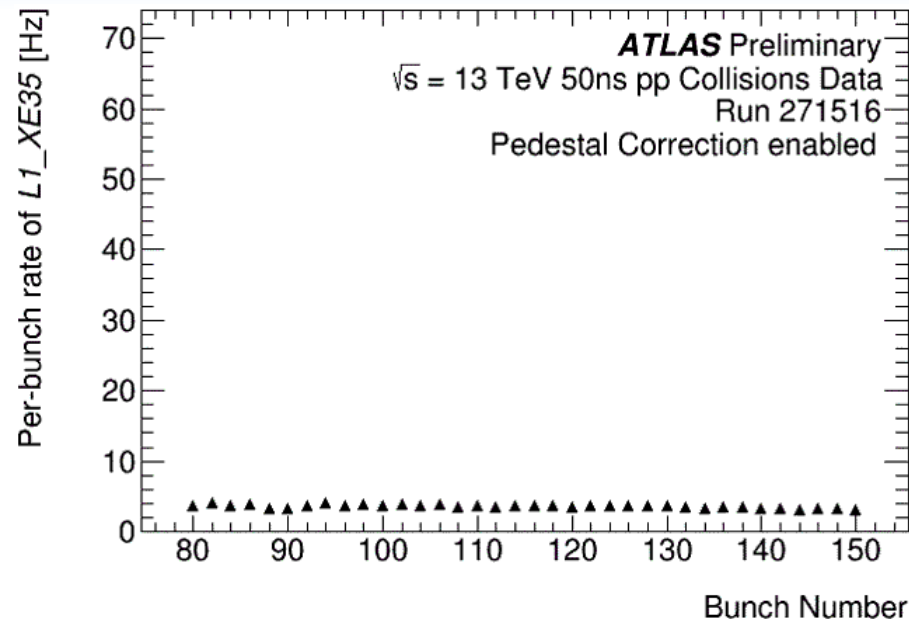
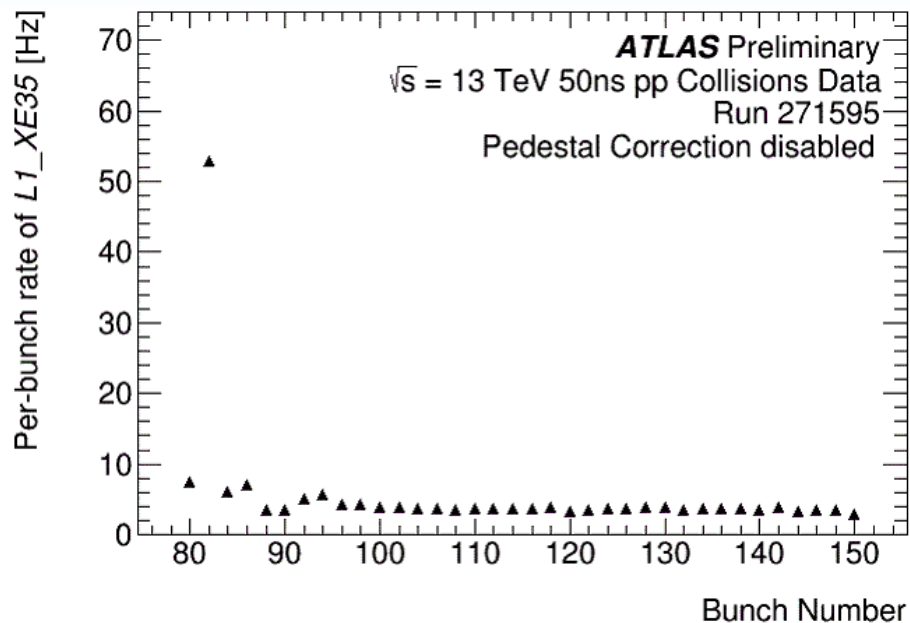
Run:279598, PedestalCorrection Vs BCN for partition LArEMBA



Run:279598, PedestalCorrection Vs BCN Vs LumiBlock for partition LArEMBA



# -New Run-2 Features- Pedestal Correction Performance



# -Summary-

- LHC Run-2 provides higher energy and luminosity
  - > More potential for physics, harsher environment for detector
- L1Calo Preprocessor upgraded to improve performance
  - Better digitisation performance from modern ADC
  - More possibilities in signal processing from modern FPGA
- Dynamic Pedestal Correction for pile-up induced fluctuations
  - Calculates on-the-fly correction for each channel, for each BC
  - Large reduction in fake E<sub>miss</sub> rates
  - Solid performance over many months of running in 2015