VMM3 L0 Data Acquisition Logic

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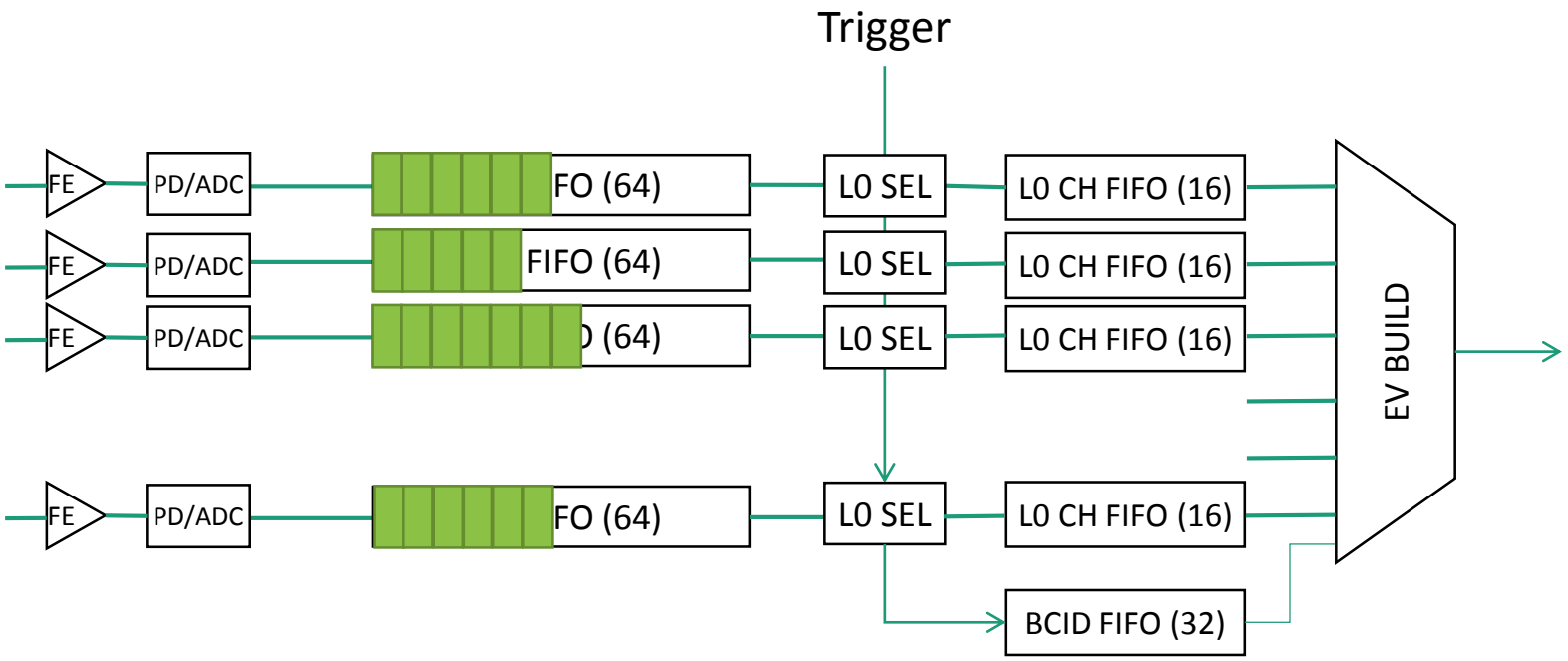
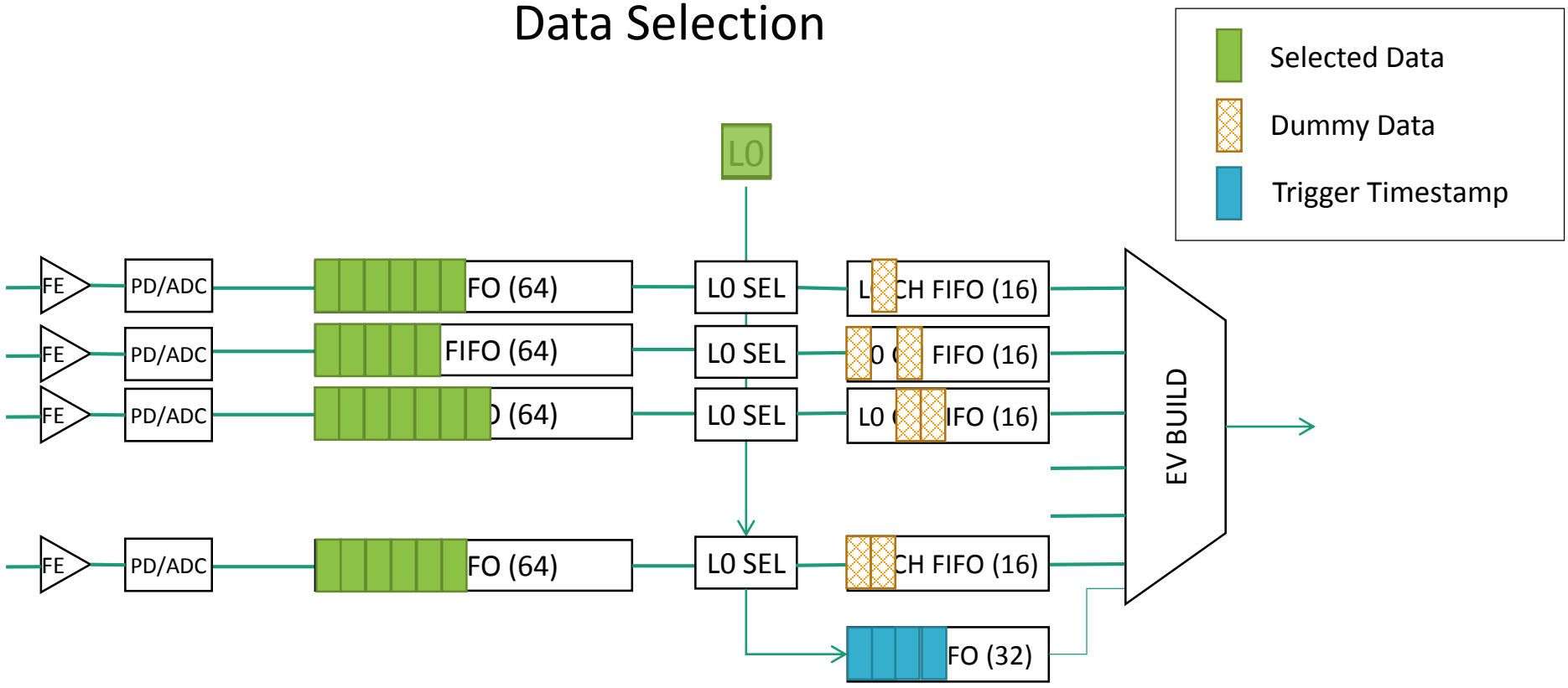
Operation of the L0 Data Acquisition Logic. Overview



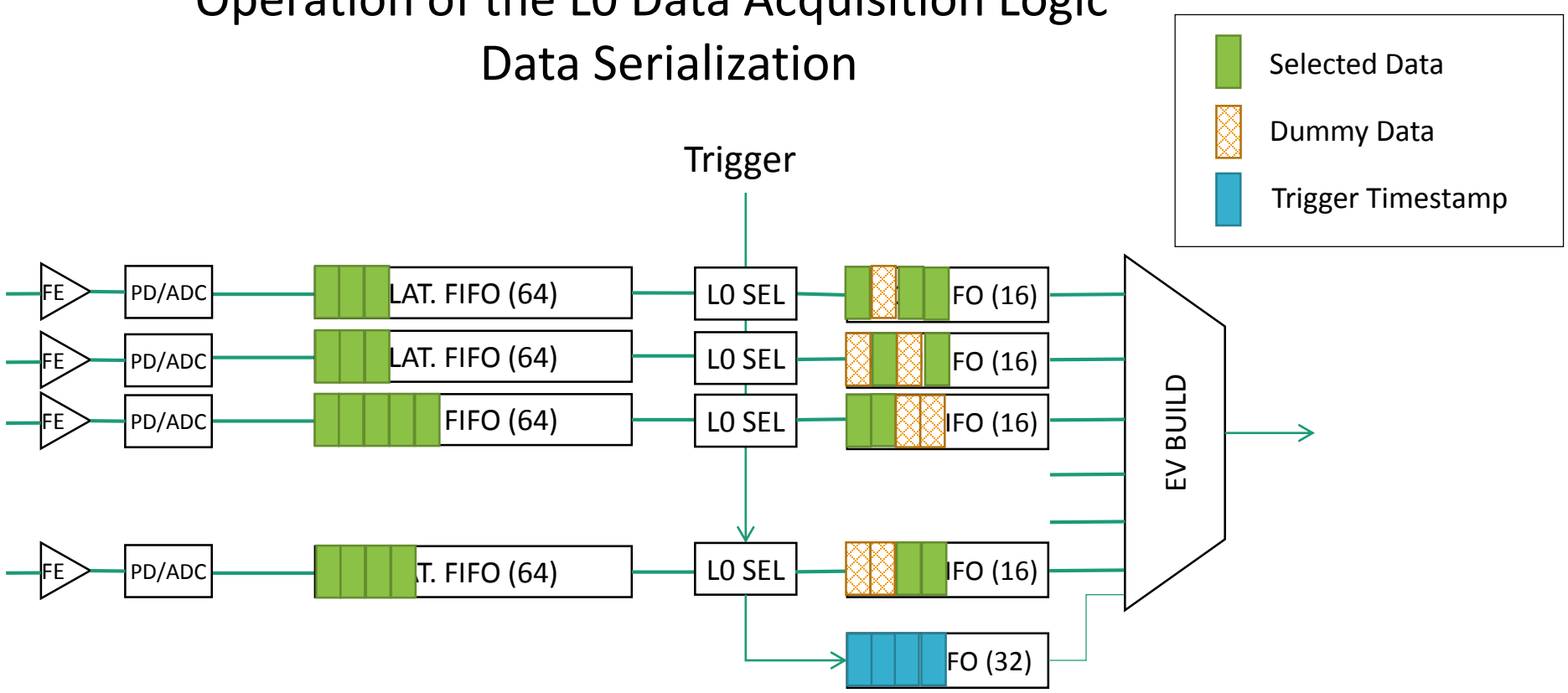
- 64-deep raw data FIFO
  - The effective latency accepted scales with the incoming hit rate
  - For max hit rate 4MHz/channel* max latency is 12.8us
- Online (25ns) data selection circuit for each channel
- 16-deep Selected Data FIFOs to allow time to serialize data to output
- 32-deep Trigger Timestamp FIFO stores the timestamp of each incoming trigger and is transmitted in the output format

Operation of the L0 Data Acquisition Logic
Data Selection



- For each incoming trigger pulse (25ns) the data in the raw FIFO is selected based on the timestamp included in raw data
  - A configurable acceptance window of 1..8 x 25ns can be used
  - If two consecutive triggers have their windows overlap, data is copied to both triggers
- In the Selected Data FIFO, dummy data is written for channels which does not have data in the trigger window. Dummy data is not readout.

Operation of the L0 Data Acquisition Logic
Data Serialization



- The Event Builder builds packets for each trigger and serializes the data to the output
- Each packet contains:
  - the Trigger Timestamp
  - Hit Data for each channel which has a hit in the trigger window (dummy data is discarded)
  - Hit Data includes differential timestamp relative to the Trigger Timestamps