Universidade de São Paulo

USP

ALICE

SAMPA Chip:
a new ASIC for the ALICE TPC and MCH Upgrades

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on behalf of the ALICE-SAMPA group

RD51 Collaboration Meeting, WG5 Session: 9.3.2016

Outlines

- Motivation
- SAMPA ASICS for ALICE TPC and MCH readout upgrade
    - Overview of the full chip
- Analog front-end
    - Architecture
    - Simulations & Measurement results
        - Pulse shape & Peaking time
        - Gain value and linearity
        - Noise & PSRR
        - “on the field”: reading a GEM detector
- 10 bit SAR ADC
    - Simulation & Measurement results

ALICE Upgrade Strategy

- Operate ALICE at high rate, record all MB events
  - Goal: 50kHz in Pb-Pb (~$10nb^{-1}$ in Run3 and Run4)
- Upgrade detectors and electronics during Long Shutdown 2 (2020)
  - GEM TPC with continuous readout
    - High rate capability, preserve PID and tracking performance
  - Muon Chamber (Forward muon spectrometer)
    - High rate capability, new electronics needed (same as TPC?)

TPC requires a new readout, MCH too.

A common project to design a new ASIC: SAMPA

SAMPA design specifications

- TSMC CMOS 130 nm, 1.25V technology
- 32 channels, Front-end + ADC + DSP
- package size ≤15x15mm^2 (total footprint)
- negative input charge (reading GEM, ALICE "TPC")
  - Sensor capacitance 12 – 35 pF
  - Sensitivity 20mV/fC & 30mV/fC
  - Noise: ENC ≤ 480 e^- @ 18.5pF
  - Pulse Shape: ~160 ns, tail to baseline in less than 290 ns

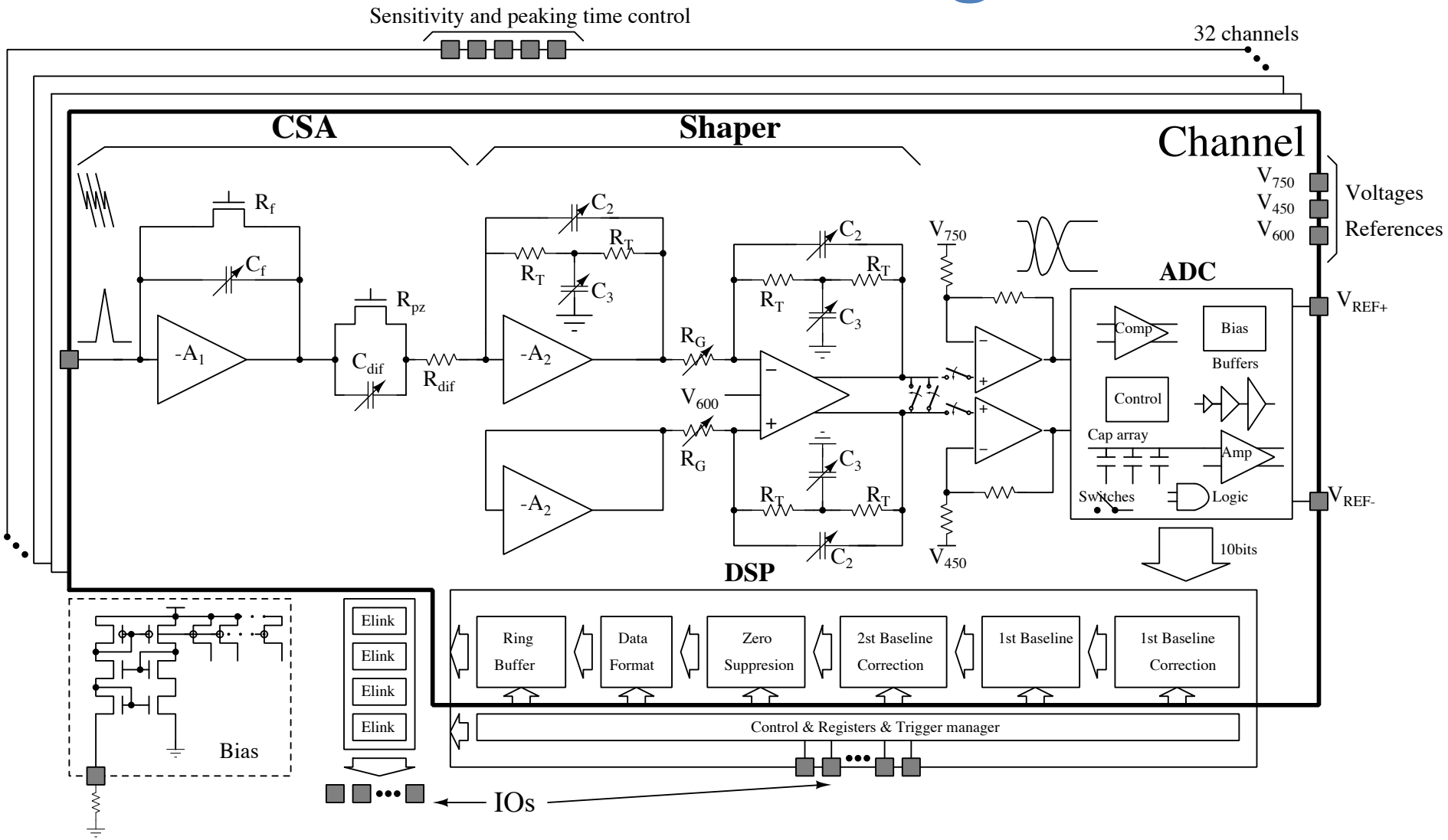
TPC Mode

- positive input charge (reading MPWC, ALICE "MCH")
  - Sensor capacitance 40–80 pF
  - Sensitivity 4mV/fC
  - Noise: ENC ≤ 950 e^- @ 40pF (1600 e^- @80pF)
  - Pulse Shape: ~300 ns, tail to baseline in less than 550 ns

MCH Mode

- Crosstalk < 0.2%
- ADC: 10-bit resolution, 10MS/s
- DSP functions: pedestal removal, baseline shift corrections, zero-suppression, …
- Data transmission: ≥ 4 e-link at 320 Mbps to GBT, SLVS I/O
- Power < 32 mW/channel (FrontEnd + ADC)

SAMPA Block Diagram



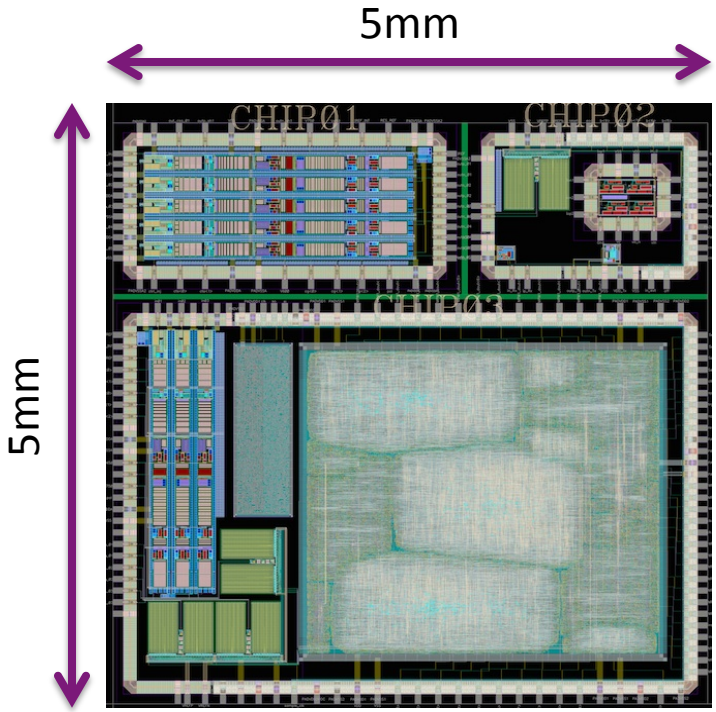
First prototype produced at the end 2014

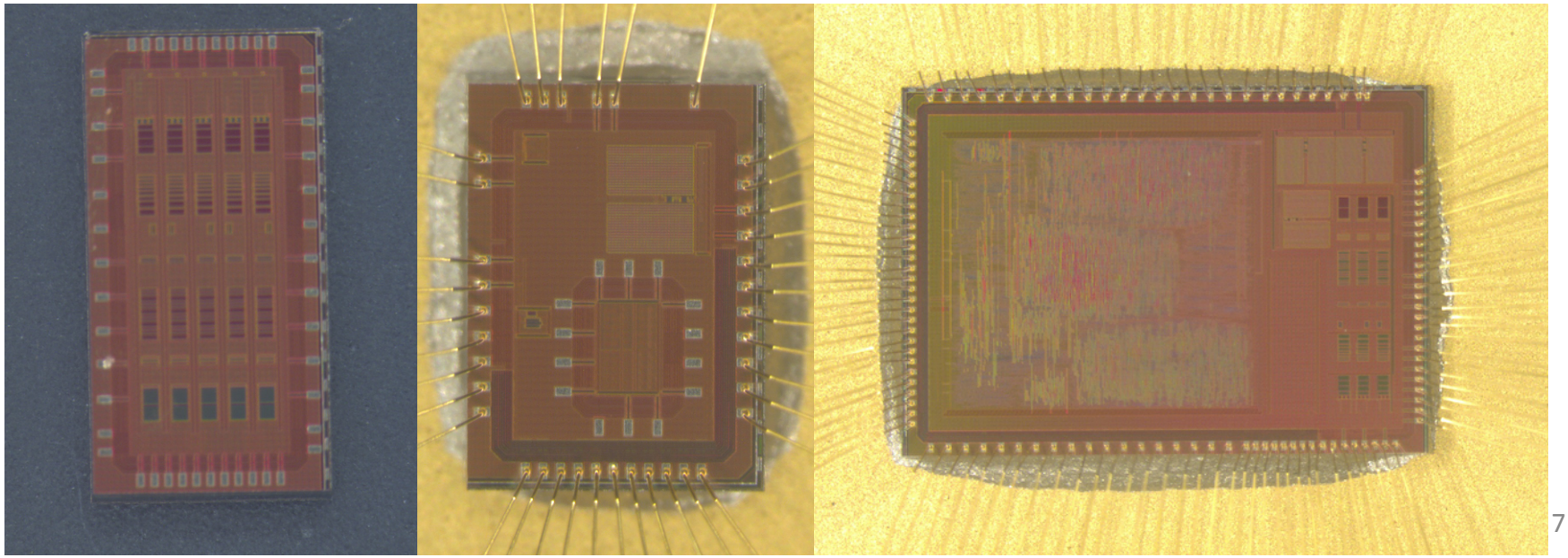
Testing building block

MPW1: 1 sample, 3 chips

MPW1: sample split in three chips

- Chip1: analog (CSA + shapers), 5 chs
- Chip2: ADC (1 ch) + LVDS Receiver and Transmitter prototypes
- Chip3: full chain (CSA-Shaper-ADC-DSP), 3chs





Second prototype being fabricated now

(presently we are in the tape-out phase)

Full size prototype (FE+ADC+DSP, 32 channels)

11 SLVS output links @ 320 Mbps

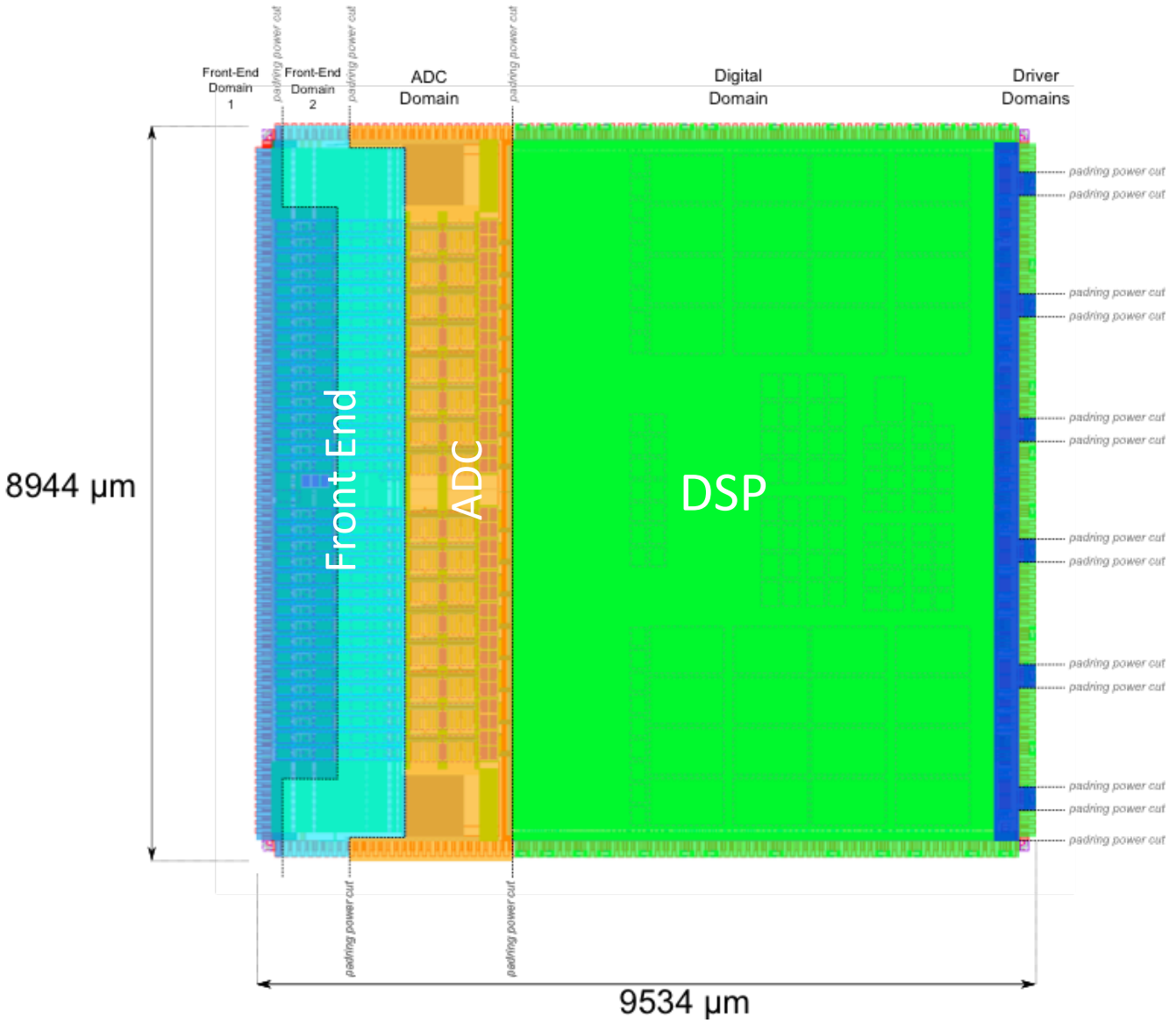
Die Size: 9575 x 8985 μm^2 (without scribes)

Engineering run (cheaper!): 10 wafers, >1500 pieces

Packaging: BGA (custom 15x15 mm^2, 372 balls), 1000 chips (MOC)

Full (FE-ADC-DSP) 32 channels prototype

32 input channels



Output via up to 11 SLVS links

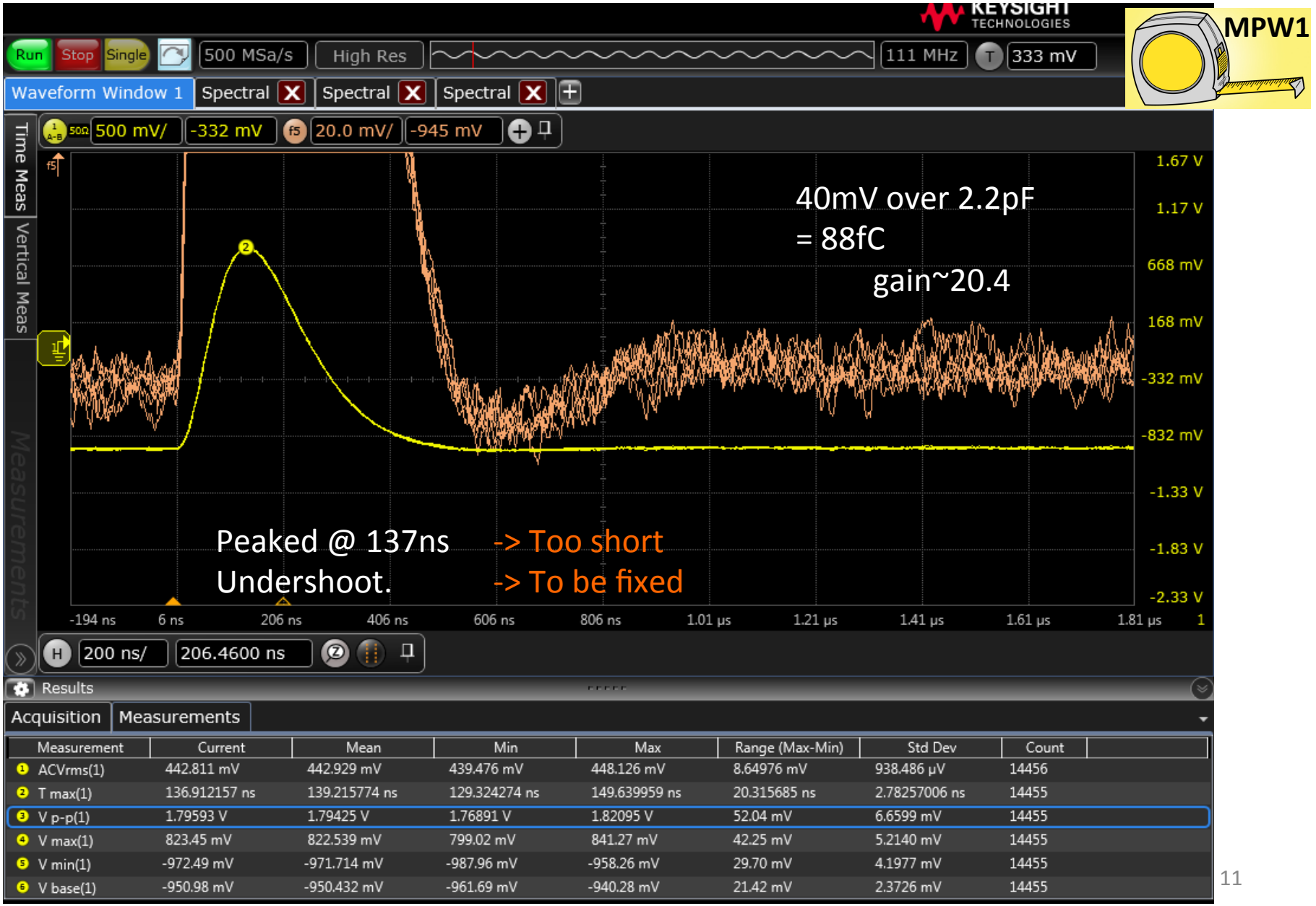
SAMPA Performance

MPW1 test blocks measurement results

&

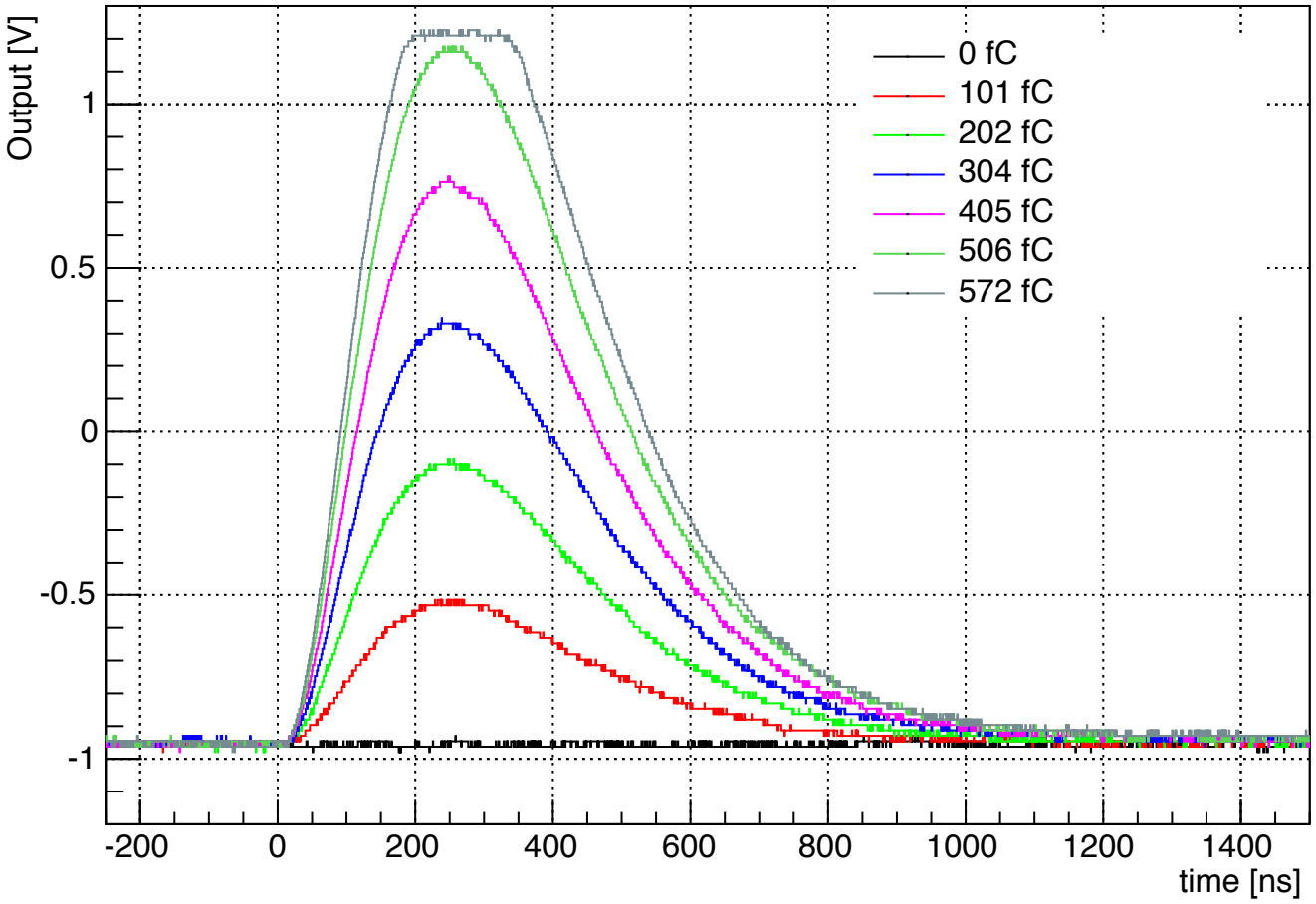
Simulation for MPW2 full prototype

Pulse shape [20mV/fC, 160 ns, Neg]

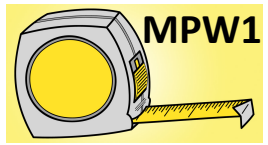


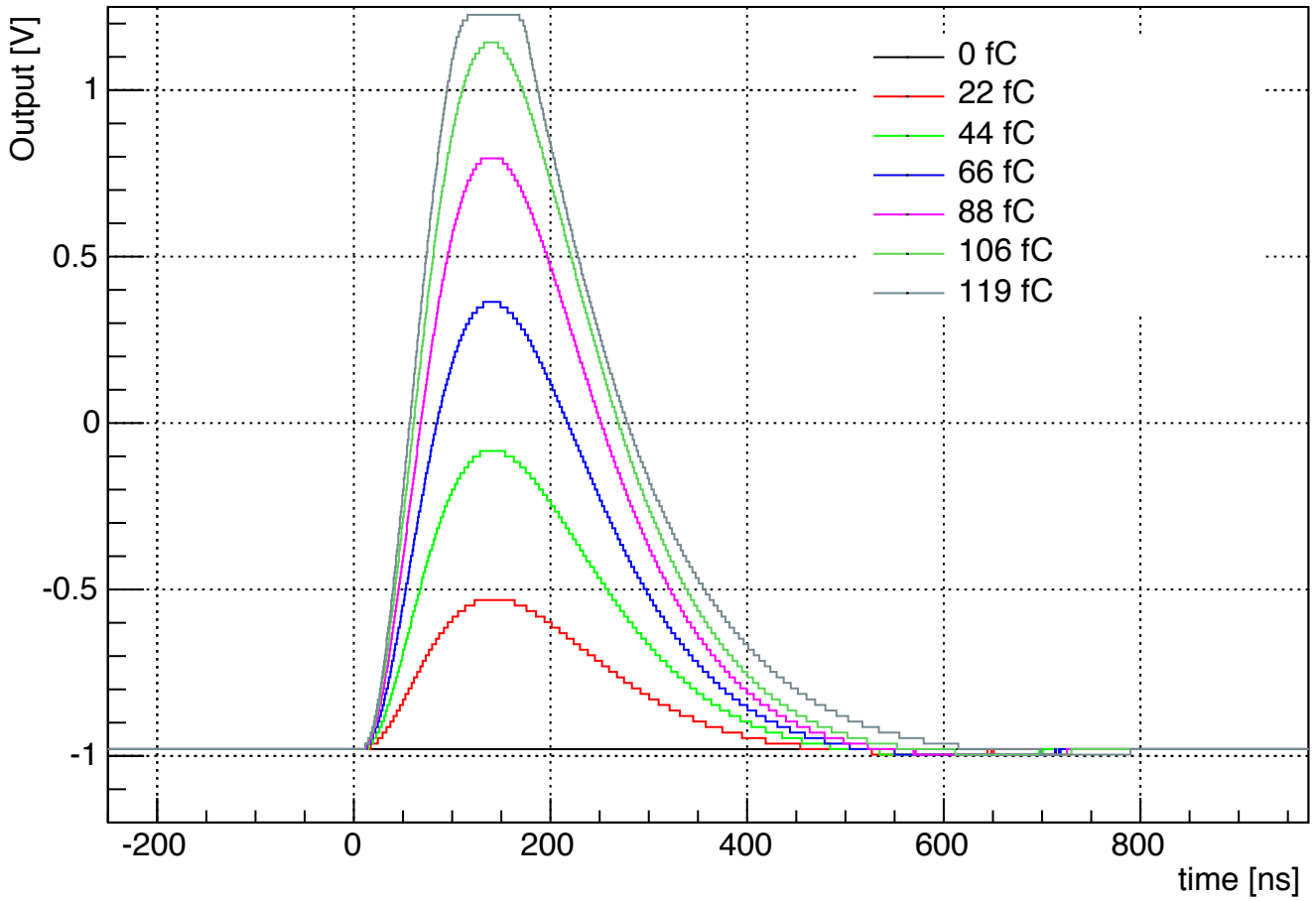
Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
ACVrms(1)	442.811 mV	442.929 mV	439.476 mV	448.126 mV	8.64976 mV	938.486 µV	14456
T max(1)	136.912157 ns	139.215774 ns	129.324274 ns	149.639959 ns	20.315685 ns	2.78257006 ns	14455
V p-p(1)	1.79593 V	1.79425 V	1.76891 V	1.82095 V	52.04 mV	6.6599 mV	14455
V max(1)	823.45 mV	822.539 mV	799.02 mV	841.27 mV	42.25 mV	5.2140 mV	14455
V min(1)	-972.49 mV	-971.714 mV	-987.96 mV	-958.26 mV	29.70 mV	4.1977 mV	14455
V base(1)	-950.98 mV	-950.432 mV	-961.69 mV	-940.28 mV	21.42 mV	2.3726 mV	14455

Pulse shape vs InputCharge [4mV/fC, 300 ns, Pos]

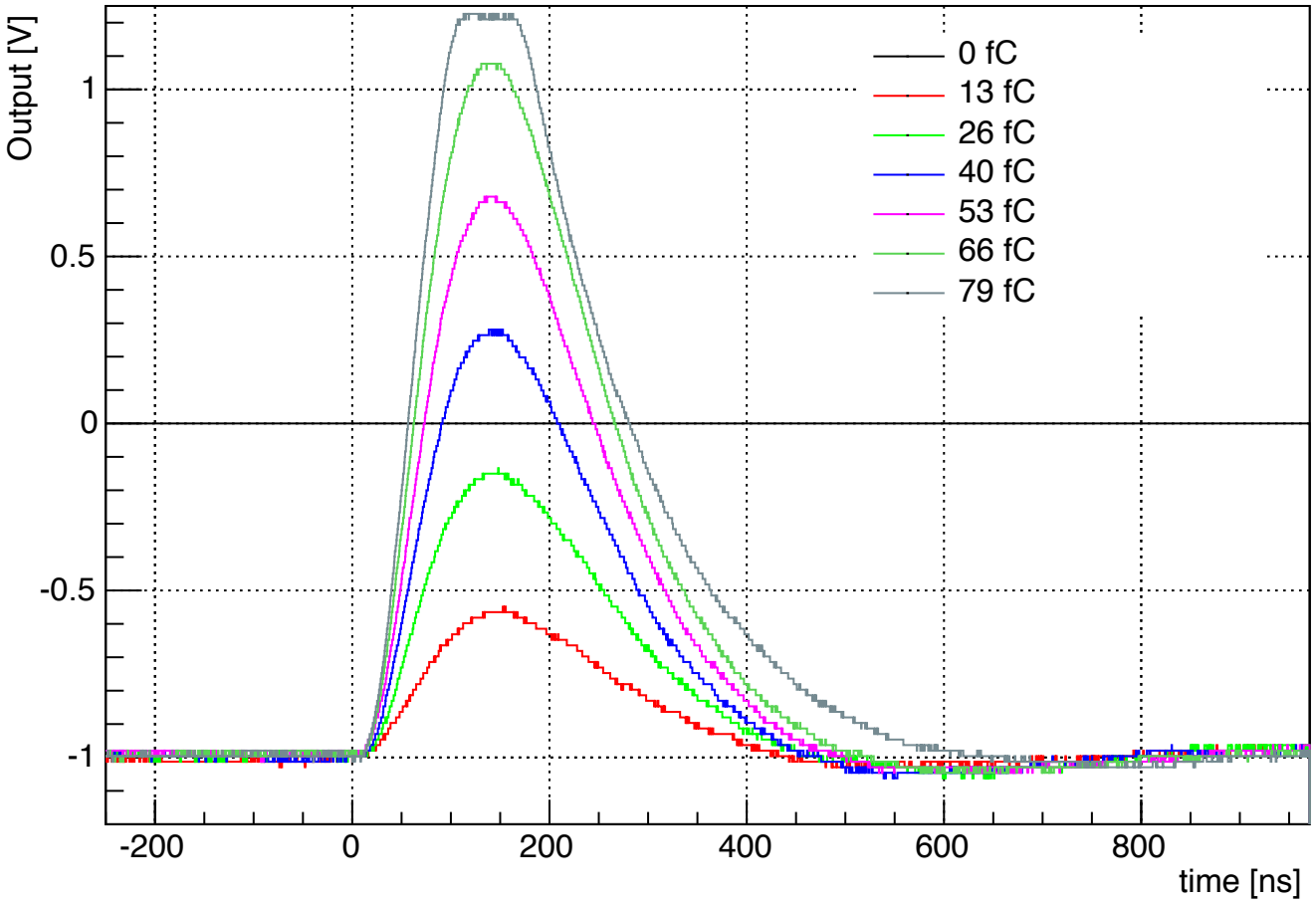


Pulse shape vs InputCharge [20mV/fC, 160 ns, Neg]

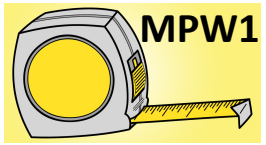




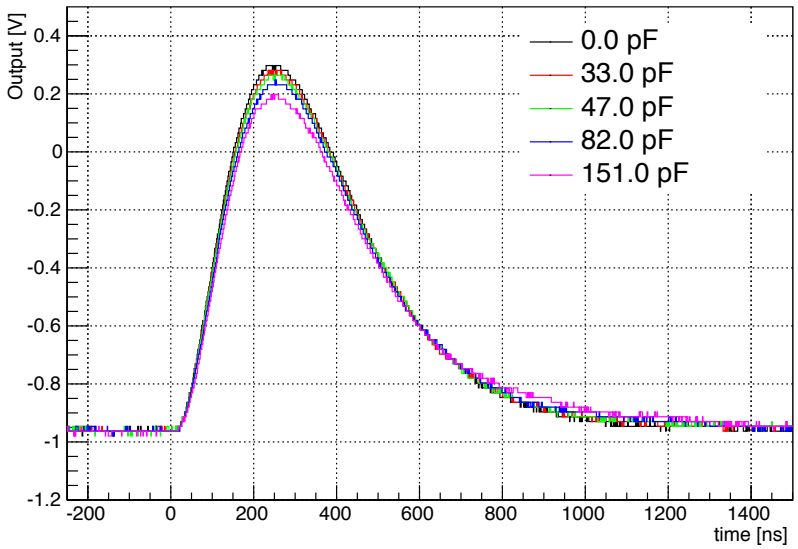
Pulse shape vs InputCharge [30mV/fC, 160 ns, Neg]



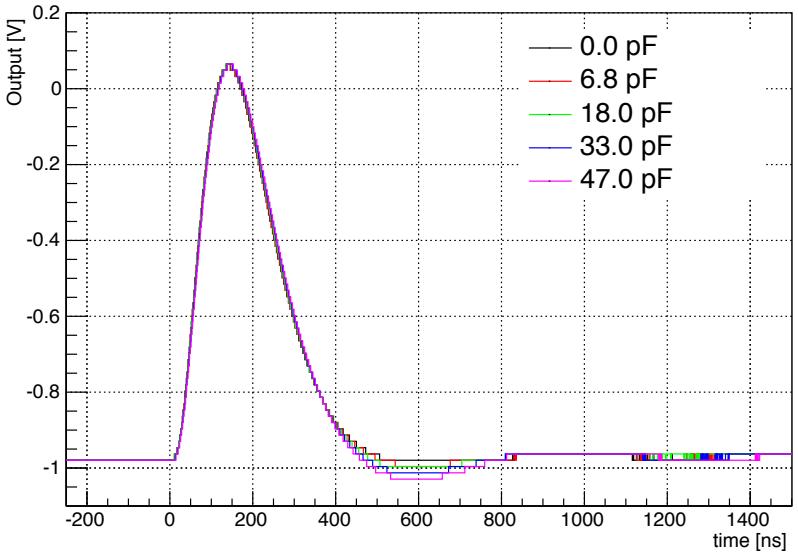
Pulse Shape vs Detector Capacitance



4mV/fC, 300 ns, POS

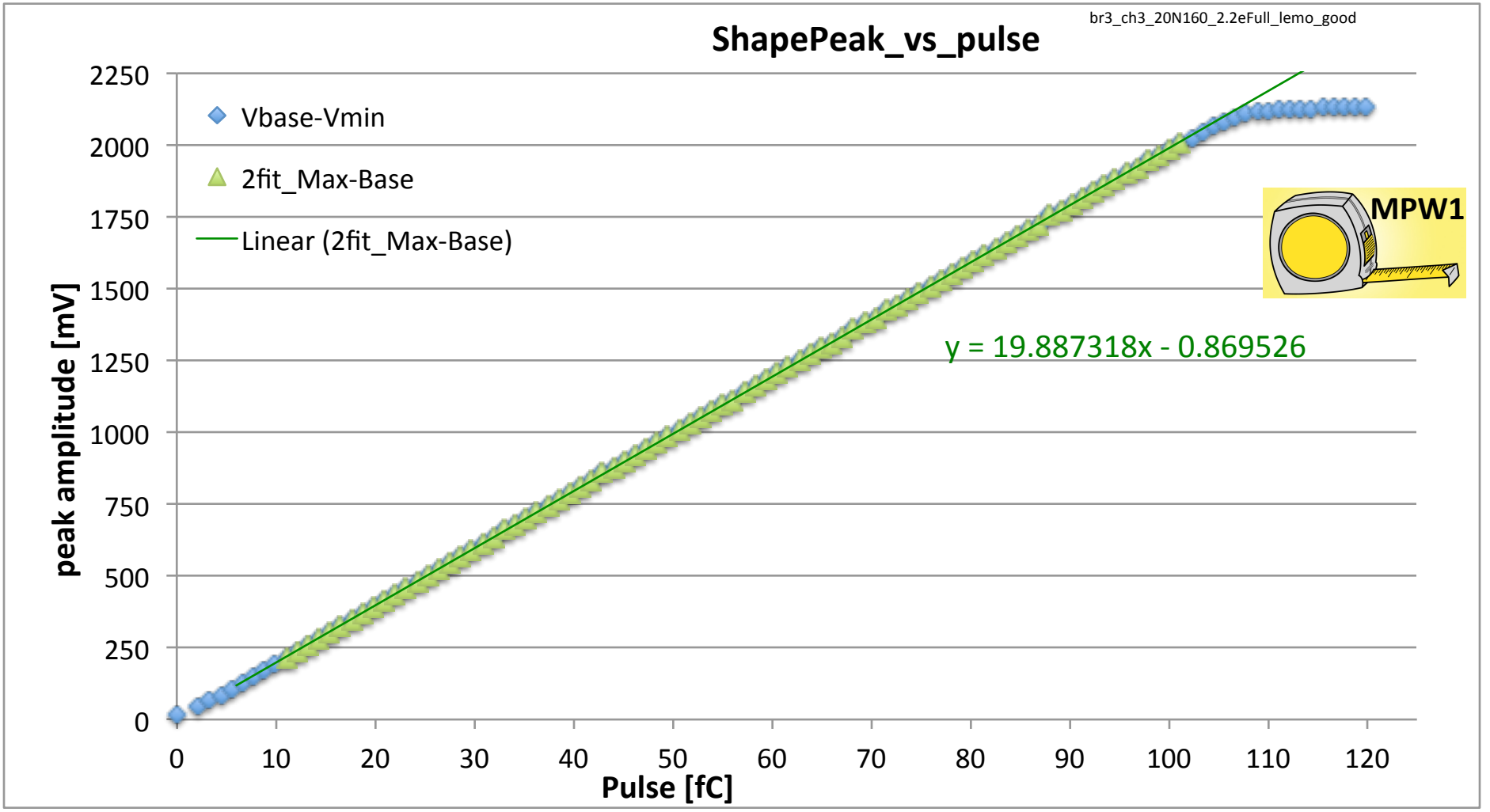


20mV/fC, 160 ns, NEG



No significant effects in the expected range of detector capacitance

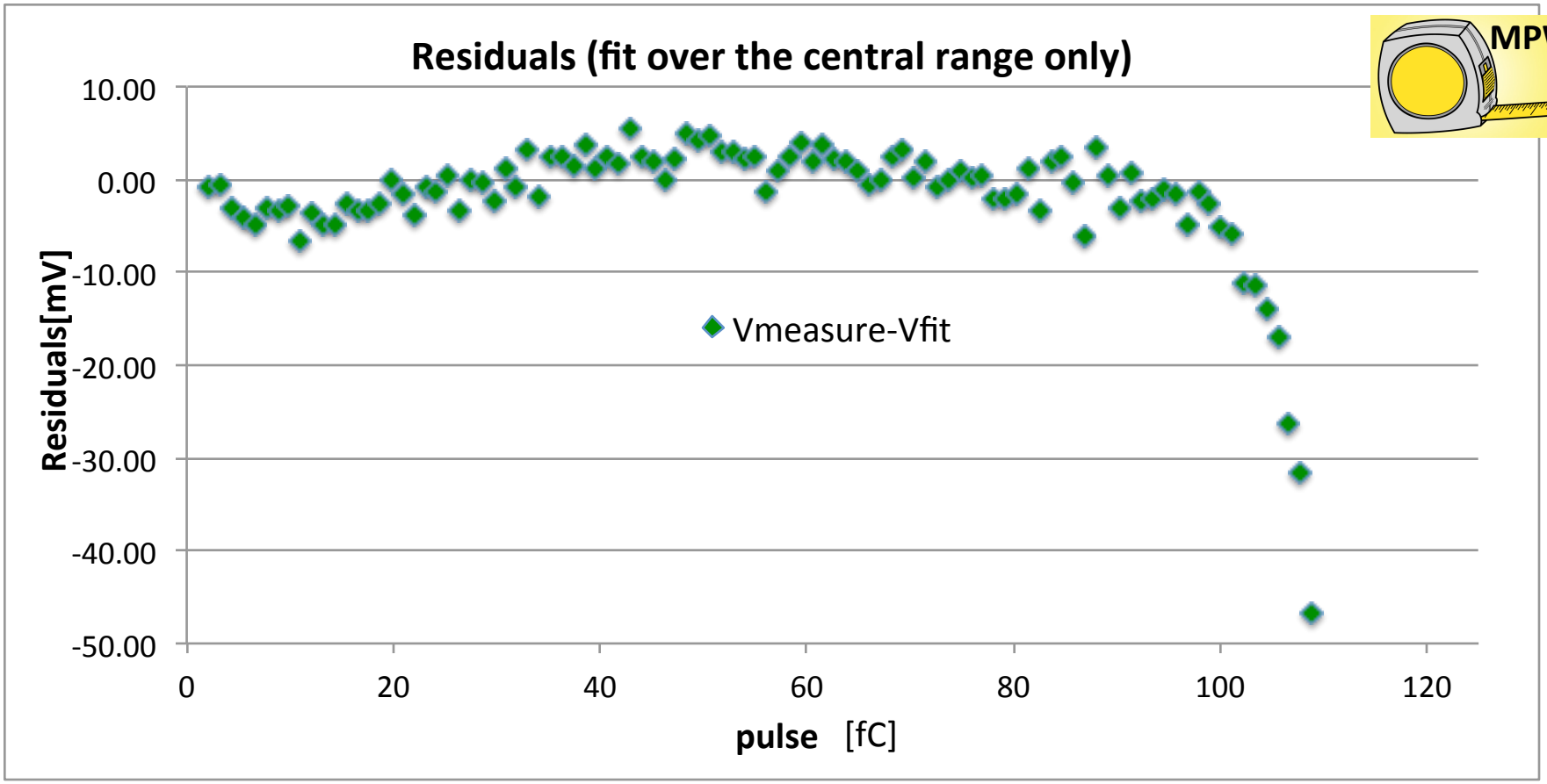
FrontEnd: Response [20mV/fC, 160 ns, Neg]



Constant slope up about 100 fC pulses

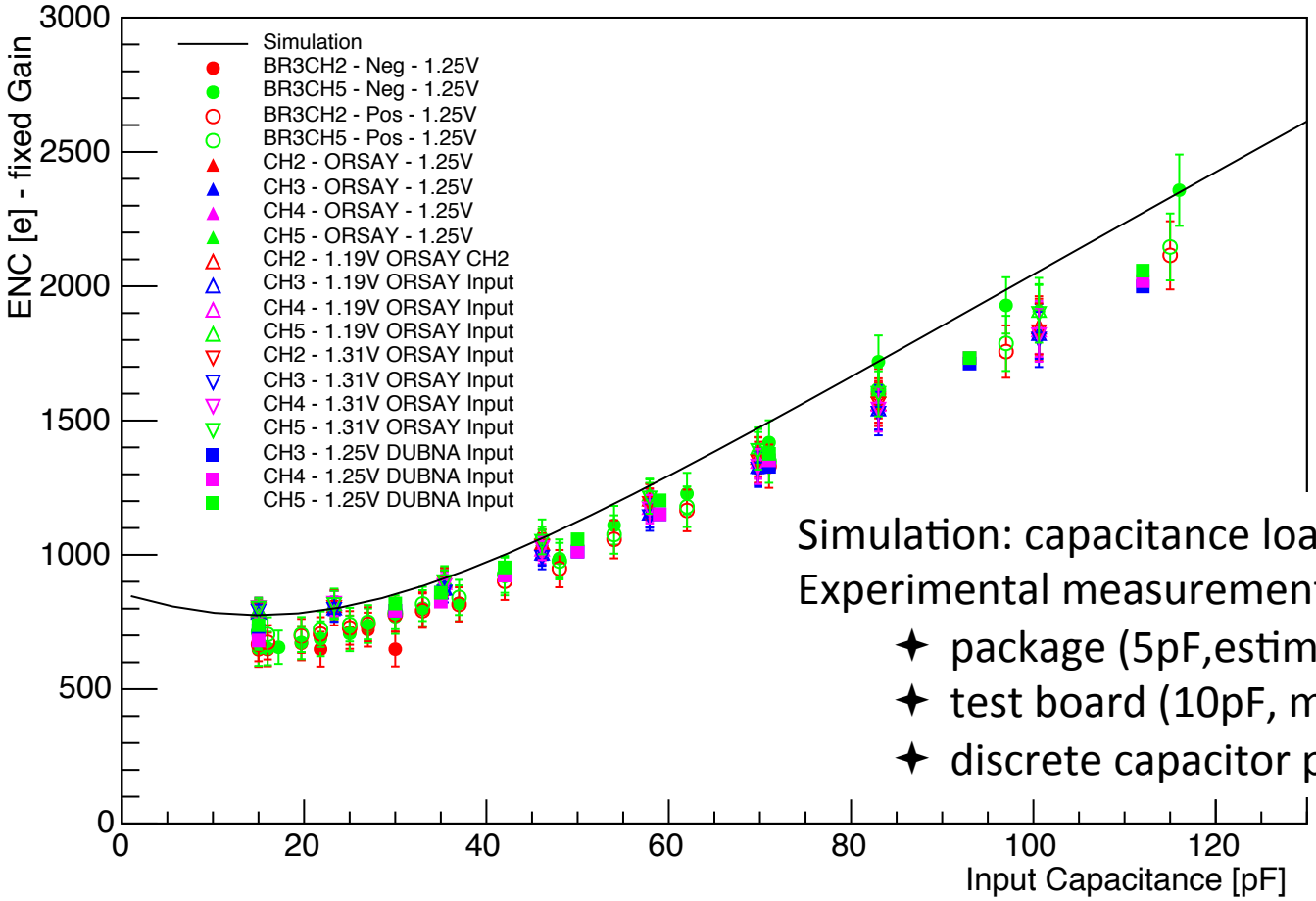
FrontEnd: Gain linearity [20mV/fC, 160 ns, Neg]

br3_ch3_20N160_2.2eFull_lemo_good



Very good (<.2%) in the 0-80-fC range.
better than 1% in the 80-100 fC range

Noise @4mV/fC 300ns



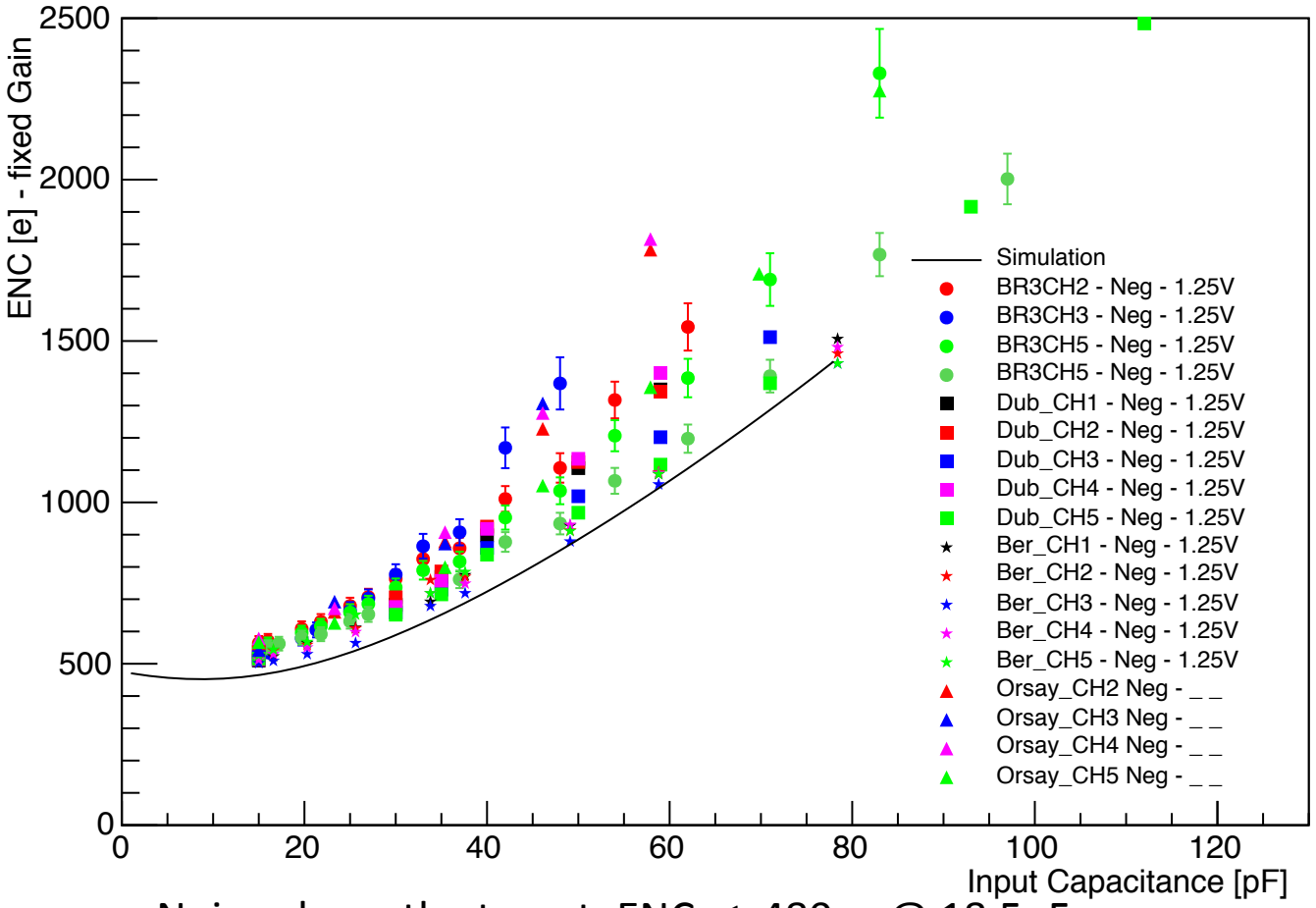
Simulation: capacitance loading the input pad (die)

Experimental measurements: total capacitance:

- ✦ package (5pF,estimated)
- ✦ test board (10pF, measured)
- ✦ discrete capacitor plugged on the board

Noise in the target: ENC ≤ 950 e^- @ 40pF (1600 e^- @80pF)

Noise @20mV/fC 160ns



Simulation: capacitance loading the input pad (die)

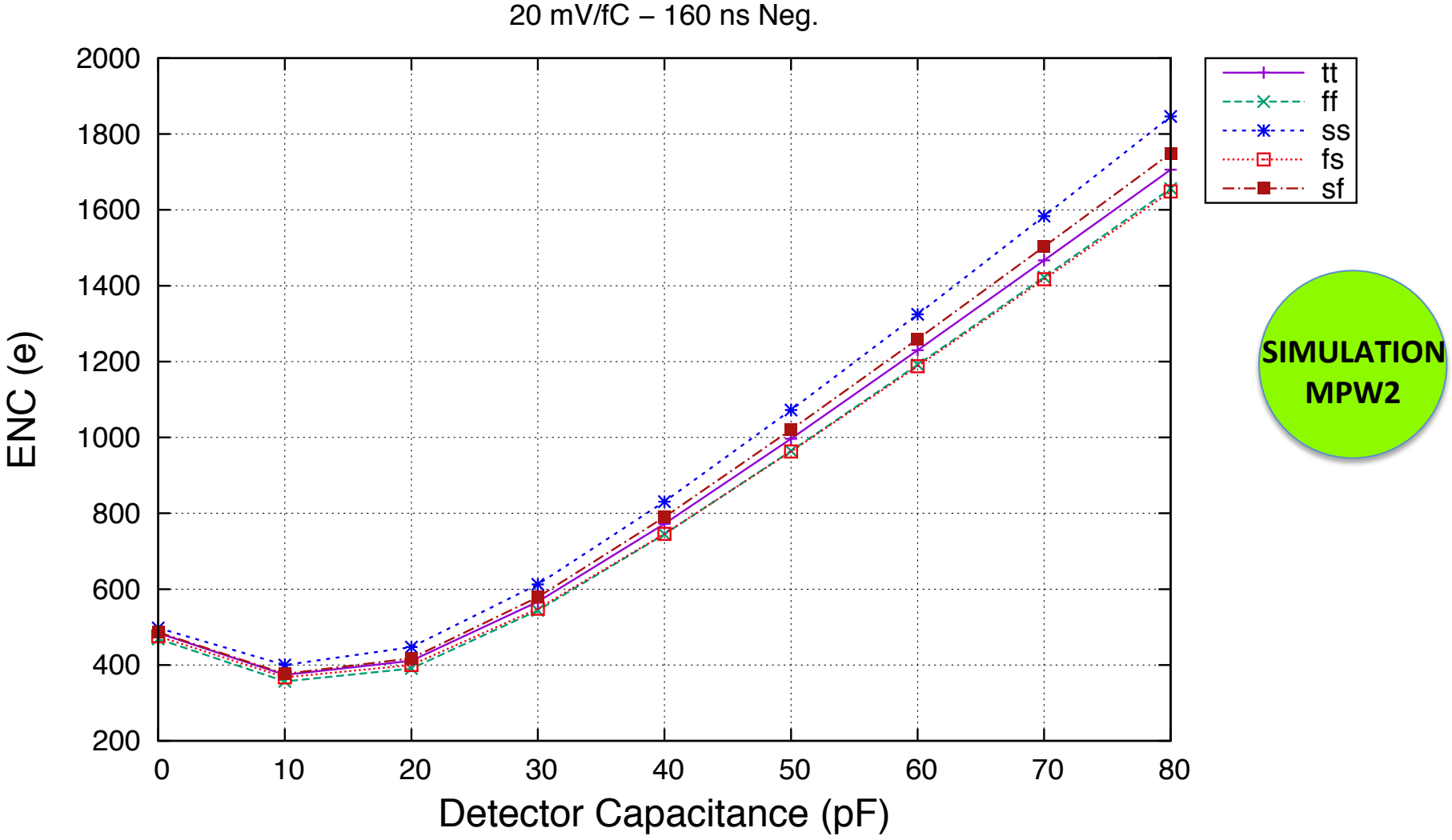
Tests: total capacitance:

- package (5pF,estimated)
- test board (10pF, measured)
- discrete capacitor plugged on the board

Noise above the target: ENC ≤ 480 e^- @ 18.5pF

Removing the unused 80ns shaping option from the circuit should permit a redistribution of the gain along the chain, allowing a significant improvement.

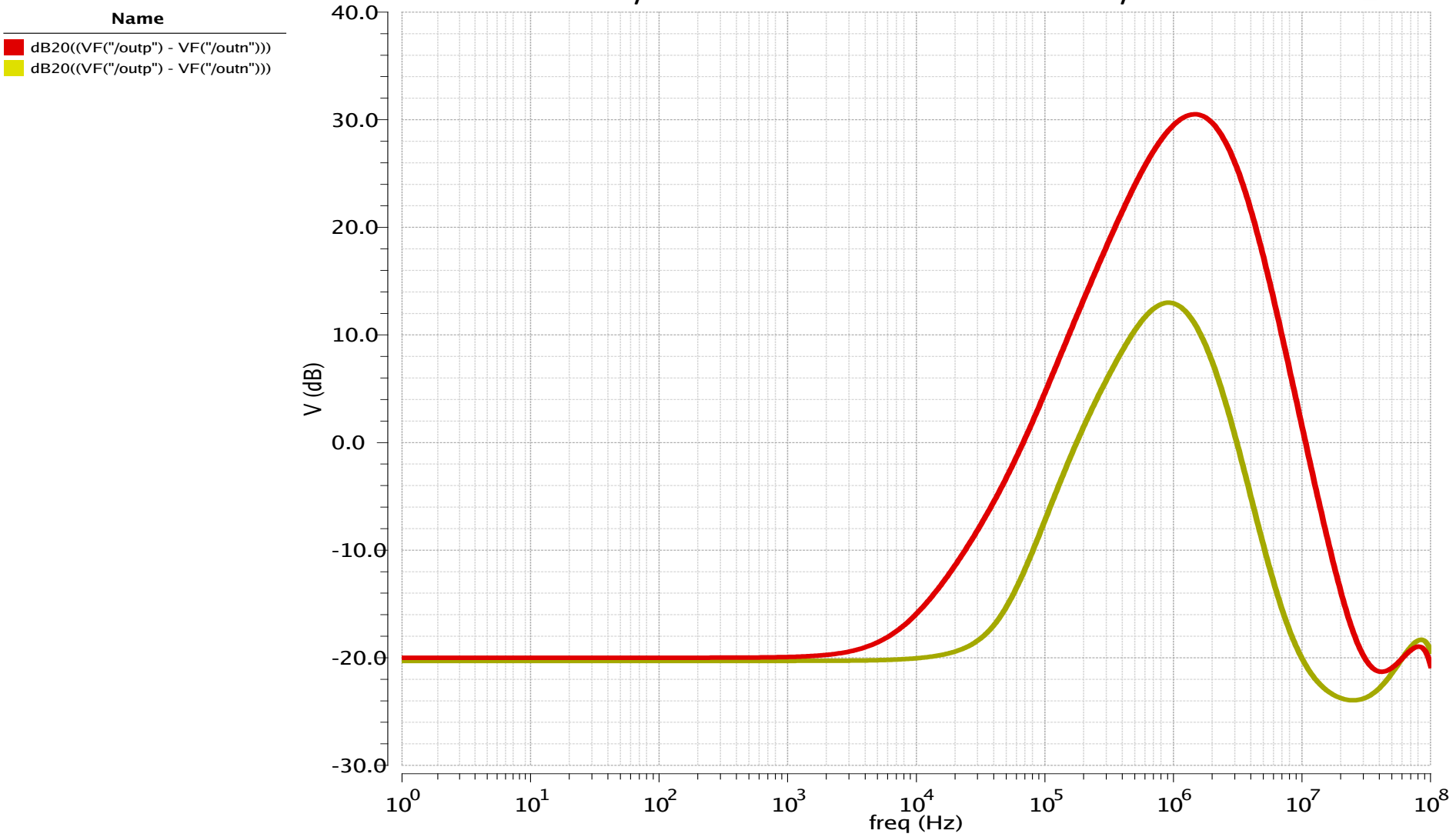
MPW2, Noise @20mV/fC 160ns



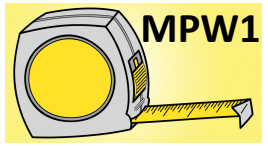
MPW1-FE: PSRR simulation

SIMULATION MPW1

RED: 160 ns 30mV/fC **GREEN**: 300ns 4mV/fC



MPW1-FE: PSRR measured



Injected a sine in the VDD, PSRR calculated as the ratio between spectral intensity (a the given frequency) of the FFT of Ch3_differential and FFT of VDD measured on pin61 of the chip

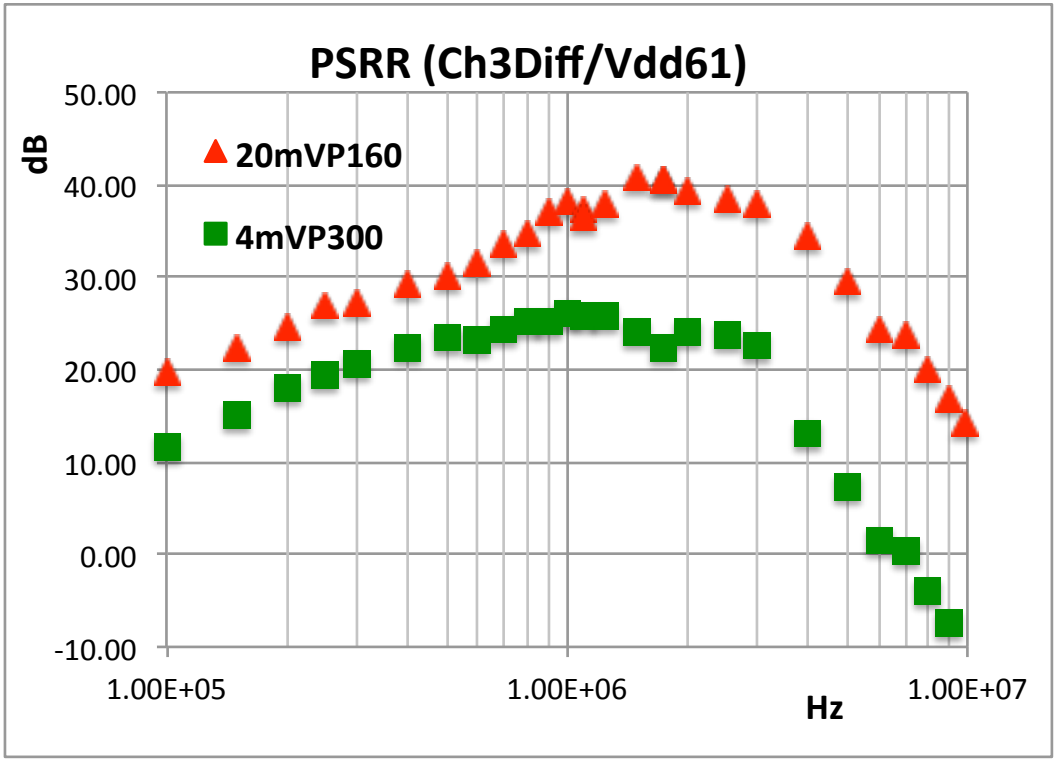
RED: 160 ns 30mV/fC **GREEN**: 300ns 4mV/fC

Shape of the PSRR reproduced.
Value even a factor 3 worse..
(but not a easy measurement..)

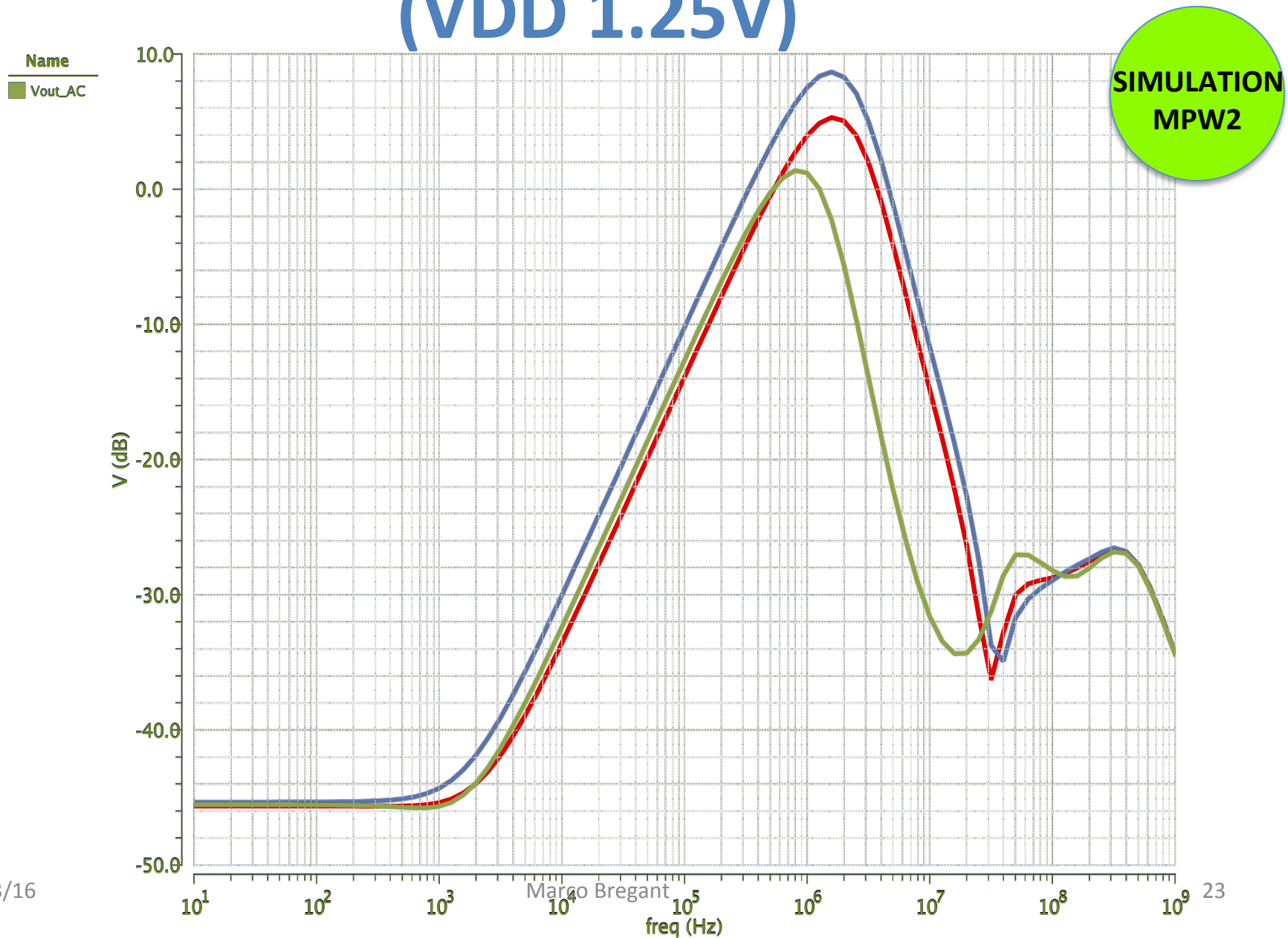
The present of a "bump" in the 50-60MHz region (corresponding to second peak on the simulation) was only visually verified performing a sweep.

Agreement Simulation/Test

PSRR improved in MPW2

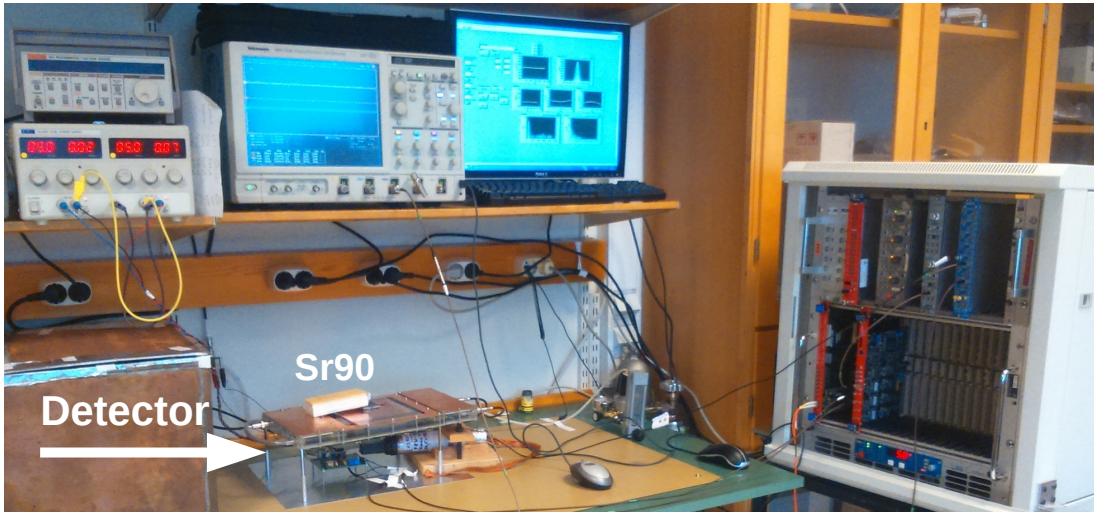


20mV/fC neg | 30mV/fC neg | 4mV/fC pos (VDD 1.25V)

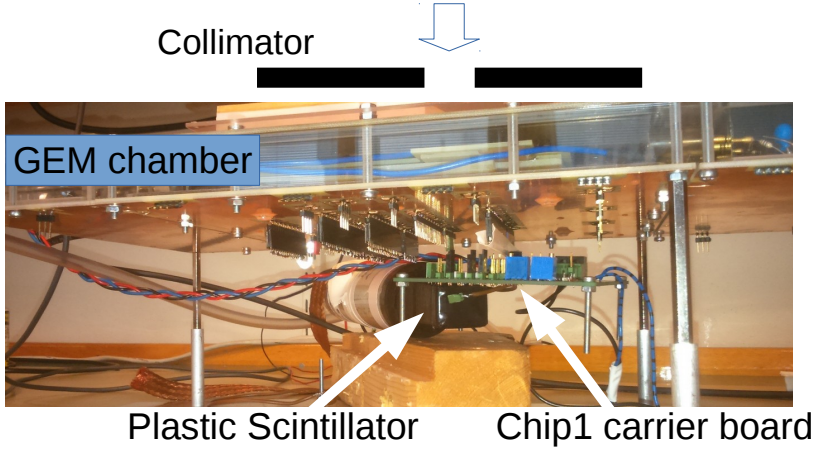


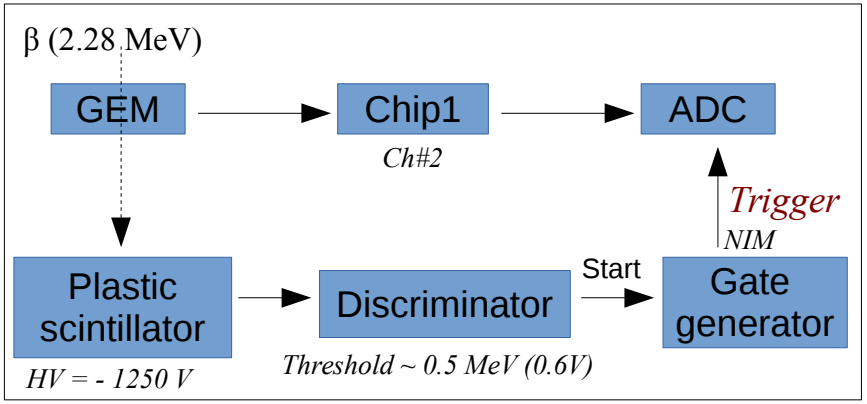
Let’s try testing it with a ‘real’ detector

Measurements with GEMs (Bergen)



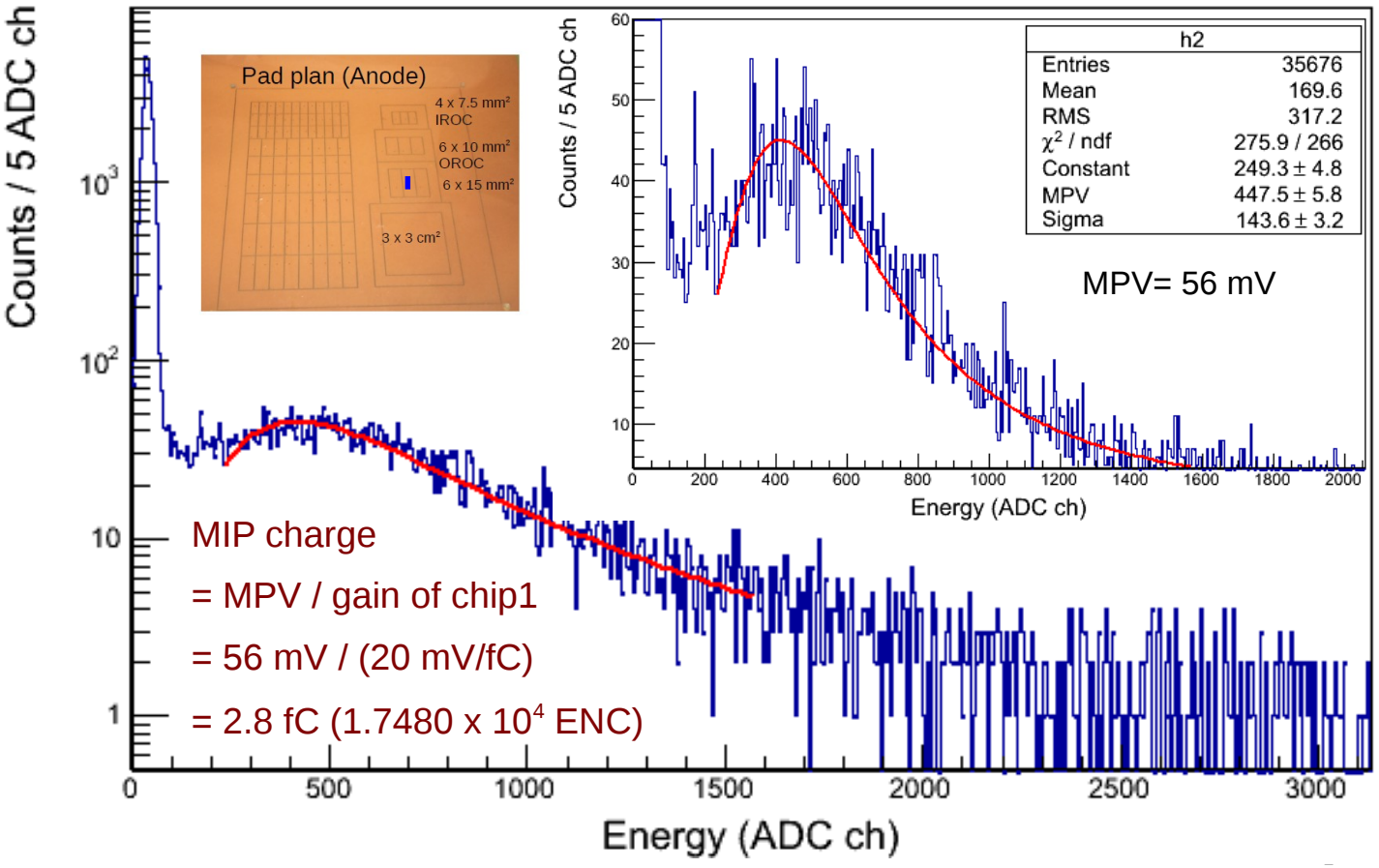
Sr90 – Beta source





Measurements with GEMs (Bergen)

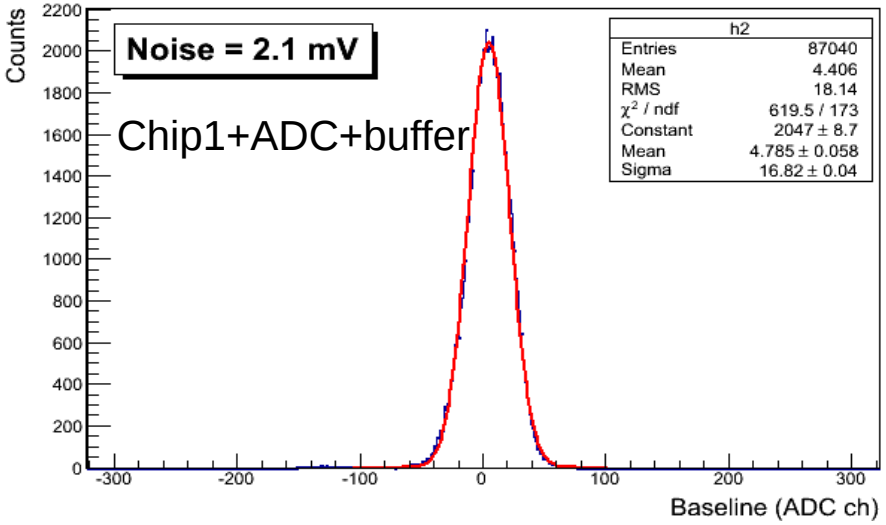
MIP using Sr90 – Landau distribution – single pad (6 x 15 mm^2) – 7 mm drift

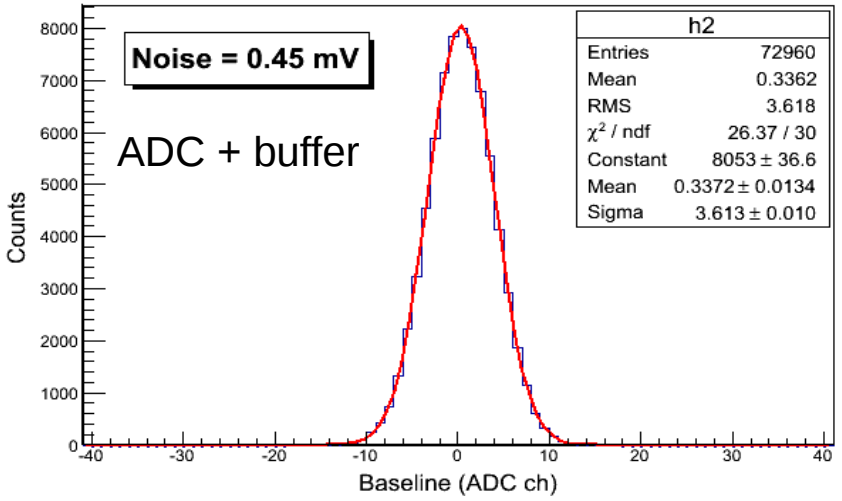


Measurements with GEMs (Bergen)

- Capacitance: single pad + readout pin = 7 pF
- Best case – kapton cable is not used to connect GEM pad and chip1

20 mV/fC gain and 160 ns peaking time





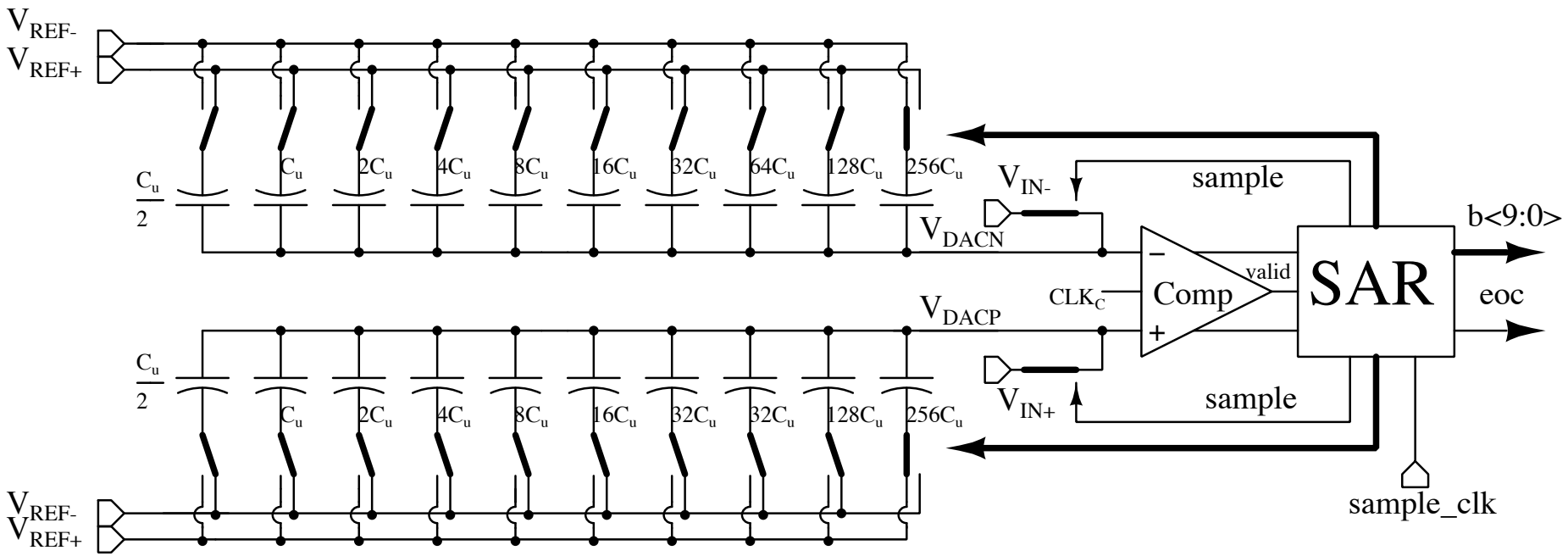
Chip1 noise = sqrt $[(\text{total})^2 - (\text{ADC\_buffer})^2]$

= sqrt $[(2.1)^2 - (0.45)^2]$

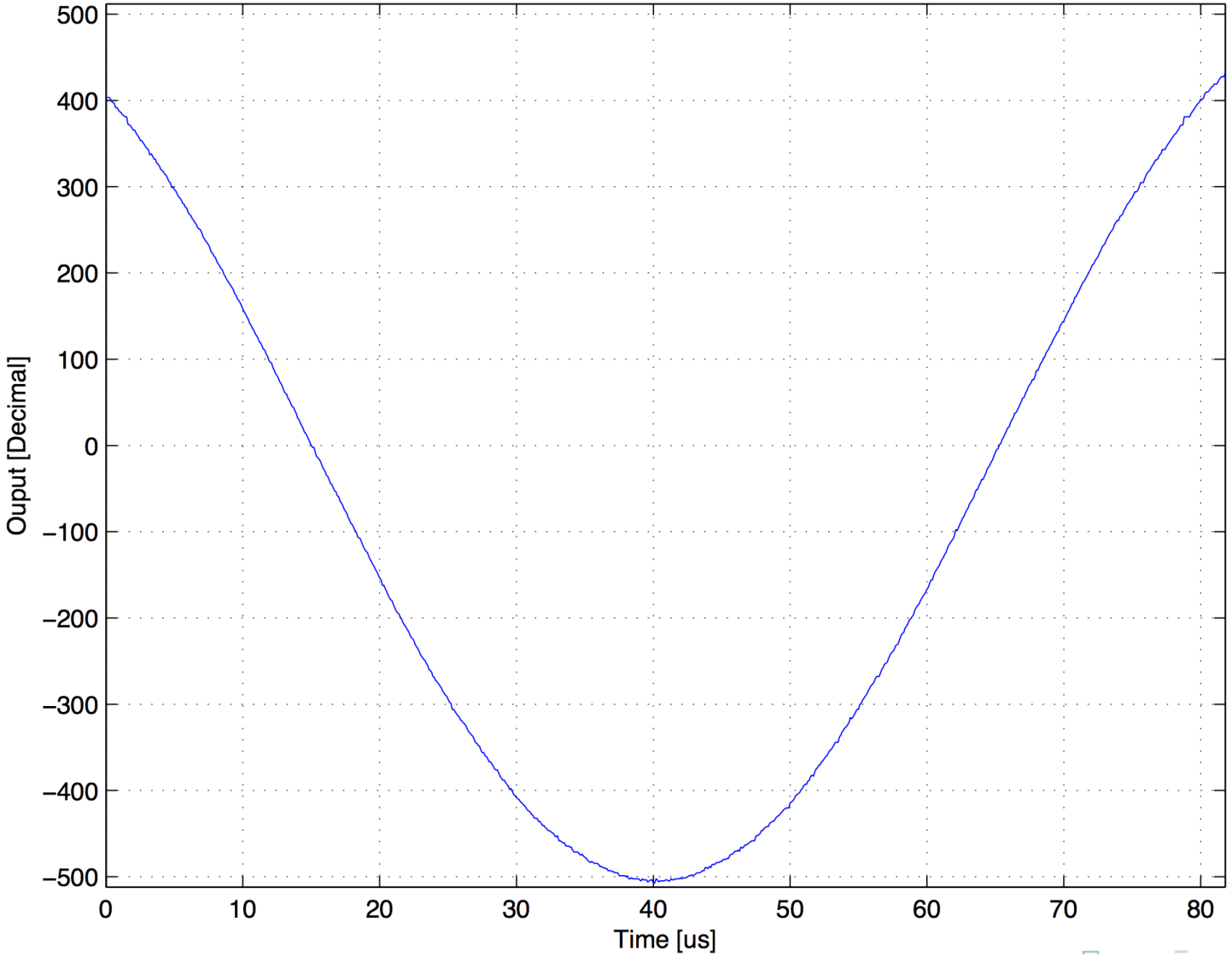
= 2.05 mV = 641 ENC

“ADC”

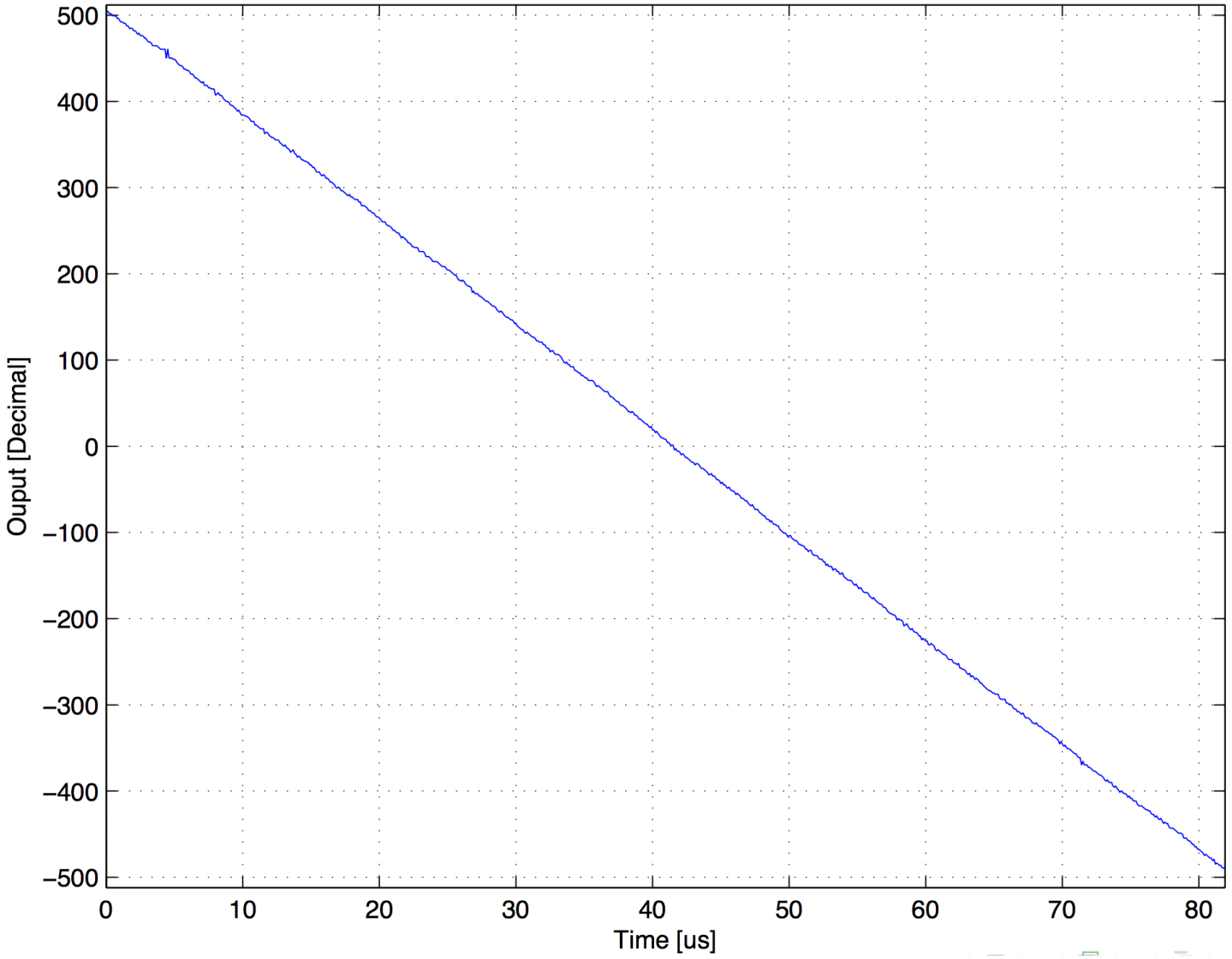
SAR ADC


V_REF-
V_REF+
C_u/2
C_u
2C_u
4C_u
8C_u
16C_u
32C_u
64C_u
128C_u
256C_u
V_DACN
V_DACP
V_IN-
V_IN+
sample
sample
CLK_C
Comp
valid
SAR
b<9:0>
eoc
sample_clk

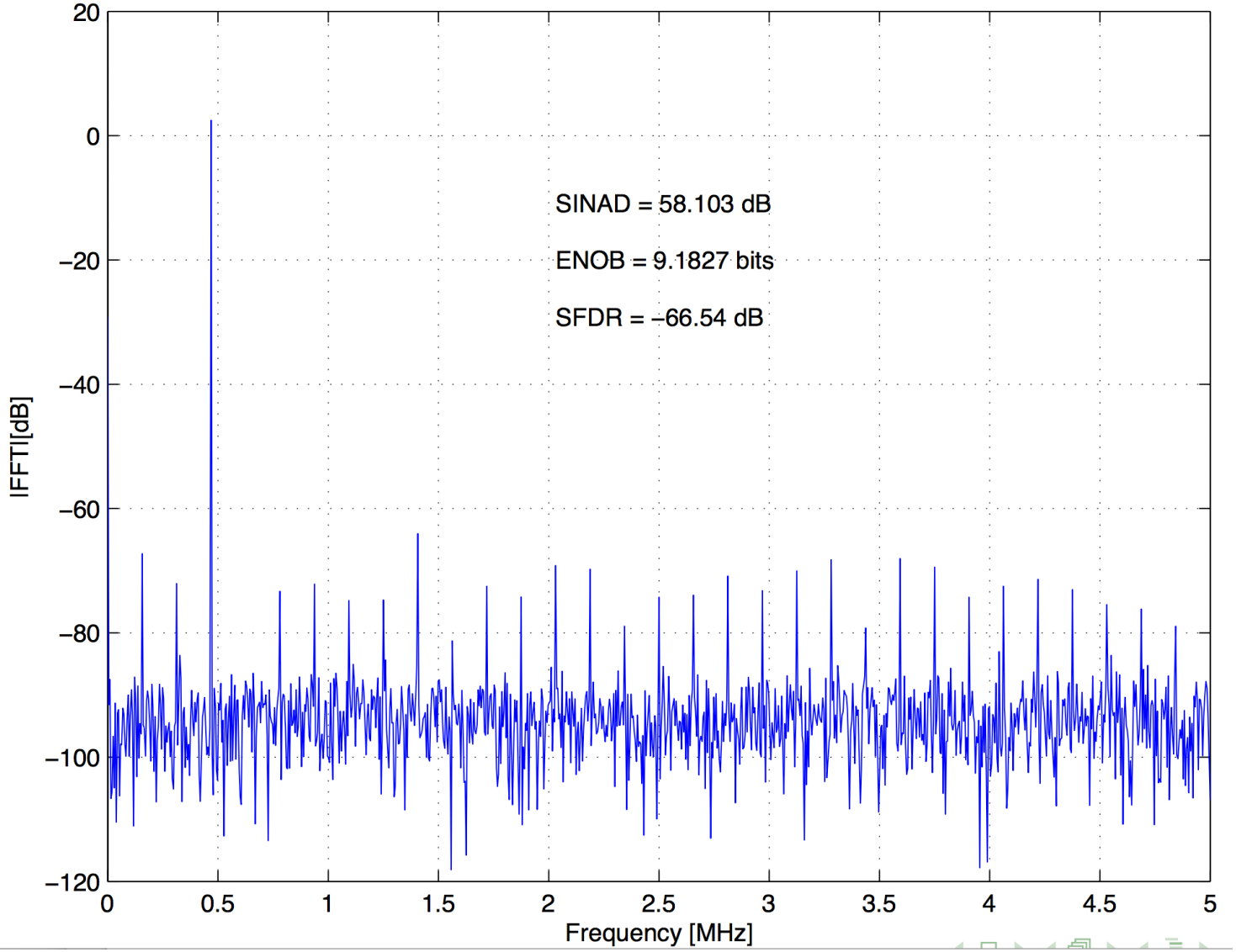
ADC: sine wave, 10kHz



ADC: ramp, 10kHz

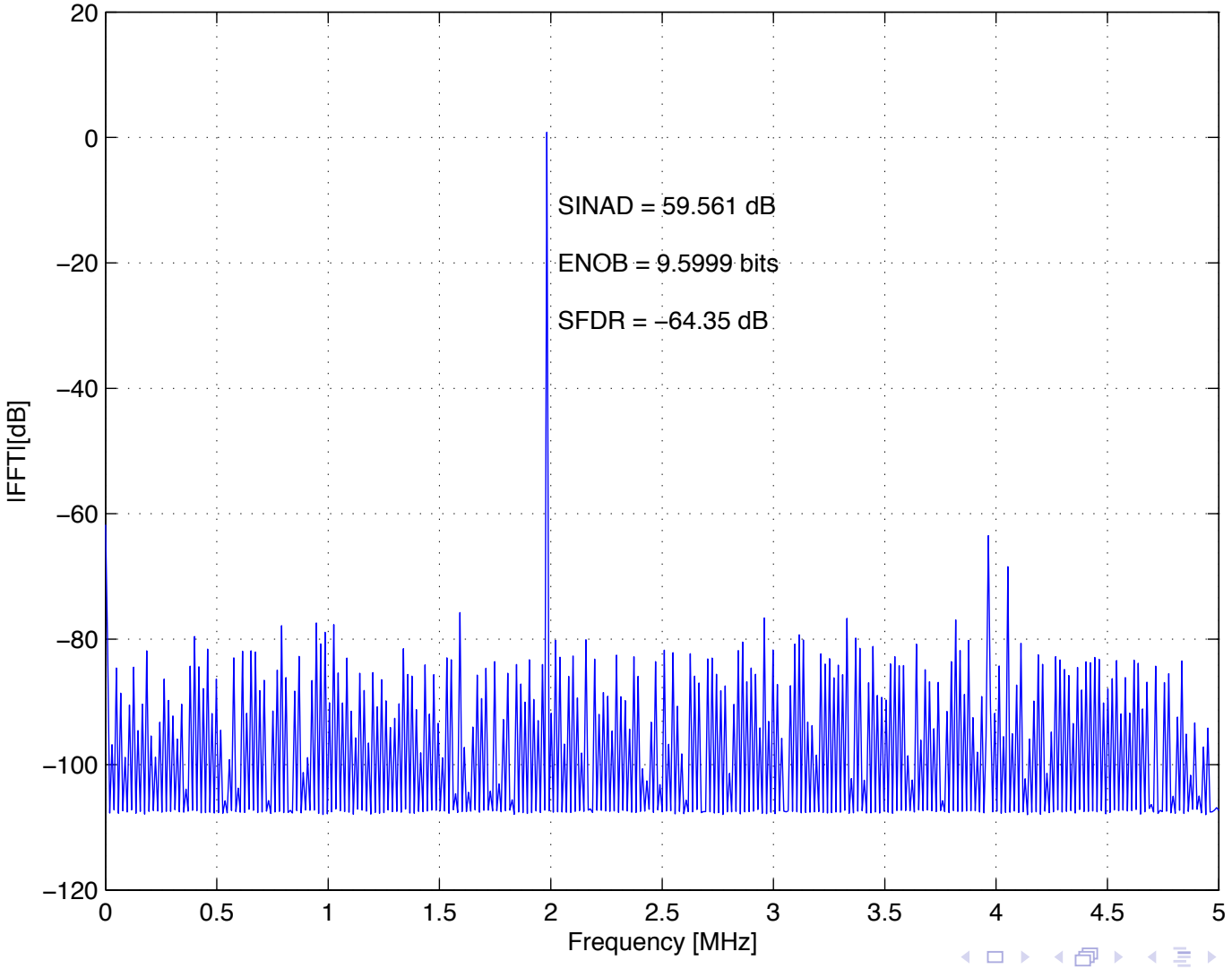


Dynamic test ν_{in}=468.750kHz ν_s=10MHz



MPW2 Simulation

SIMULATION MPW2



Digital, main features

- DSP functionalities fully programmable
- Either triggered or continuous reading operation
- Baseline correction (3 available algorithms)
- Digital shaping filter
- Zero suppression
- Handling the data packaging
- DSP-by-pass (direct streaming of raw data)
- 11 e-links for communication
- Daisy-chaining of chips

Conclusions

- A new ASICs, 32 Ch, Front-end + SAR-ADC + DSP is being produced
- First MPW with single blocks produced and tested
  - Some early prototype problems found and understood.
  - Front-end works, needs some tuning
  - ADC works
- Waiting for the full 32 channels prototype, fabrication is starting right now.

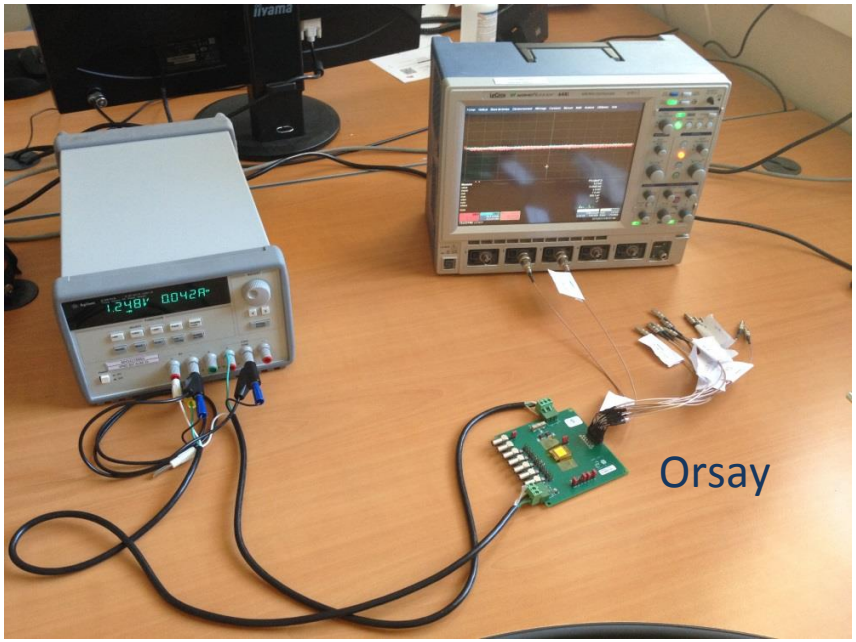
Acknowledging
SAMPA's main designers

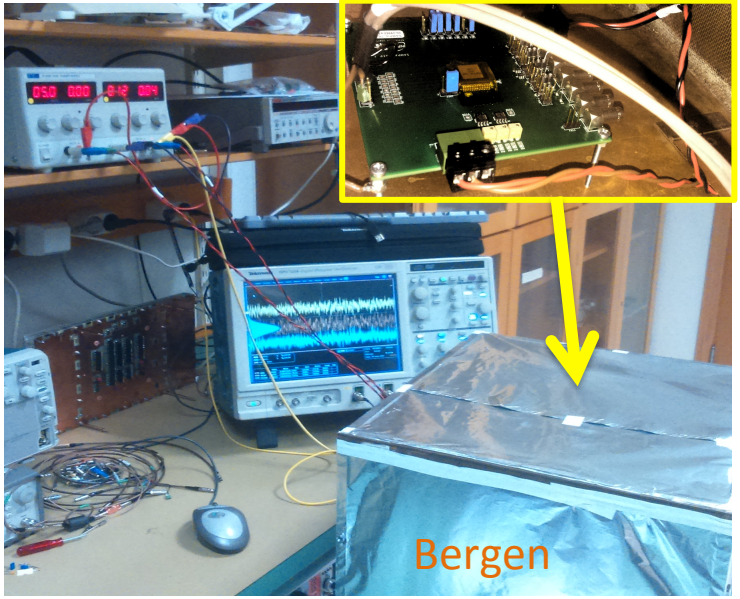
- Br – USP-Poli: Hugo Hernandez, Bruno Sanches
- No - Bergen: Arild Velure

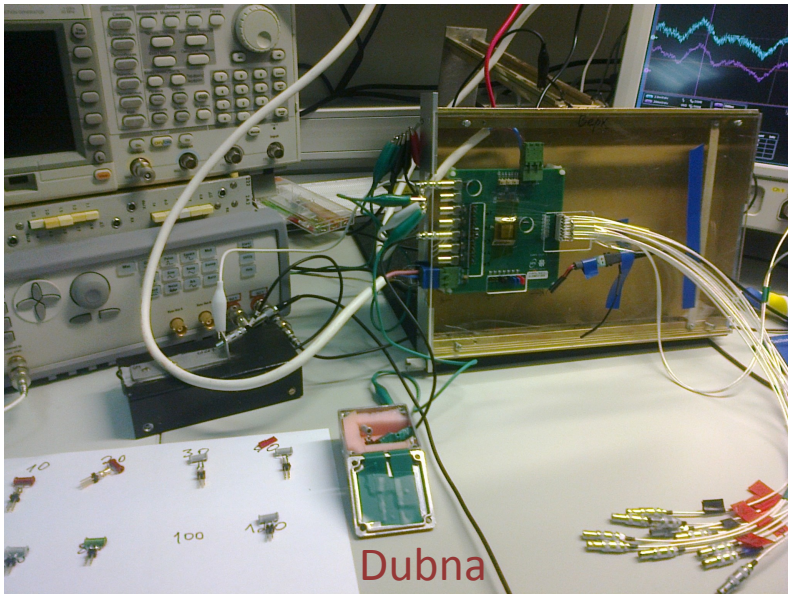
And several other people involved
(either in design or in testing)

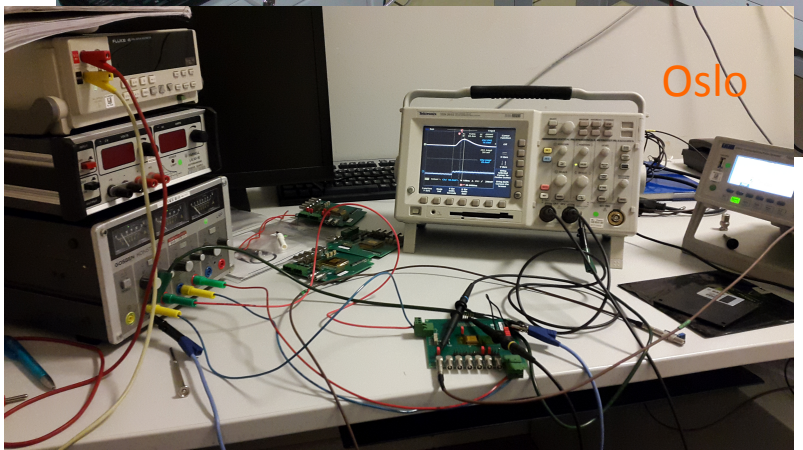
- Br – USP-Poli: W. van Noije, A. Ayala, T. O. Weber, D. Carvalho,
- Br – USP-IF: M. G. Munhoz
- Br – São José: D. Moraes
- Fr – Orsay : P. Russo, V. Chambert, K.M.M., Tun-Lanoë
- No – Bergen: G. J. Tambave
- No – Oslo: S. Musa Mahmood
- Ru – Dubna: A. Piylar, S. Vereschagin, S. Zaporozhets
- Se – Lund: A. Oskarsson

In the different labs…









BACKUP

SAMPA CSA Architecture