VMM Update

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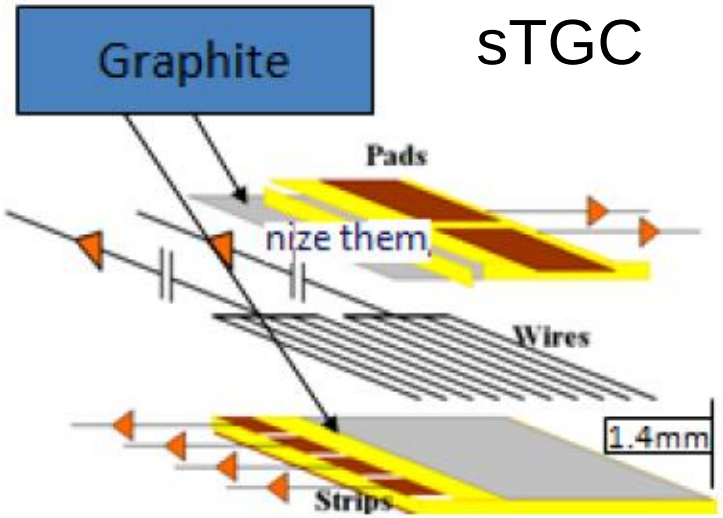
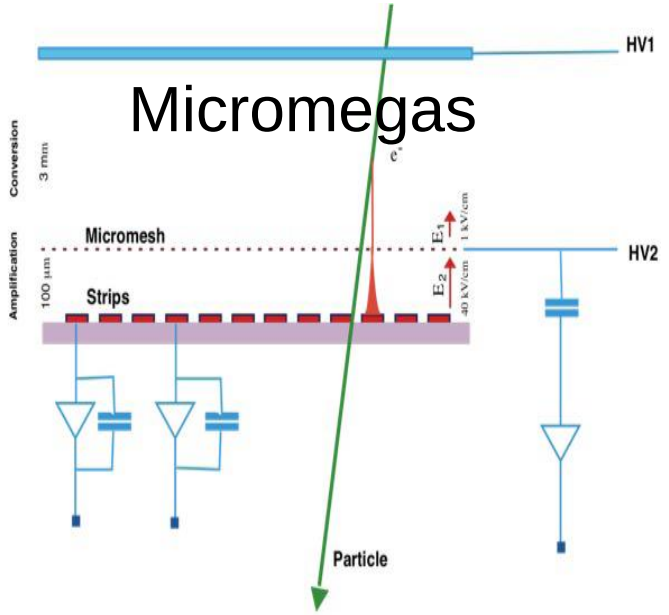
Outline

- Brief Description of the VMM2
  - Changes implemented in the VMM3 Design
- Operation mode for non-ATLAS applications
- VMM2 known problems and workarounds
- VMM2/VMM3 plans
  - Availability of VMM2
  - Plans/schedule/Availability of VMM3
- Closing remarks

Front End for both NSW Technologies

- Both Detectors will participate in the trigger as well as providing precision Level1 measurements
- Imposes severe demands throughout the project and in particular on the Front End
- Provides charge and time measurements as well as Trigger Primitives for both
- To accomplish this, the ASIC has four independent data paths

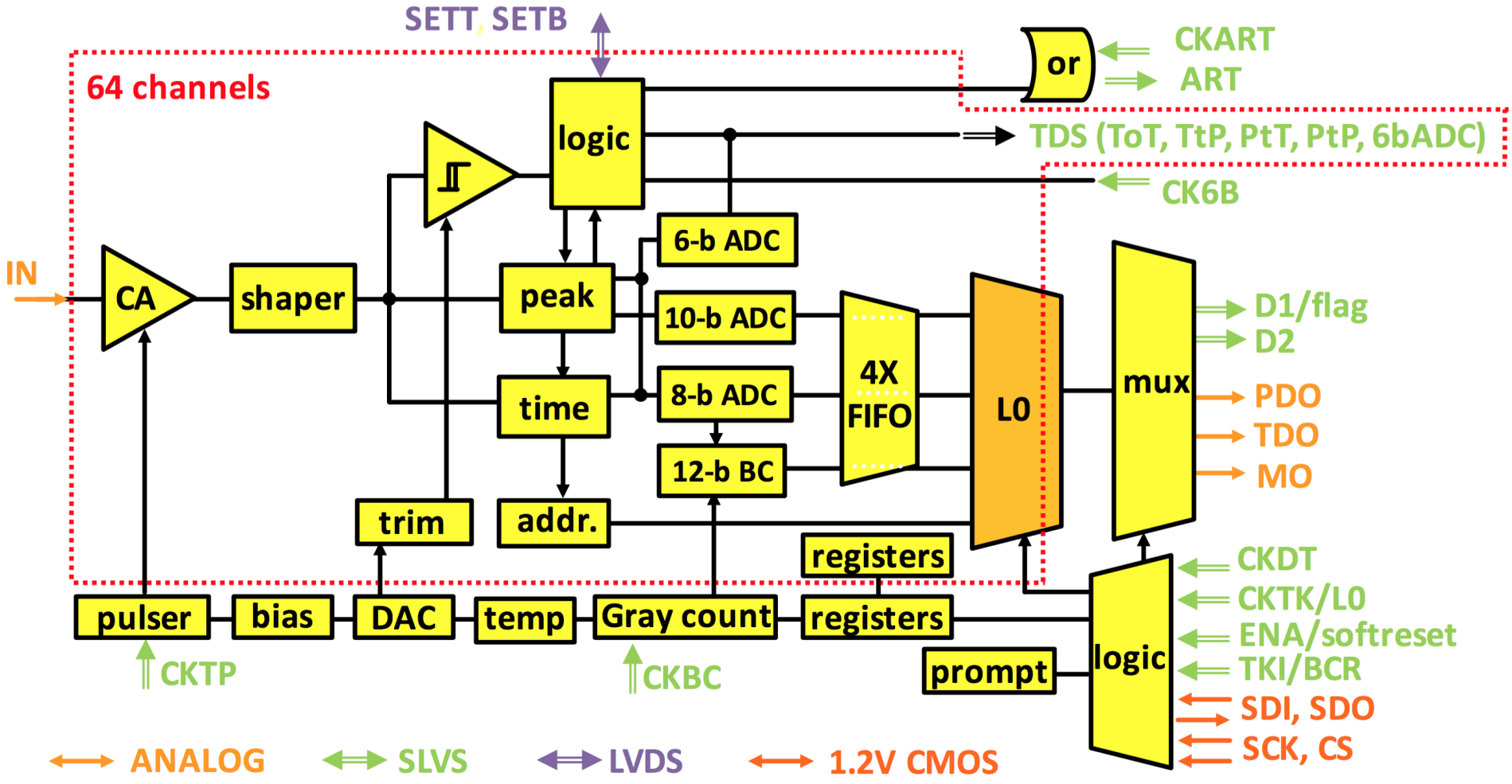




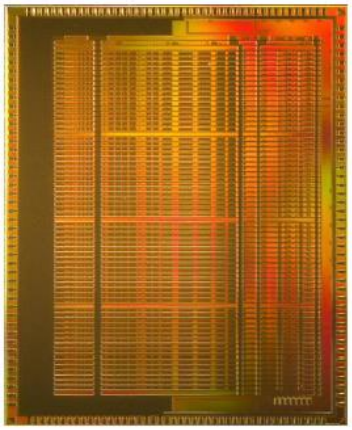
Design Parameters/Features

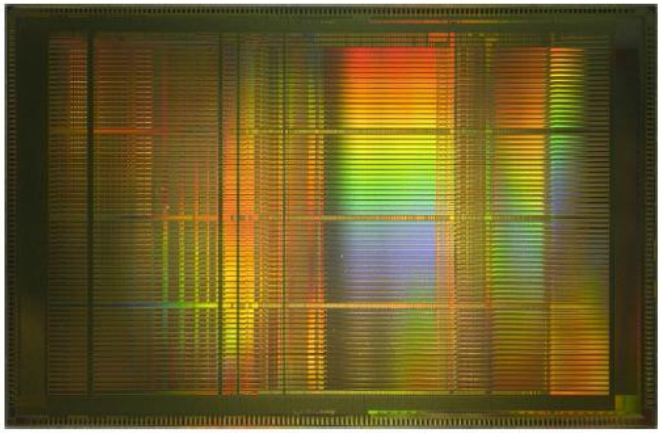
- Dual Polarity
- Adjustable Gain (0.5, 1, 3, 4.5, 6, 9, 12, 16.0 mV/fC)
- Adjustable peaking Time (25, 50, 100, 200 ns)
- Peak Amplitude ADC (10-bit)
- Address in Real Time (Fast OR in effect)
- Prompt 64 channel digitized outputs (6-bit Amplitude) that can be used for more sophisticated trigger algorithms
- Time Detector (resolution <1 ns, 8-bit fine, 12-bit coarse)
- Discriminators with sub-hysteresis
- Neighbor enable logic (channel to channel and across ICs)
- Sparse readout w/smart token passing,
- Threshold trim, built-in calibration, channel mask, analog monitor, temp. sensor, Band Gap Reference, custom sLVS

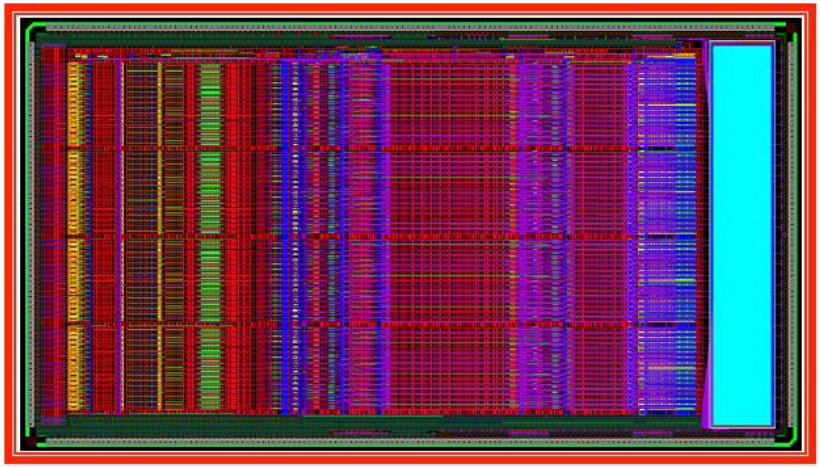
VMM3 Block Diagram (G. de Geronimo, BNL)



Front-end ASIC for Muon New Small Wheel (4)







VMM1 (2012)
50 mm²
500k MOSFETs
(8k/ch.)
- mixed-signal
- 2-phase readout

VMM2 (2014)
115 mm²
> 5M MOSFETs (>80k/ch.)
- planned deep re-design of VMM1
- much higher functionality and complexity than VMM1
- continuous fully-digital readout

VMM3 (2015-16)
130 mm²
> 6M MOSFETs
- **L0 handling, SEU-tolerant, SLVS IOs, deeply revised front-end for sTGC signals, various additional functions, various fixes**
- **input from many collaborating teams with broad range of expertise**
- **aims at pre-production**

- *VMM ASIC is a SoC developed for Muon NSW in ATLAS Phase-I upgrade*
- *Collaborating with university groups, study is ongoing to use VMM in MDT trigger and readout design in ATLAS Phase-II upgrade*

VMM3 Pinout - Preliminary

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
B	Vddp	Vddp	Vddp	Vss	Vss	Vss	Vss	pdo	Vdd	Vdd	Vdd	Vssd	+ CKBC -		+ CKTP -		SDI	SDO	CS	SCK
C	i0	i1	i2	i3	Vss	Vss	Vss	mo	Vdd	Vdd	Vdd	Vssd	+ TKI -		+ TKO -		+ ENA -		+ CK6B -	
D	i4	i5	i6	i7	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vssd	+ CKTK -		+ DT0 -		+ DT1 -		+CKART-	
E	i8	i9	i10	i11	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vssd	+ ART -		+ CKDT -		+ t0 -		+ t1 -	
F	i12	i13	i14	i15	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vssd	+ t2 -		+ t3 -		+ t4 -		+ t5 -	
G	i16	i17	i18	i19	Vss	Vss	Vss	Vdd	Vdd	Vssd	Vssd	Vssd	+ t6 -		+ t7 -		+ t8 -		+ t9 -	
H	i20	i21	i22	i23	Vss	Vss	Vss	Vdd	Vdd	Vssd	+ t10 -		+ t11 -		+ t12 -		+ t13 -		+ t14 -	
J	i24	i25	i26	i27	Vss	Vss	Vss	Vdd	Vdd	Vssd	+ t15 -		+ t16 -		+ t17 -		+ t18 -		+ t19 -	
K	i28	i29	i30	i31	Vss	Vss	Vss	Vdd	Vdd	Vssd	+ t20 -		+ t21 -		+ t22 -		+ t23 -		+ t24 -	
L	i32	i33	i34	i35	Vss	Vss	Vss	Vdd	Vdd	Vddd	+ t25 -		+ t26 -		+ t27 -		+ t28 -		+ t29 -	
M	i36	i37	i38	i39	Vss	Vss	Vss	Vdd	Vdd	Vddd	+ t30 -		+ t31 -		+ t32 -		+ t33 -		+ t34 -	
N	i40	i41	i42	i43	Vss	Vss	Vss	Vdd	Vdd	Vddd	+ t35 -		+ t36 -		+ t37 -		+ t38 -		+ t39 -	
P	i44	i45	i46	i47	Vss	Vss	Vss	Vdd	Vdd	Vddd	Vddd	Vddd	+ t40 -		+ t41 -		+ t42 -		+ t43 -	
R	i48	i49	i50	i51	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	+ t44 -		+ t45 -		+ t46 -		+ t47 -	
T	i52	i53	i54	i55	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	+ t48 -		+ t49 -		+ t50 -		+ t51 -	
U	i56	i57	i58	i59	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	+ t52 -		+ t53 -		+ t54 -		+ t55 -	
V	i60	i61	i62	i63	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	+ t56 -		+ t57 -		+ t58 -		+ t59 -	
W	Vddp	Vddp	Vddp	Vss	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	+ t60 -		+ t61 -		+ t62 -		+ t63 -	
Y	Vddp	Vddp	Vddp	Vss	Vss	Vss	Vss	Vdd	Vdd	Vdd	V ssad	V ssad	V ssad	V ssad	V ddad	V ddad	V ddad	V ddad	+ SETB -	

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
B	Vddp	Vddp	Vddp	Vss	Vss	Vss	Vss	tdo	Vdd	Vdd	V ssad	V ssad	V ssad	V ssad	V ddad	V ddad	V ddad	V ddad	+ SETT -	

Vddp preamp +1.2V

Vdd analog +1.2V

Vss analog 0V

V ddad ADC +1.2V

V ssad ADC 0V

Vddd digital +1.2V

Vssd digital 0V

analog in

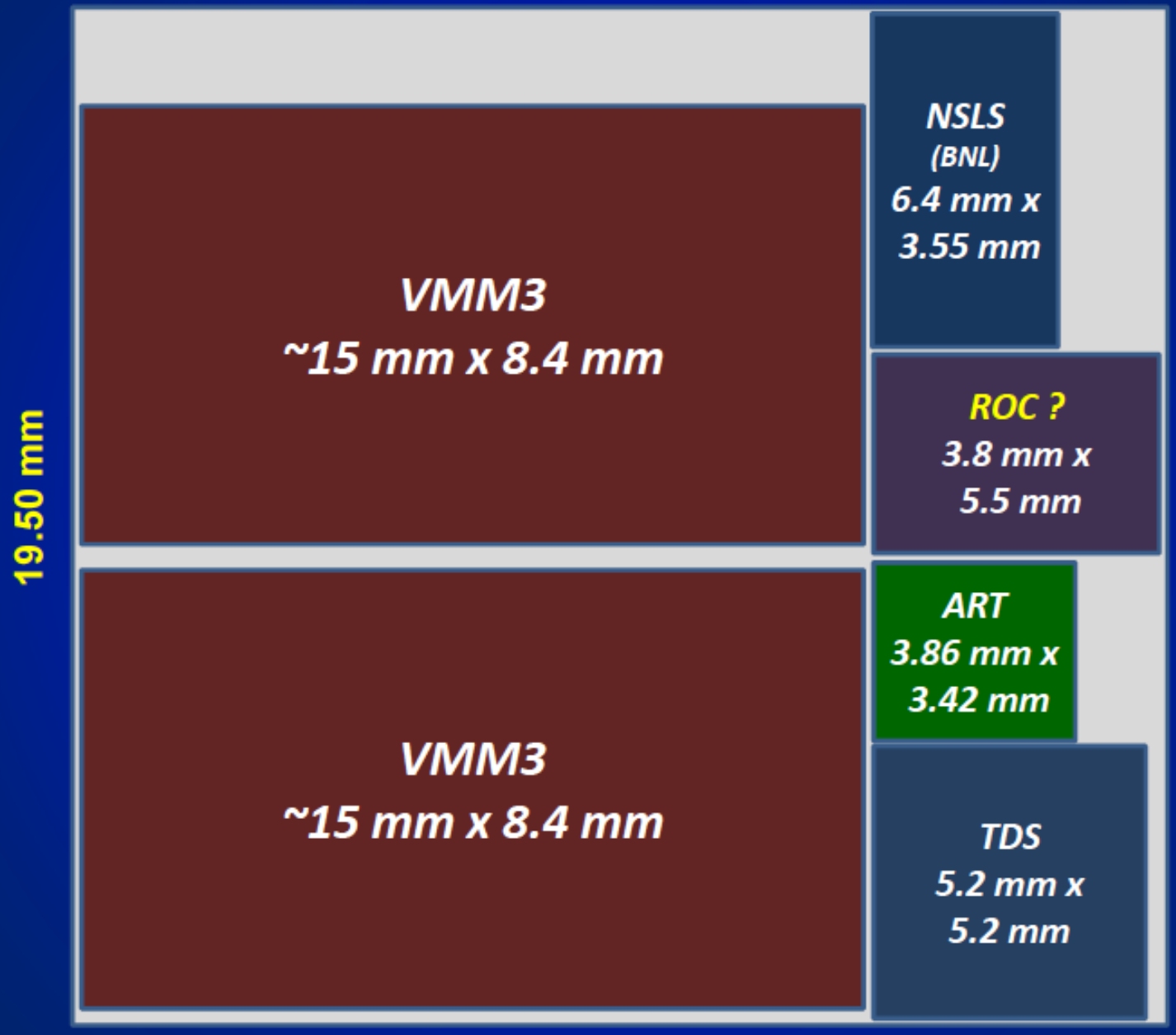
analog out

digital SE IO

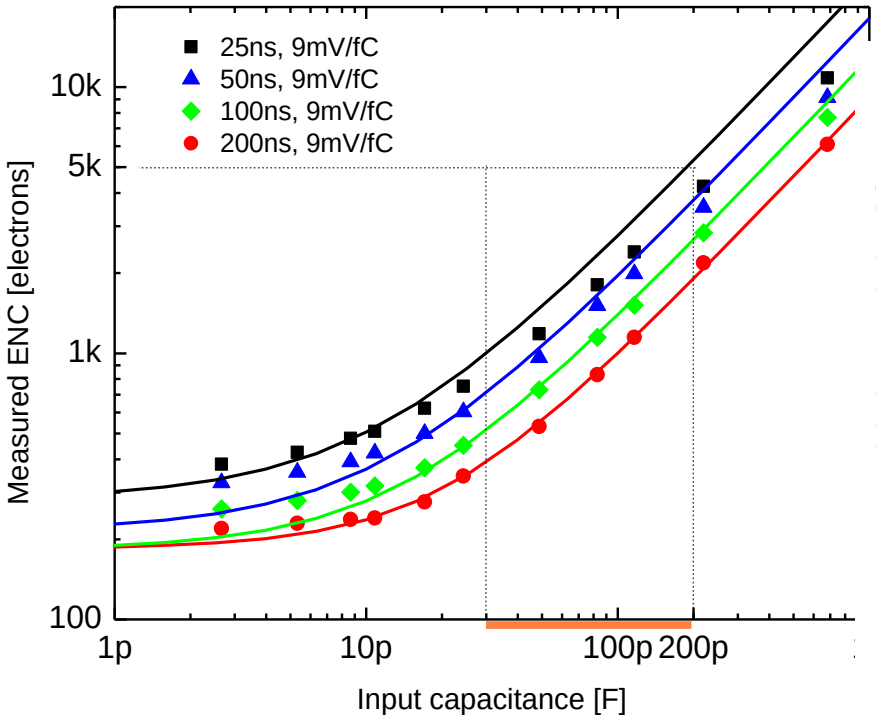
+ xxx - SLVS IO

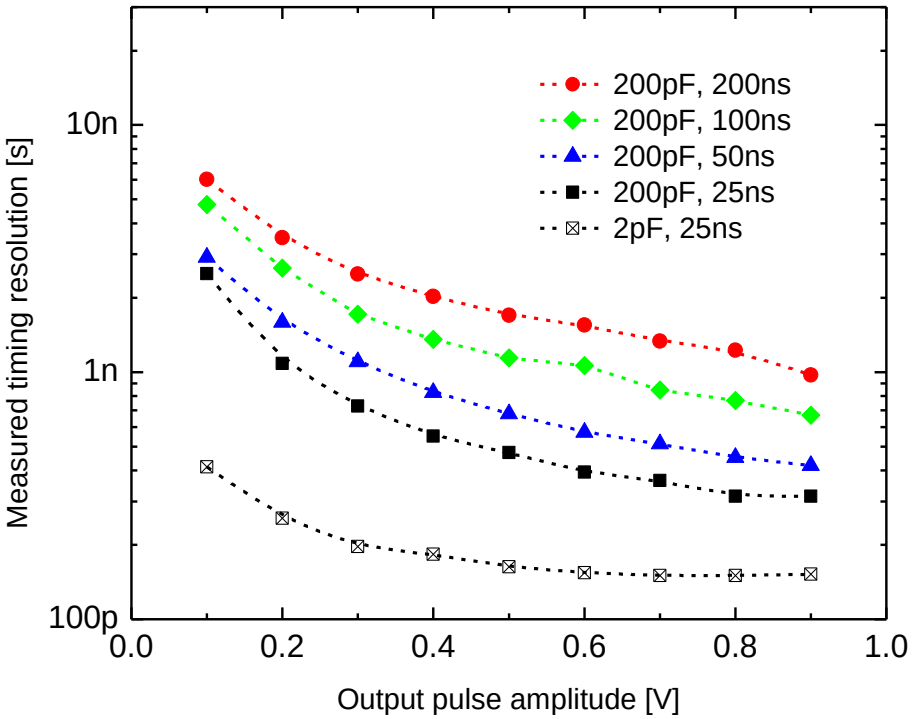
BGA 400 pin, 21 x 21 mm, pitch 1 mm

Wafer Reticle Occupancy



Measured and Expected Noise and Timing Resolution

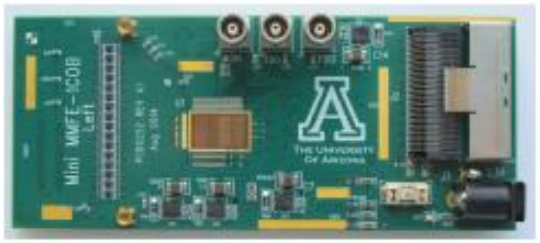




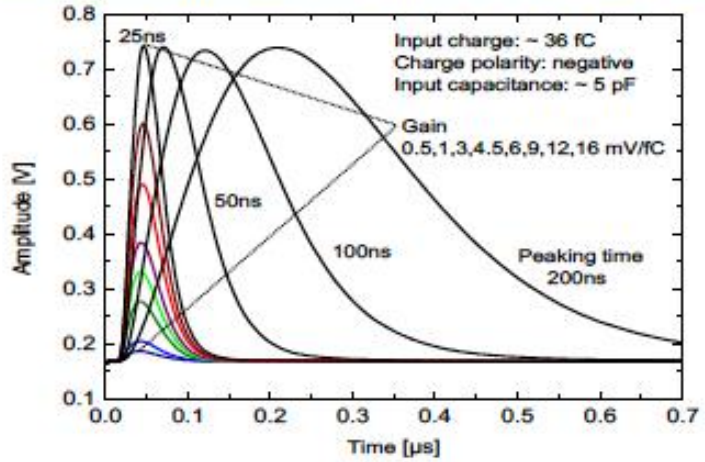
- ENC as a function of input capacitance
- <1fC even with fast shaping (25 ns) and large input capacitance (200 pF)

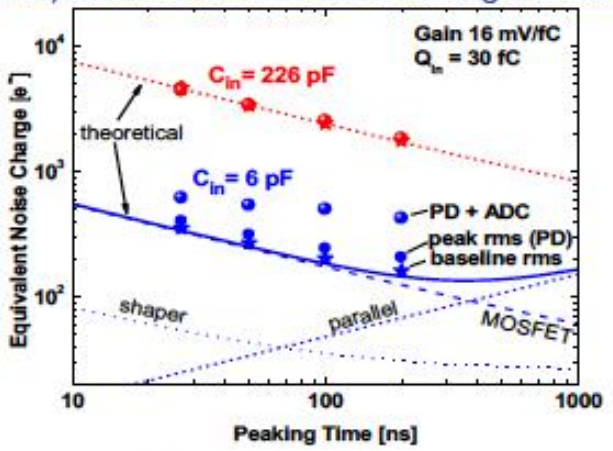
Time resolution as a function of amplitude ~ ns resolution and timewalk

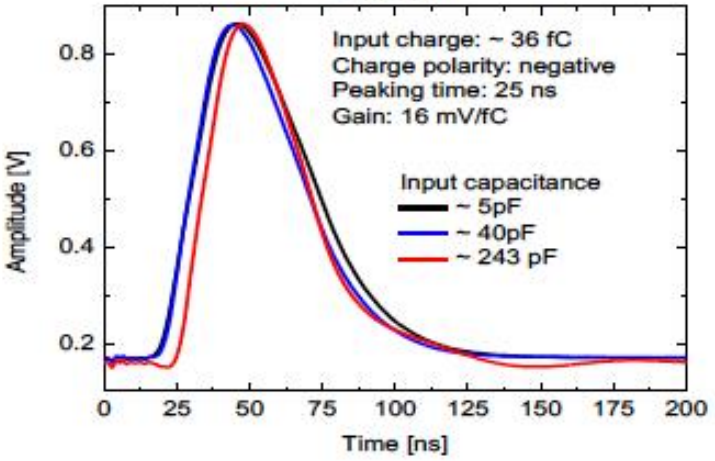
Early Tests of VM2

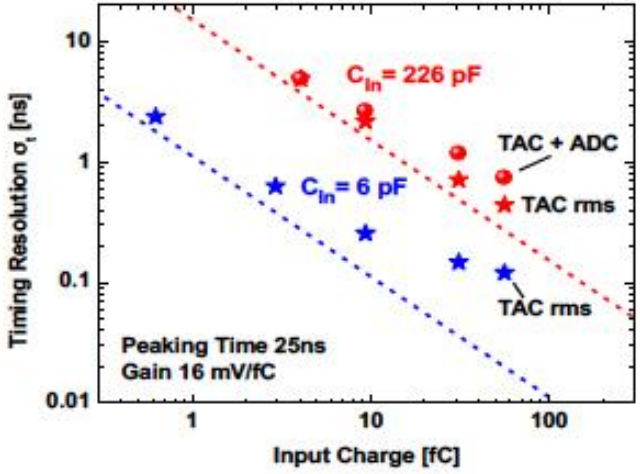


Several board developments with 1x (ATLAS), 2x (RD-51 SRS), 8x (ATLAS) realised last months allowing the extensive testing









4 Independent Data Paths

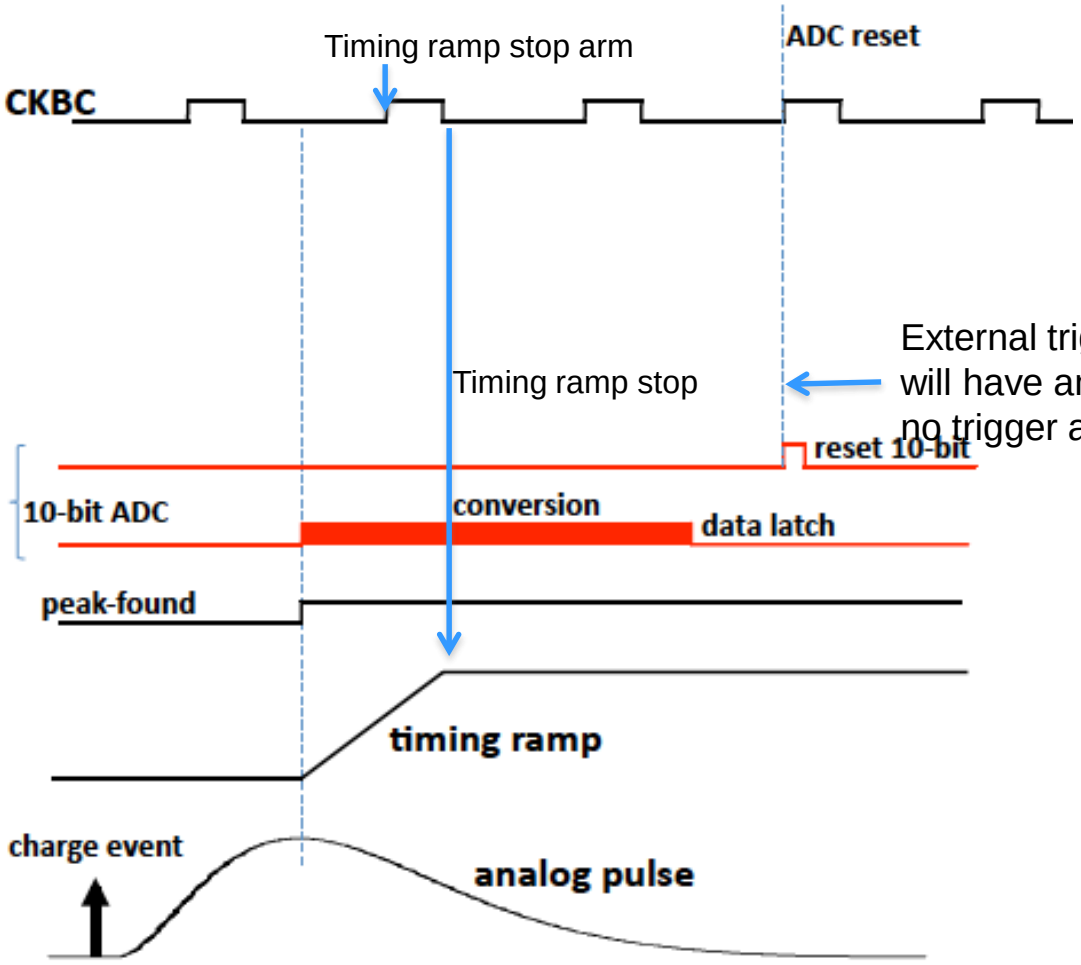
- Digital Serial out in DDR and two phase clock for 640 Mbps effective bandwidth
  - ATLAS mode with adjustable Latency and Level0/1 buffers
  - Local, non-ATLAS 4-deep buffer, "test beam mode"
- Address in Real Time (ART), serial out 320 Mbs
- Direct 64 channel out (6-bit amplitudes, serially out 320 Mbps)
- Serial Analog out (both amplitude and time)
  - Can be used with external digitizers, e.g., the SRS Analog card

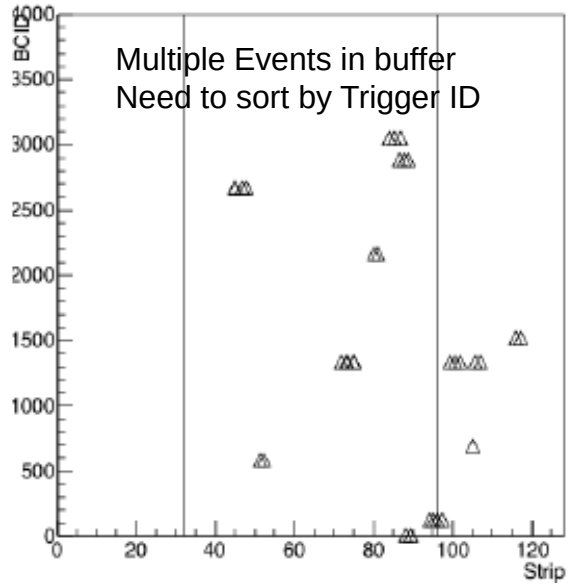
The VMM is designed for synchronous machines like the LHC, Data driven, Continuous read/write, not responding to triggers.

Work around for test beam or traditional fixed target experiments

Amplitude and Timinng

Timing Measurement Pro





Multiple Events in buffer
Need to sort by Trigger ID

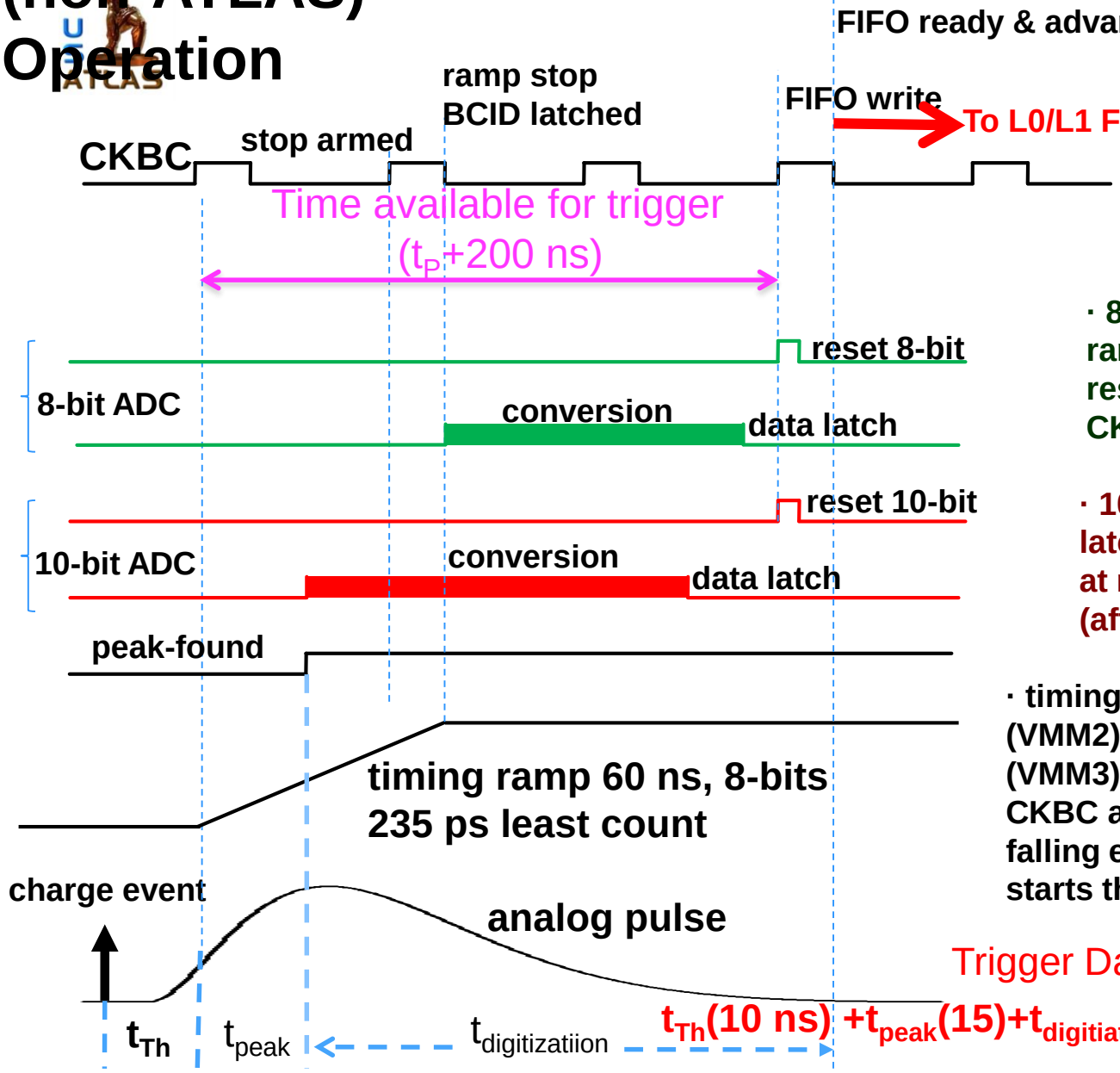
External trigger initiates Readout. VMM3 will have an option to reset the channel if no trigger arrives at the end of timing ramp

- 10-bit ADC starts at peak, latches after conversion, resets at next rising edge of CKBC (after latch)

- timing ramp starts at peak-found

Test-beam mode (non-ATLAS) Operation

Use external trigger to push Data



· first ck of CKBC after peak-found stops ramp
· first ck of CKBC after latches writes FIFO

· 8-bit ADC starts at stop of ramp, latches after conversion, resets at next rising edge of CKBC (after latch)

· 10-bit ADC starts at peak, latches after conversion, resets at next rising edge of CKBC (after latch)

· timing ramp starts at peak-found (VMM2) or threshold crossing (VMM3); the next rising edge of CKBC arms the stop circuit; the next falling edge stops the ramp and starts the 8-bit ADC conversion

Trigger Data Latency

t_{Th}(10 ns) +t_{peak}(15)+$t_{digitiation}$(200)+t_{GBT} (170) ~400 ns

Main Problems of the VMM2

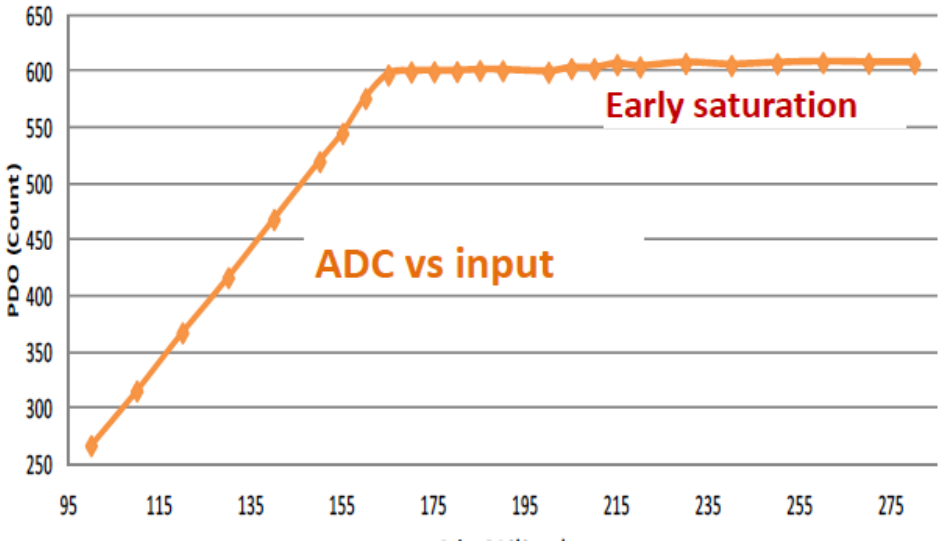
Several bugs found and corrected in the new design (VMM3)

Many improvements were implemented

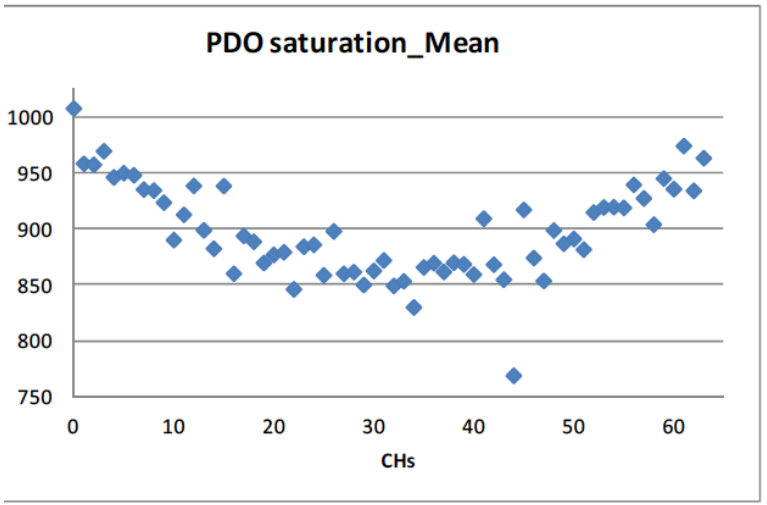
I will describe the three main problems found in the VMM2

1. Early saturation limiting the dynamic range by ~20-25%
2. Token logic getting out of sync
3. ADC problem limiting the resolution to probably 7 or so bits

Early Saturation



Average of Early Saturation

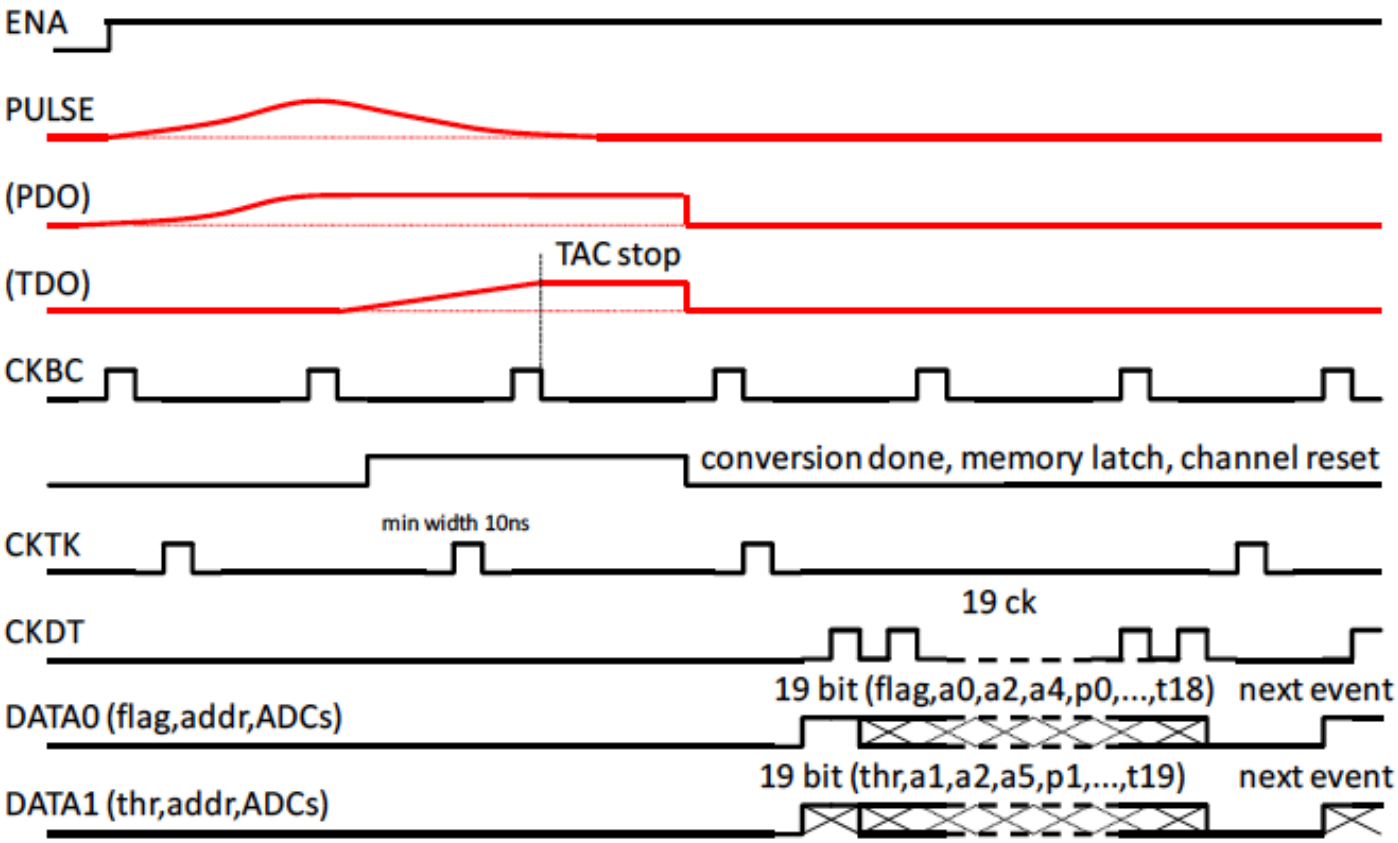


- Early saturation has an average minimum at center channels

Found that many channels saturate earlier than designed (1 V)
Problem traced to weak mixed-signal power supply
Affects channels in the middle of the 64 channel chain because power distribution is provided at the ends of the chain.
Fixed in VMM3

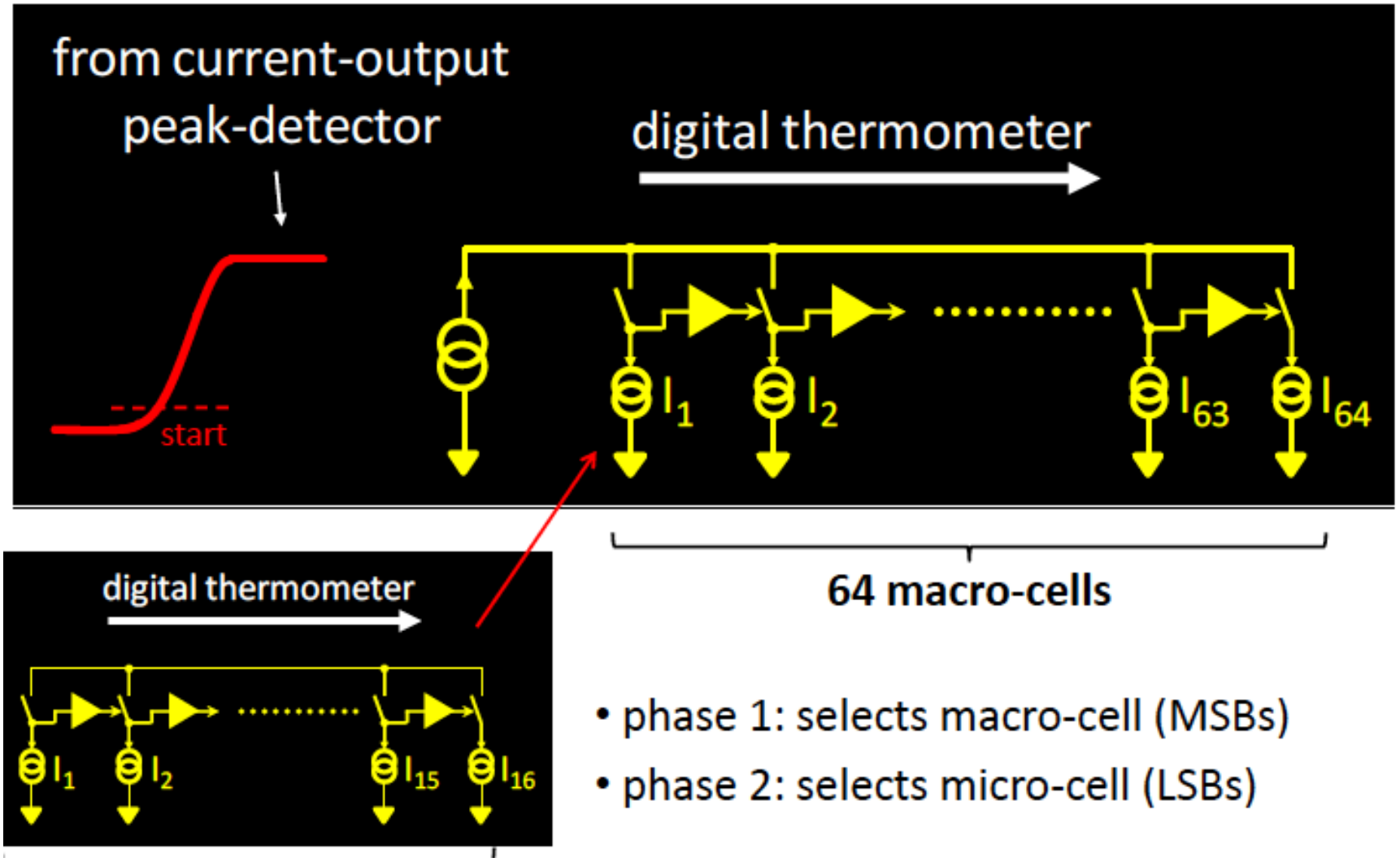
Token Logic out of Sync

- Results in many readout problems, multiple data,



Issuing a "SoftReset" after readout restores state machine

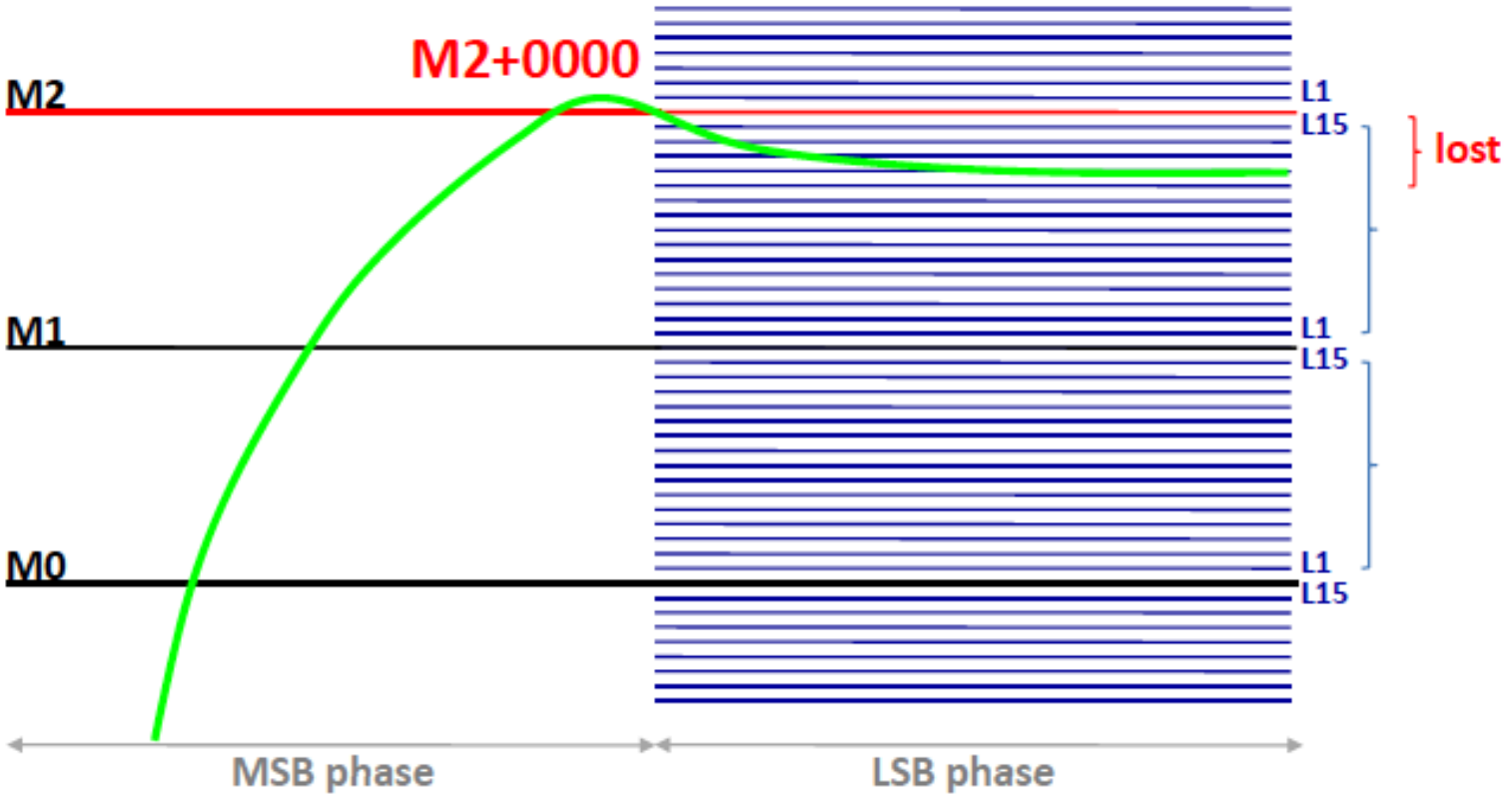
ADC problem
Current Mode "Domino" ADC



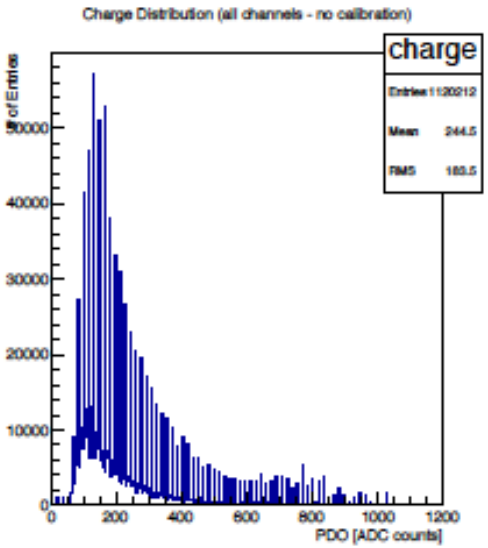
- phase 1: selects macro-cell (MSBs)
- phase 2: selects micro-cell (LSBs)

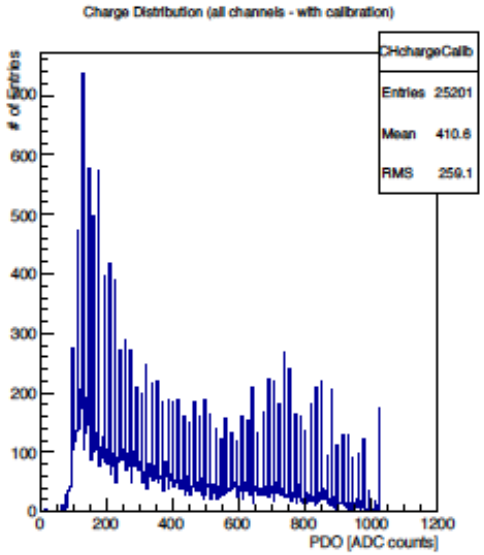
LSB lost due to overshoot

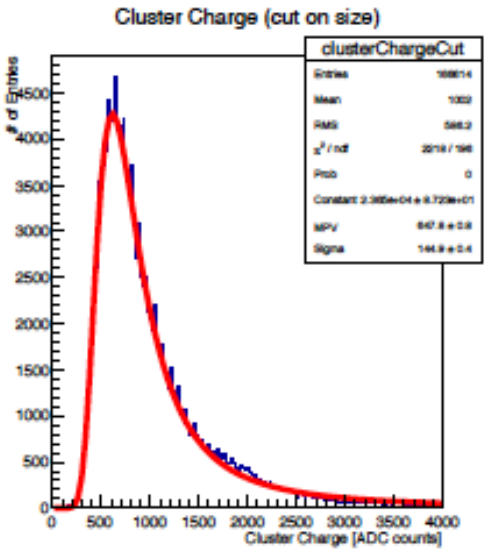
Impact of Current Overshoot on ADC

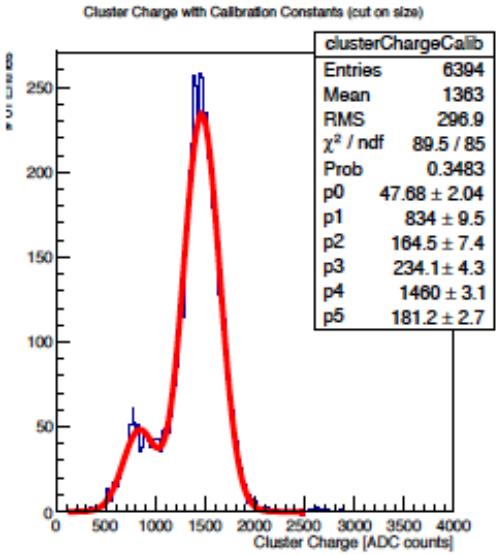


Some results using the SRS “hybrid”









The “mini-2” front end card (Sorin Martoiu) pin compatible with the APV25 hybrids

Measurements by George Iakovidis

(Left) Landau distribution before and after calibration and clustering

(Right) ^{55}Fe Spectrum

Summary, Plans, Availability of VMM2/3

- VMM2 was produced 1.5 years ago, has been undergoing tests since then
- Several issues uncovered, studied, corrected in VMM3 design
- Work arounds exist for the main Issues
- Ordered additional engineering wafers, die expected this Friday March 11
- Will be packaged by Novapack ~1-2 months
- Samples in modest quantities will be available
- No license issues, anybody can have them
- VMM3 to be submitted this month, die expected 10 weeks later
- Have ordered 25 additional wafers →~6000 chips
- Samples again should be available