ATCA-SRS and GEMROC

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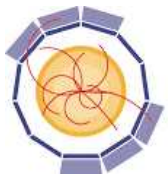

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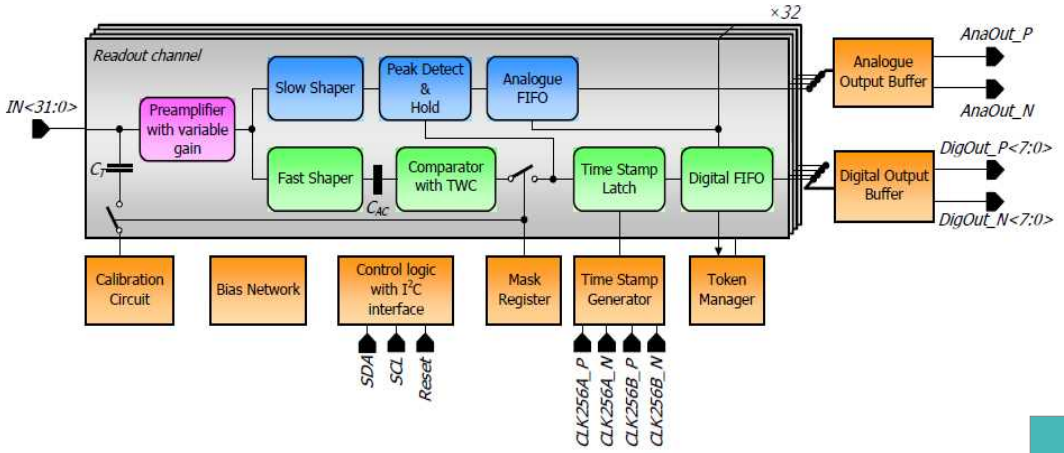
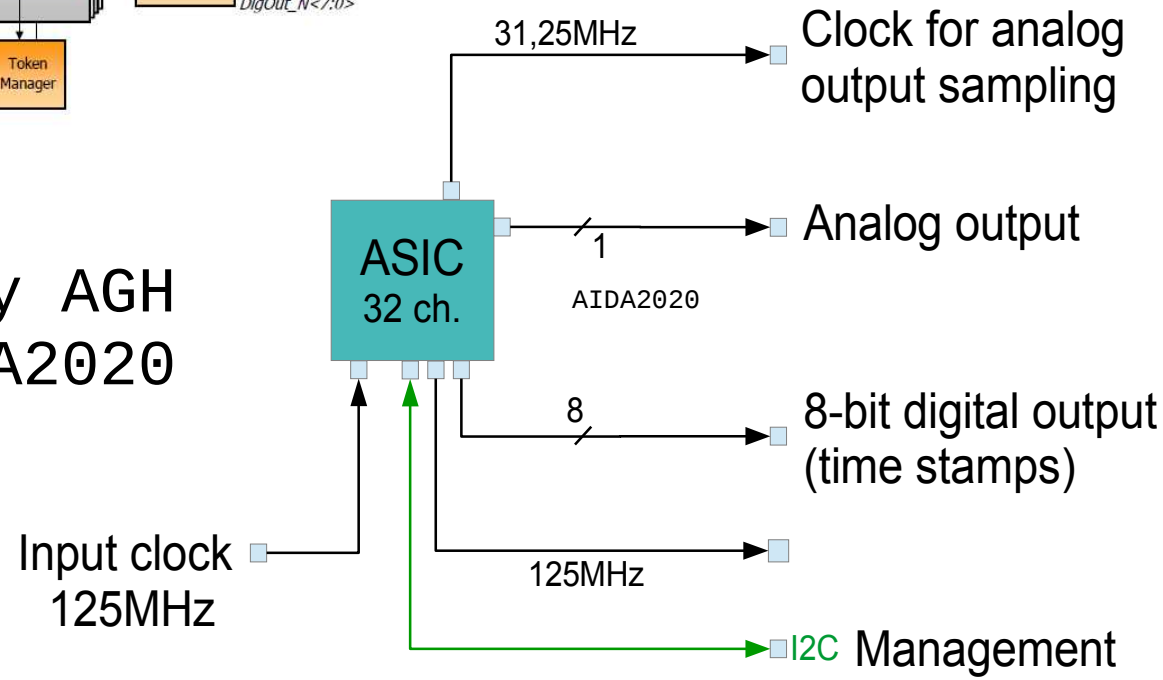
eicSys GmbH
Embedded Integrated Control Systems

GEMROC



GEMROC designed by AGH and supportet AIDA2020



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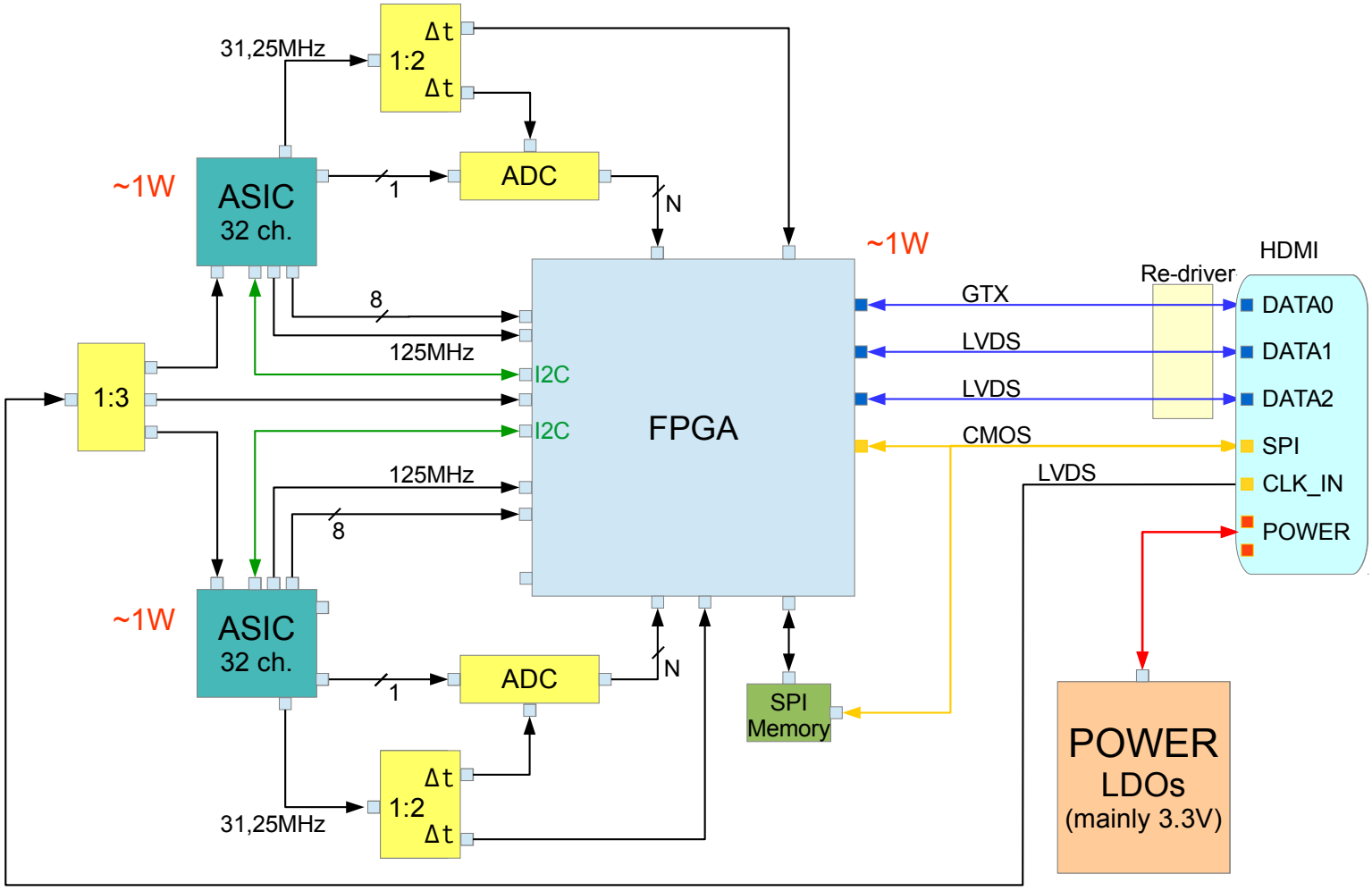
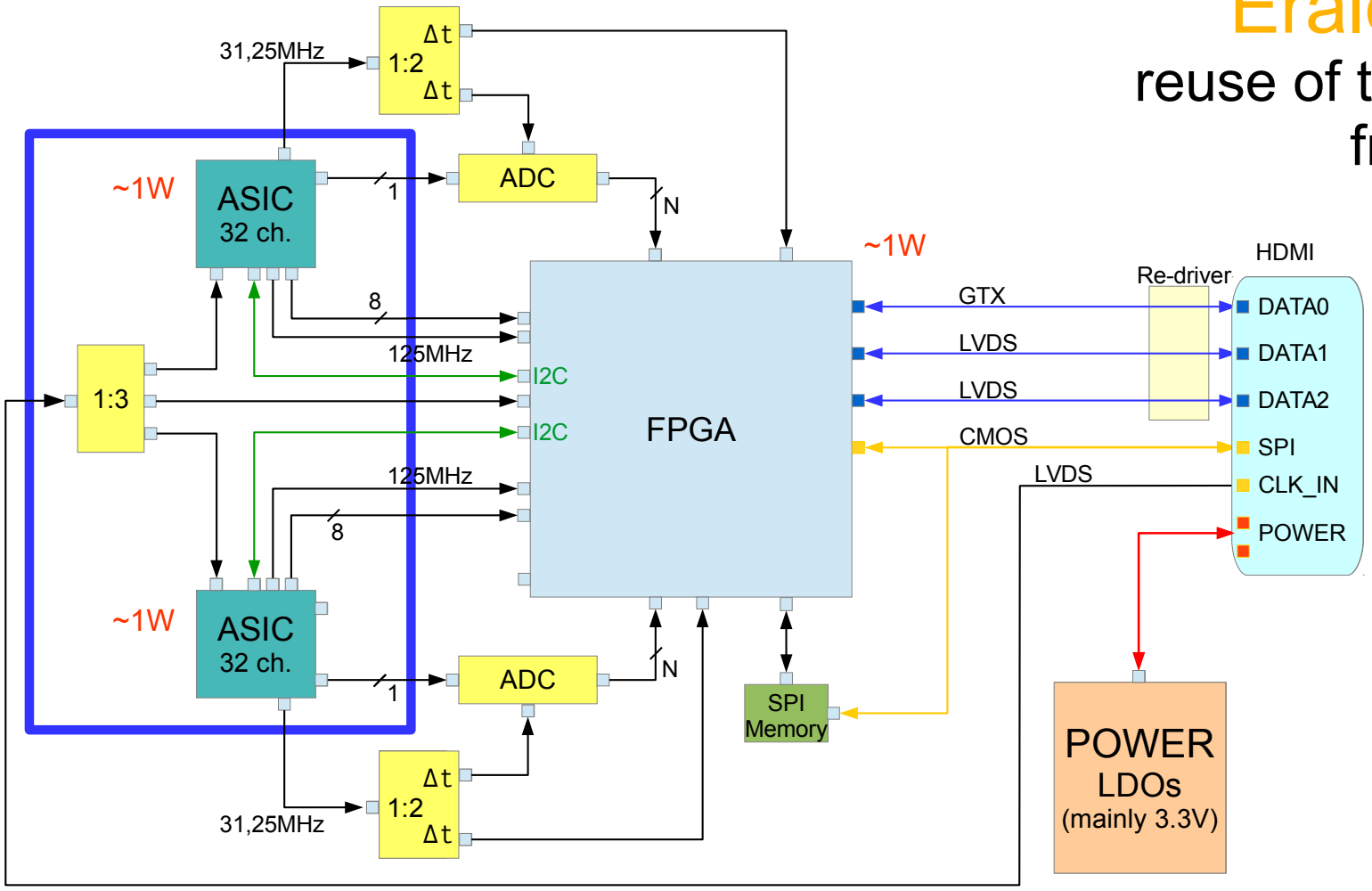
GEMROC – Hybrid – ATCA-SRS



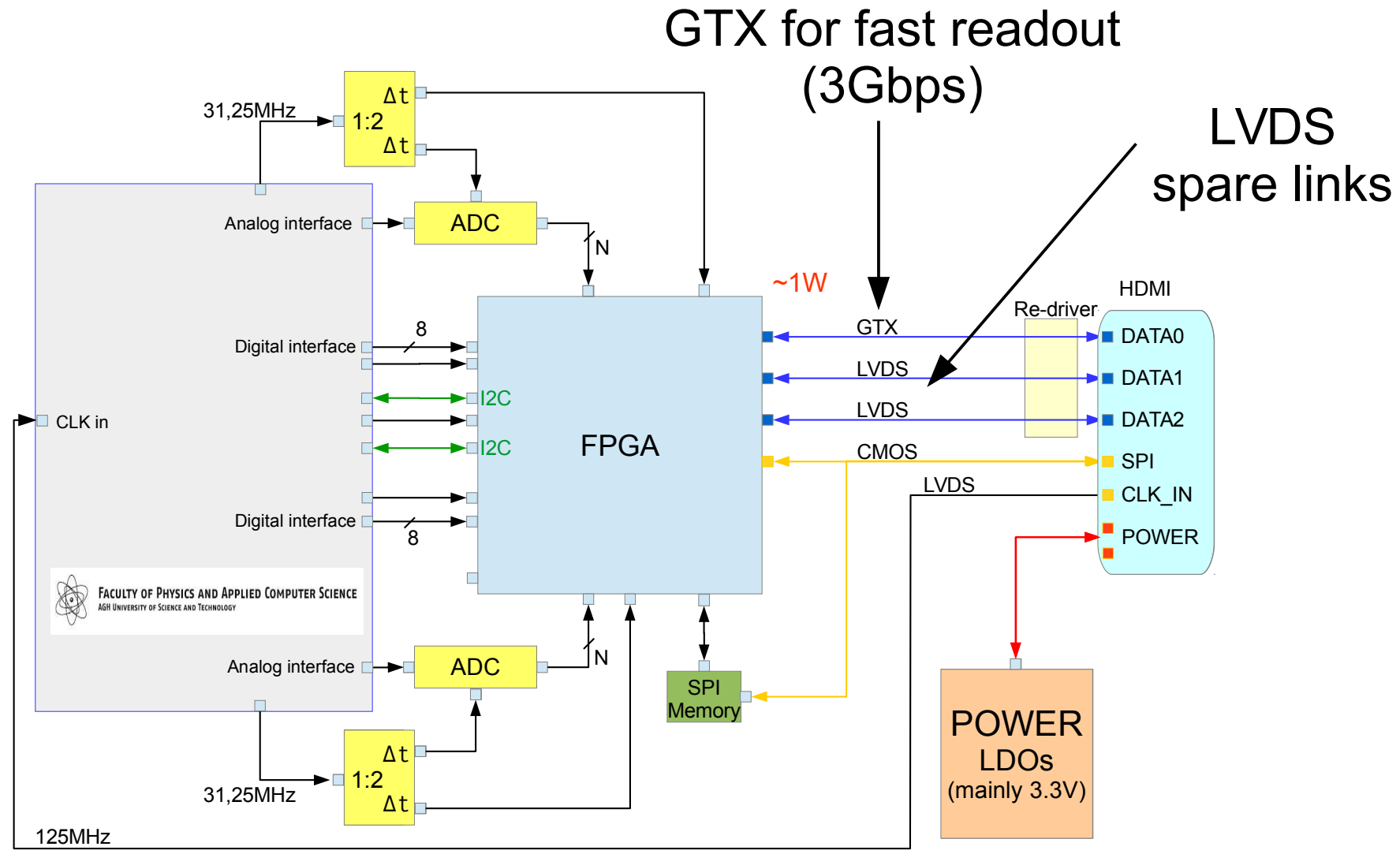
GEMROC – Hybrid – ATCA-SRS

Eraldo & Hans

reuse of the existing hybrid from AGH



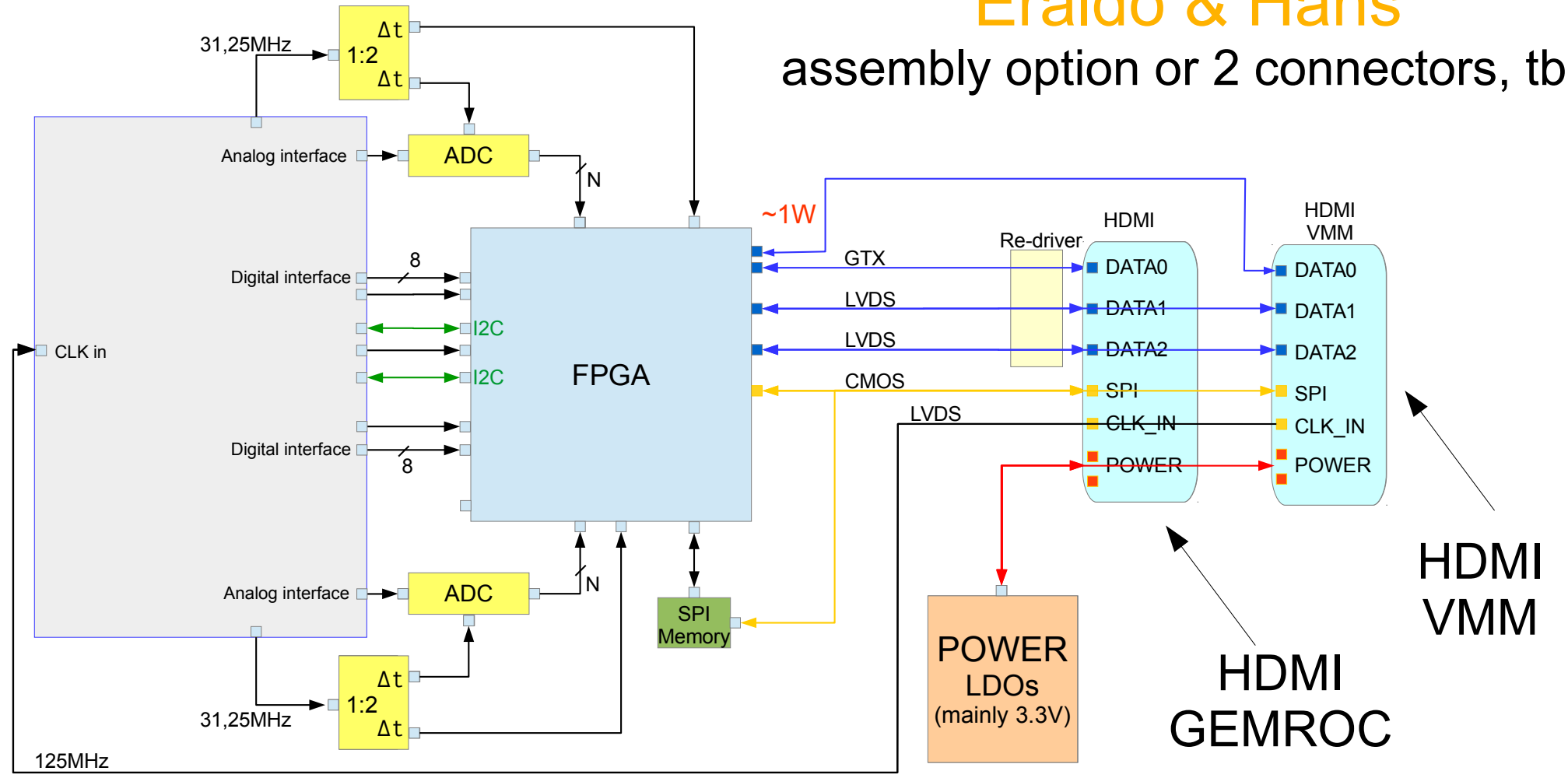
GEMROC – Hybrid – ATCA-SRS an intermediate solution



GEMROC – Hybrid – ATCA-SRS an intermediate solution

Eraldo & Hans

assembly option or 2 connectors, tbd



GEMROC – Hybrid – ATCA-SRS
VMM interface

HDMI-MICRO D	HDMI-standard A	SRS	SRS	SRS
hybrid side	SRS adapter side	VMM2	APV	Beetle
		chiplink	chiplink	chiplink
1	19	Power2a	SCL_B	TGOUT
2	14	Power2b	SDA_B	TGOUT*
3	1	DOUT0_P	AOUT0	AOUTA
4	2	VSS/G	VSS/G	VSS/G
5	3	DOUT0_N	AOUT0*	AOUTA*
6	4	DOUT1_P	AOUT1	AOUTB
7	5	VSS/G	VSS/G	VSS/G
8	6	DOUT1_N	AOUT1*	AOUTB*
9	7	TRG_P	TRGIN	TRGIN
10	8	VSS/G	VSS/G	VSS/G
11	9	TRG_N	TRGIN*	TRGIN*
12	10	CLK_P	BCLK	BCLK
13	11	VSS/G	VSS/G	VSS/G
14	12	CLK_N	BCLK*	BCLK*
15	13	RST_N	RST*	RST*
16	17	VSS/G	VSS/G	VSS/G
17	15	SCL	SCL_C	SCL_C
18	16	SDA	SDA_C	SDA_C
19	18	Power 1	P3V3/G	5V
SHELL	Shell	VSS/Ground	VSS/Ground	VSS/Ground

Chip power P2 (Voltage adjustable)

Uplink data-0 400 Mbps LVDS

Uplink data-1 400 Mbps LVDS

Downlink trigg/ config 400 MHz LVDS

Downlink link clock 40 MHz LVDS

RESET

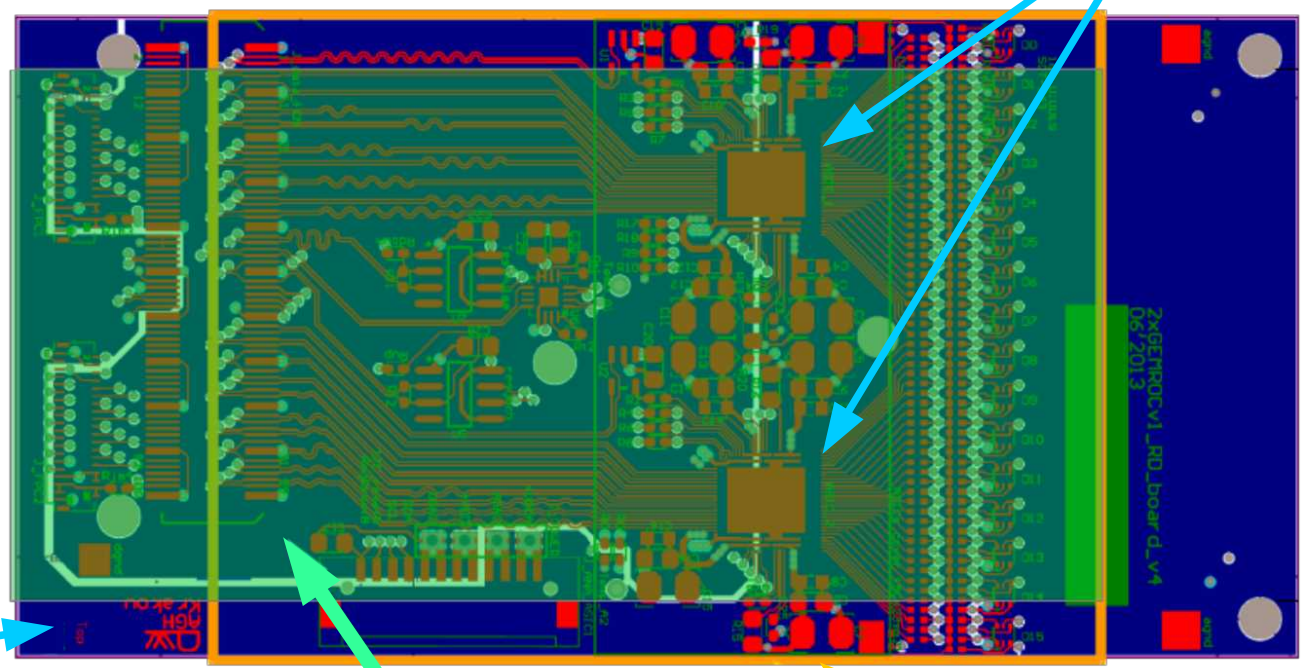
I2C

FPGA power P1 (Voltage fixed 3V3)

GEMROC – Hybrid – ATCA-SRS space on PCB

GEMROC is smaller then VMM.

There is enough space for FPGA, LODs, connector, clock distribution, etc.



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GEMROC – Hybrid

- use mainly 3.3V

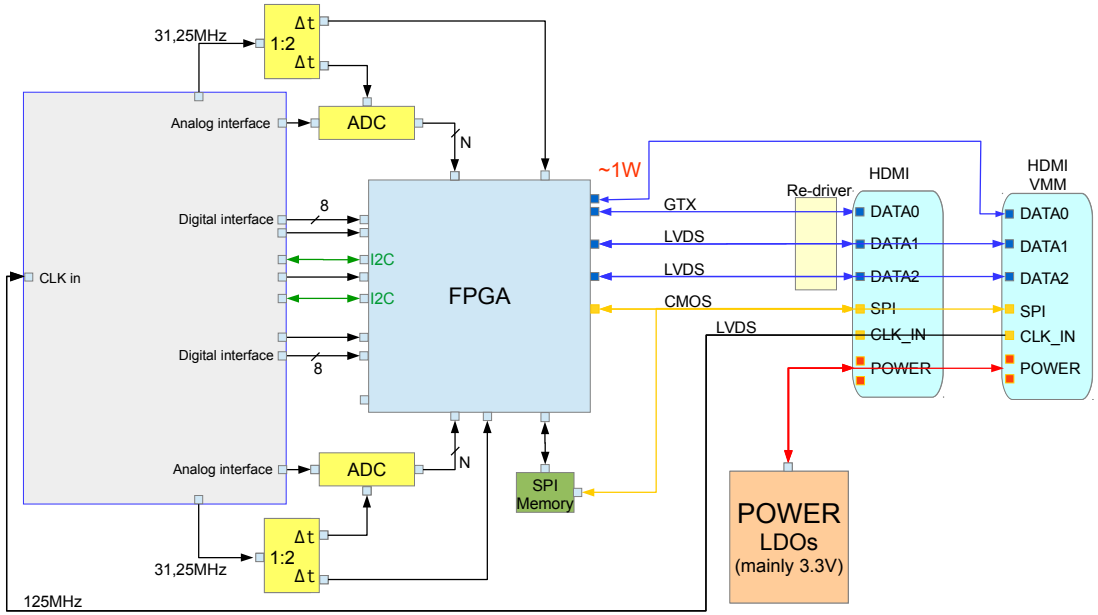
- MGT and LVDS for data transfer (pre-emphasis & de-emphasis)

- ADCs need lower power, e.g. AD9649 (~60mW)

- hybrid control over SPI

- remote firmware upgrade (SPI)

- all unused pins in hdmi connector for power (GEMROC version, VMM according to spec)



SRS ATCA – mezzanine module for GEMROC

Mezzanine:

- power regulators

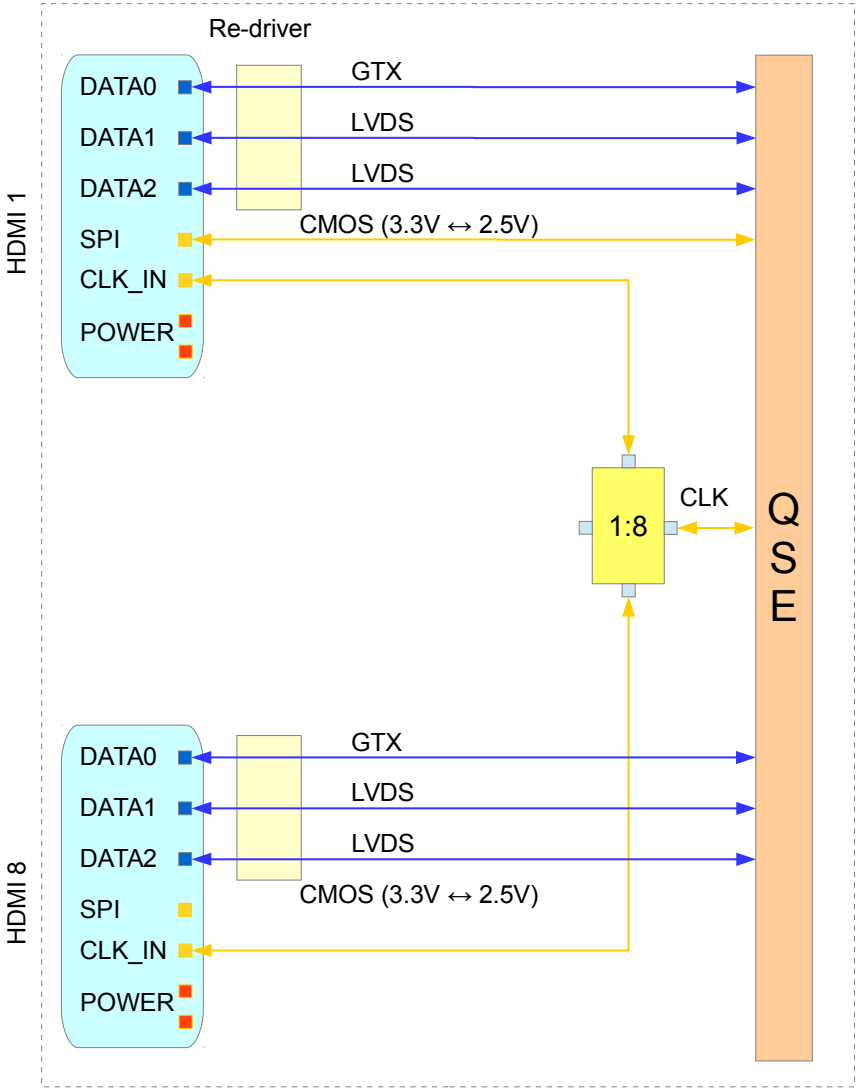
- clock distribution

- hybrid control (SPI)

- Re-drivers for data lines

- 8 x HDMI (8 GTX available on mezzanine)

- ready for GEMROC and VMM



SRS ATCA – GEMROC -Firmware

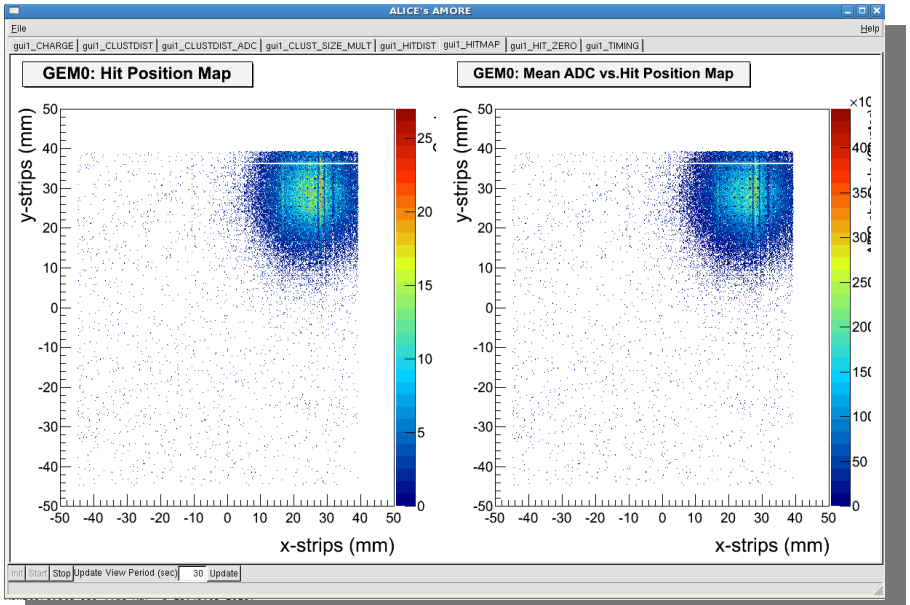
The goal:

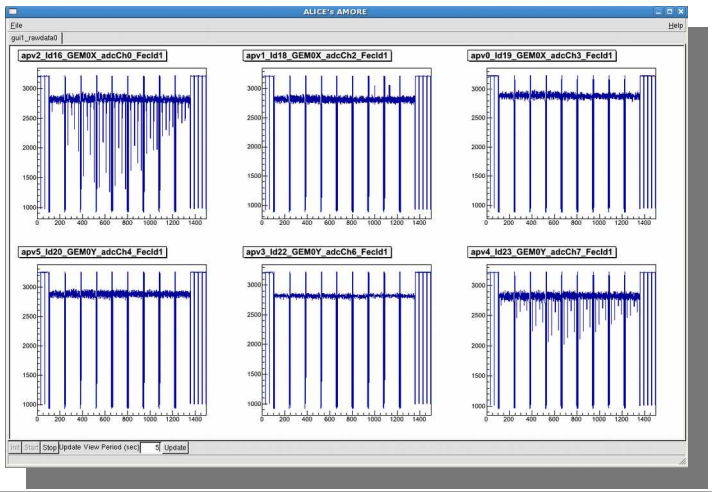
There will be no difference from point of view higher level application (Amore/DATE) – FPGA firmware will convert data to “standard” format.

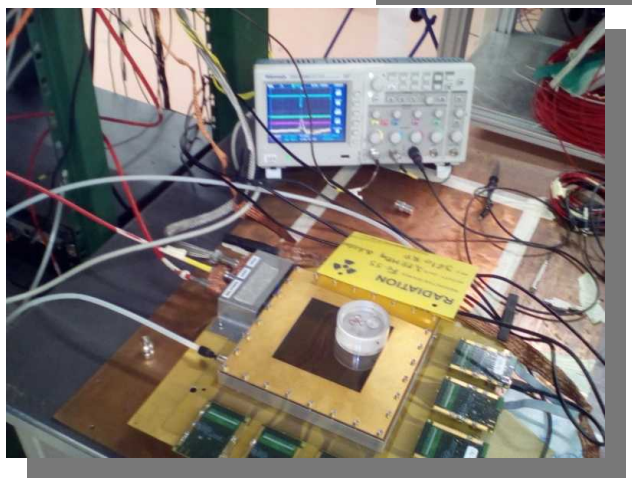
The same tools and data format between user application and hardware

SRS ATCA – Firmware

- FECv6 firmware was ported to ATCA







SRS ATCA – Firmware

- JUMBO frames not supported at the moment (needs investigation)
- External trigger problem exists - it is registered several times
- Interfacing to DATE/Amore and mmDAQ was successfully tested - frame format and interface is compatible with existing software
- Corrected firmware will be prepared in the coming week
- IPMC modules are ready and are being extensively tested.

Thank you for attention!