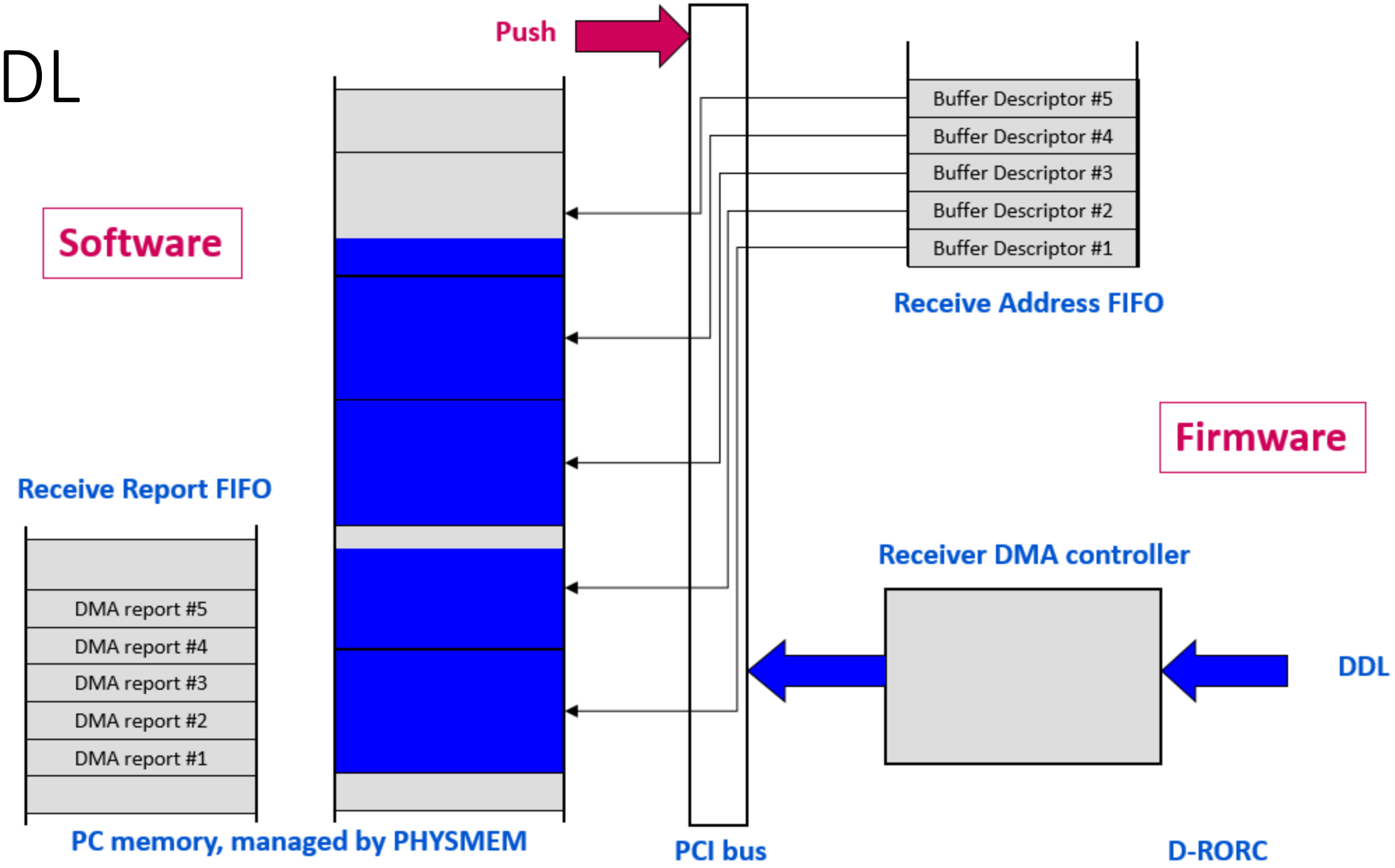
CRU buffer structure

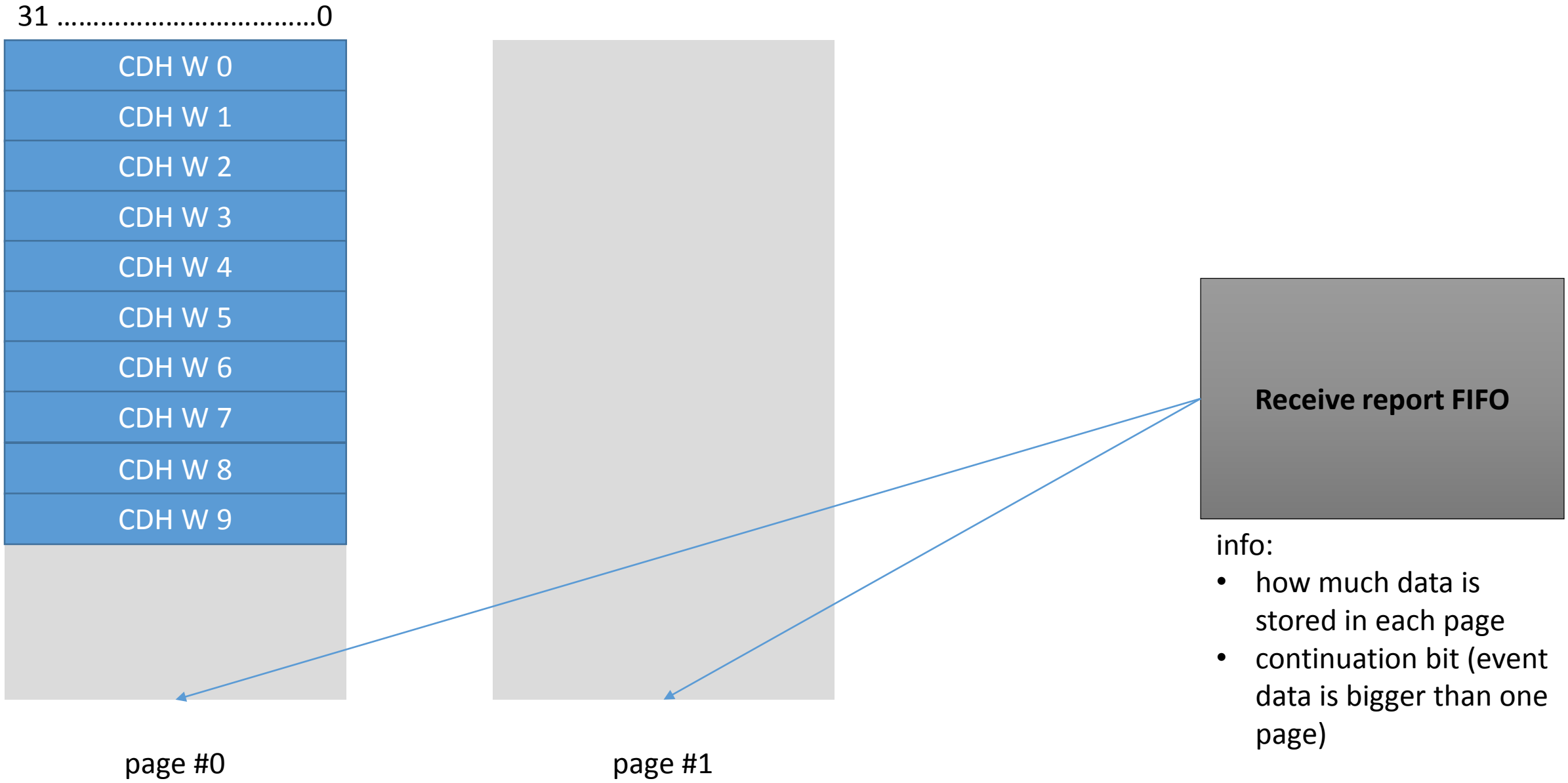
2 type of buffers

- C-RORC DDL
  - the DDL will be used during RUN3 so the software must treat data coming from DDL (CHD v3 + payload)
- CRU
  - the data coming from GBT is not defined yet, but it will be similar to what is available in the DDL (SDH + payload)

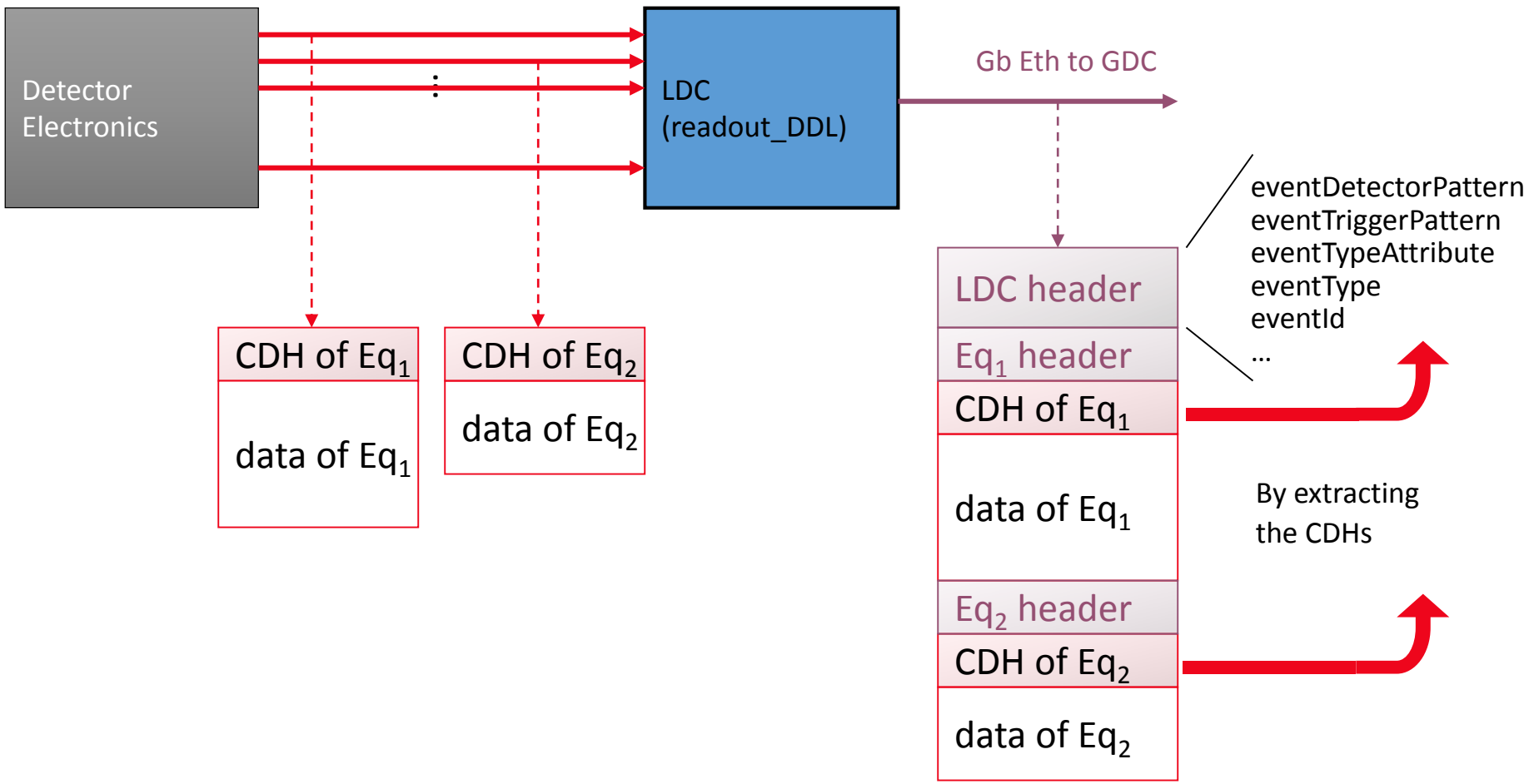
DDL


Push
Software
Buffer Descriptor #5
Buffer Descriptor #4
Buffer Descriptor #3
Buffer Descriptor #2
Buffer Descriptor #1
Receive Address FIFO
Firmware
Receive Report FIFO
Receiver DMA controller
DMA report #5
DMA report #4
DMA report #3
DMA report #2
DMA report #1
DDL
PC memory, managed by PHYSMEM
PCI bus
D-RORC

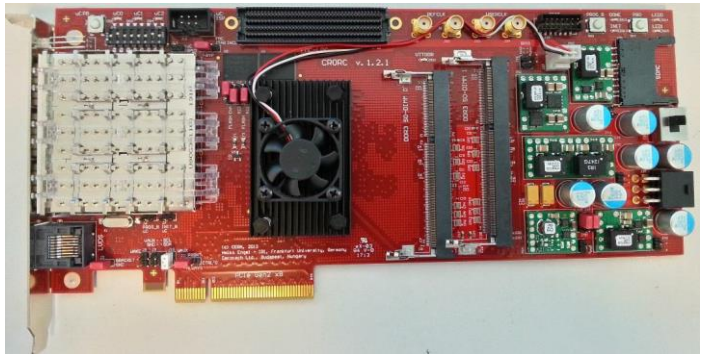
DDL BUFFER structure



DDL


Detector Electronics
LDC (readout_DDL)
Gb Eth to GDC
CDH of Eq1
data of Eq1
CDH of Eq2
data of Eq2
LDC header
Eq1 header
CDH of Eq1
data of Eq1
Eq2 header
CDH of Eq2
data of Eq2
eventDetectorPattern
eventTriggerPattern
eventTypeAttribute
eventType
eventId
...
By extracting the CDHs

DDL how it looks like in memory
(1 DMA ch per DDL)



RORC DRIVER
+
READOUT

DDL CH0

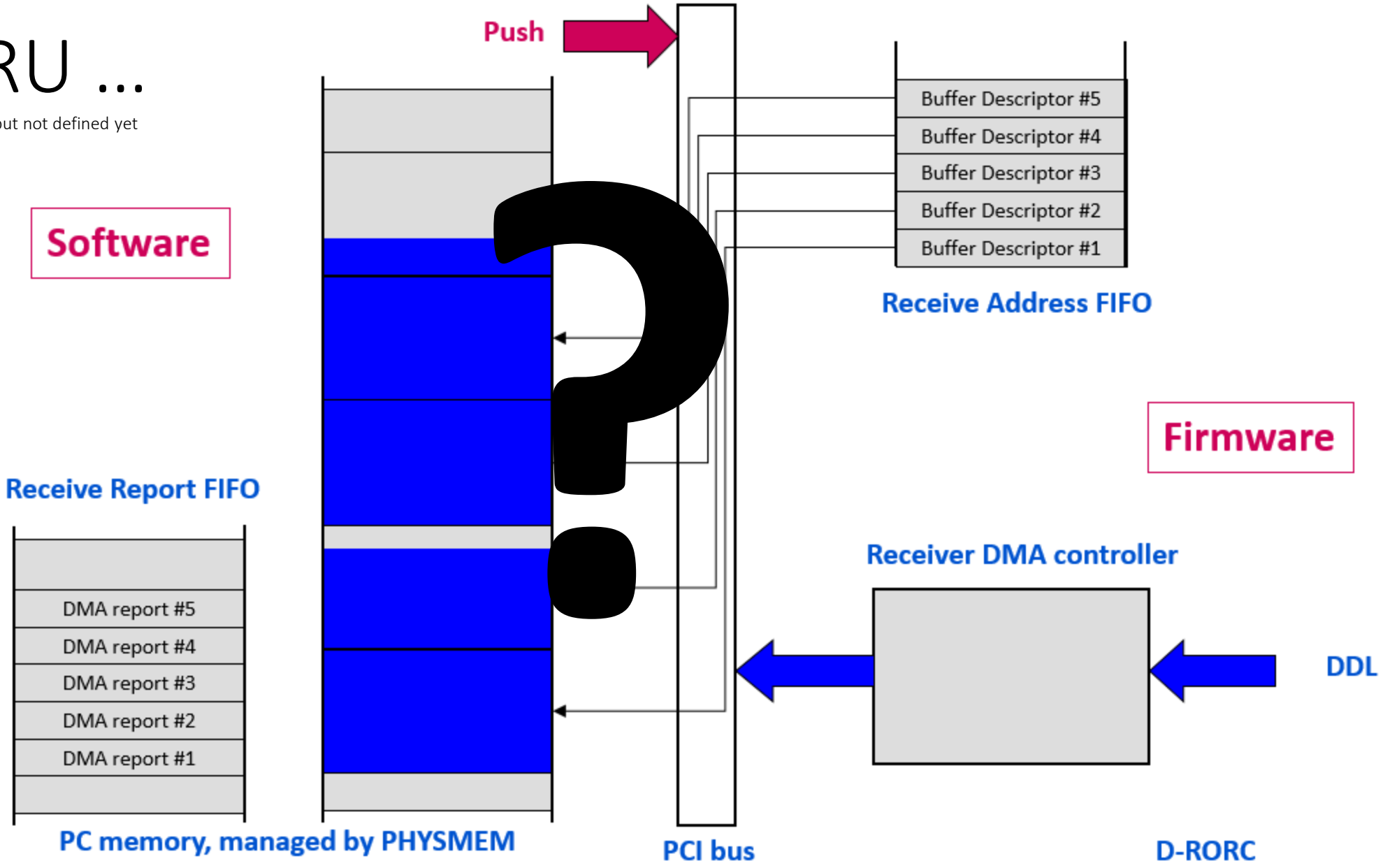
DDL CH1

DDL CH2

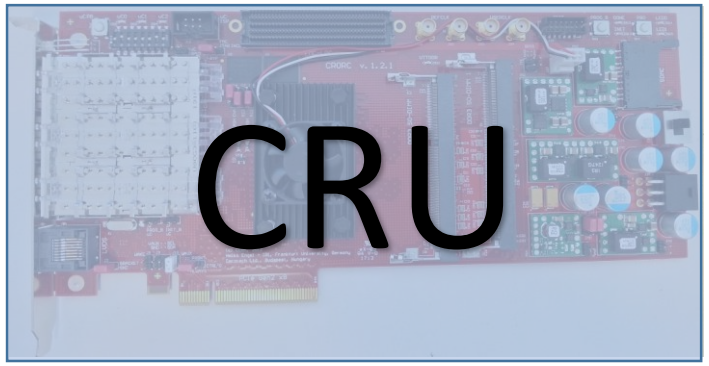
DDL CH3

CRU …

similar, but not defined yet



CRU how it could look like in memory (1)
(1 DMA ch)



CRU DRIVER
+
READOUT

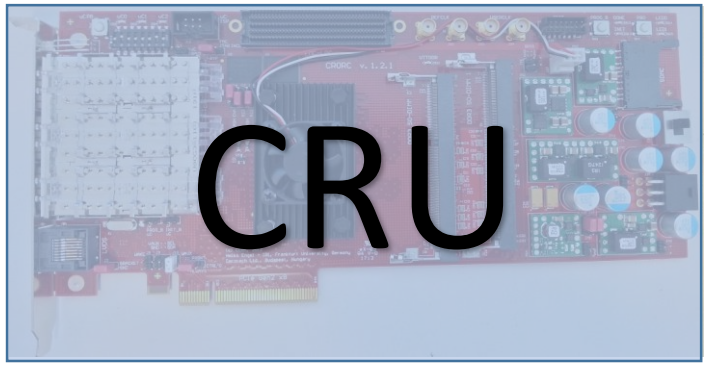
GBT CH0

GBT CH1

GBT CH2

GBT CH3

CRU how it could look like in memory (2)
(1 DMA ch)



CRU DRIVER
+
READOUT

GBT CH0	GBT CH1	GBT CH0	GBT CH2
GBT CH3	GBT CH4	GBT CH1	GBT CH2

.
.
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CRU BUFFER structure (?)