TWEPP-09 Topical Workshop on Electronics for Particle Physics

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Book of Abstracts

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Plenary Session 6 - Programmable Logic, Boards, Crates and Systems / 3

A flash high-precision Time-to-Digital Converter implemented in FPGA technology

Authors: Salvatore Loffredo[1]; paolo branchini[1]

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Time to Digital Converters (TDCs) are often required in many applications in High Energy and Nuclear Physics. Furthermore, they have been widely used in many scientific equipments such as Time-Of-Flight (TOF) spectrometers and distance measurements. Different configurations of tapped delay lines are widely used to measure sub-nanosecond time intervals both in ASIC and FPGA devices. However, the design process of an ASIC device can be expensive, especially if produced in small quantities, while FPGAs lower the development cost and offer high design flexibility. Rapid progress in FPGA electronics technology allowed achieving a time resolution values in between 50 ps and 500 ps .
The architecture used in this paper beside being dead time is multi-hit and allows for a resolution of about 35 psec. We'll show in this paper its performance in terms of resolution, integral and differential non linearity

Summary:

The construction and design process of a high-resolution time-interval measuring system implemented in a SRAM-based FPGA device is discussed in this paper.
A flash architecture has been implemented. The architecture used is dead time free.
Pulses with a jiitter less than 0.5 psec between the start and stop signal have been generated over a time interval of 20 musec.
In this way we have measured a resolution on the time interval better than 35 psec on every single measurement.
The results of the device built in terms of resolution differential and integral non-linearity are shown in this paper.

POSTERS SESSION / 4

Commissioning of the CSC Level 1 Trigger Optical Links at CMS

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The Endcap Muon (EMU) Cathode Strip Chamber (CSC) sub-detector at the CMS experiment at CERN has been fully installed and operational since summer of 2008. The system of 180 optical links connects the middle and upper levels of the CSC Level 1 Trigger chain. Design and commissioning of all optical links presents several challenges, including reliable clock distribution, link synchronization and alignment, status monitoring and system testing. We gained a lot of experience conducting various tests, participating in local and global cosmic runs and initial stage of the LHC operation. In this paper we present our hardware, firmware and software solutions and first results of the optical link commissioning.

POSTERS SESSION / 5

Simple parallel stream to serial stream converter for Active Pixel Sensor readout.

Author: Vasilii Kushpil[1]

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This paper describes a new electronics module for converting a parallel data flow to a serial stream in the USB 2.0 High Speed protocol. The system provides a connection between a PC USB port and a parallel interface of the DAQ board, which is used for investigation of performance of Active Pixel Sensors (APS) prototypes. The DAQ readout software supports Win XX OS and Linux OS. GUI examples have been prepared in the Lab Windows and Lab View environments. The module that was designed using virtual peripheral concept can be easily adapted for many similar tasks.

Summary:

The Active Pixel Sensor (APS) detectors are widely investigated for application in HEP. Parallel data channel (about 60Mbytes per seconds) is usually used for readout information from APS. Special PC parallel port card or similar solution in VME standard are used in this case. DAQ for this case is heavy and difficult for manipulation. More flexible solution, simple 16 bit parallel to USB2 stream converter is described in this paper. It allows readout with rate about 48Mbytes per second and it can be easy adapted for many different readout architectures and can run on different OS (Win XP, Linux). Flexibility of converter is reached by using virtual periphery concept for design, fastest 8-bits micro controller SX20 from UBICOM and Quick-USB module from BITWISE. The DAQ of APS can be connected to portable computer using this converter and moreover the converter also allows to use the same HW and SW for different OS. Examples of code used for readout of APS are prepared for C++, Lab View and Lab Windows and can be download from author Web page. The hardware description, Gerber files and firmware for converter can be downloaded too.

POSTERS SESSION / 6

A facility and a web application for real-time monitoring of the TTC backbone status

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Co-authors: Markus Joos [1]; Sophie Baron [1]

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The Timing Trigger and Control (TTC) system distributes timing signals from the LHC Radio Frequency (RF) source to the four experiments. A copy of these signals is also transmitted to a monitoring system, installed in the Control Center in Prevessin, which provides continuous measurement of parameters such as Bunch Clock jitter and frequency, Orbit period in BC counts, transmission delay over fiber versus temperature. A web application has been designed to ensure real time remote monitoring and post-mortem analysis of these data.
The paper discusses the architecture of the monitoring system including measurement setup as well as different concerns of data acquisition, storage and visualization.

Summary:

As a distribution of synchronous timing signals for the LHC and experiments is of great importance, there has been a need for CERN TTC backbone global monitoring system with a real time and post-mortem analysis facility.

The designed system is mostly based on the measurement equipment installed in the Rack zone of the CERN Control Center (CCR) in Prevessin site. However as the RF timing signals have to reach different

destinations, it is necessary that they are monitored all the way from their sources in Echenevex, through CCR, where they are retransmitted, and down to all the four experiments.
Data Interchange Protocol (DIP) is used to send status of monitored signals from different places around CERN sites. The status of RF/TTC receivers is first published to DIP and then collected and stored in a database for the post-mortem analysis.

The monitoring system in CCR is based on a copy of the TTC receiver crate of the experiments (basically a VME crate equipped with a VP110 crate controller connected to the Technical Network (TN), RF_Rx optical receivers, ECL fanouts and an RF2TTC board). Two oscilloscopes are installed to analyze the quality of the timing signals, together with three frequency meters using the 10MHz GMT clock for precise frequency tracking.

Among the measured and monitored values, the TTC monitoring system will focus on bunch clock and orbit frequency and synchronization, as well as jitter and temperature drift. These values are complemented with Beam Synchronous Timing (BST) system modes and status.

The main computer server responsible for data gathering is installed in CCR. While having to deal with data acquisition from all the monitoring devices and signal sources, it has also to comply with the existing CERN infrastructure and available services. This includes security restrictions that are enforced on data transmission between Technical Network (TN) and General Public Network (GPN), database access and other.

A web based application will provide fast data visualization means to the LHC experiments, in order to monitor the TTC status in real time. This application will be available to the users and will help them to quickly detect unexpected conditions and cross correlate those with other events. As all the data will be time-stamped and stored in a database, data analysis and post-mortem will also be simplified.

The paper discusses the architecture of the monitoring system including measurement setup as well as different concerns of data acquisition, storage and visualization.

Parallel Session B5 - Optoelectronics and Links / 7

Radiation Hardness of Graded-index Optical Fibre in Sub-Zero Temperature Environments

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Co-authors: Cigdem Issever [1]; Tony Weidberg [1]

[1] *Oxford University*

Optical fibres experience significant differences in Radiation induced absorption (RIA) depending upon the temperature environment. At the LHC upgrade there are plans in some cases to mount optical fibres on or near to cold surfaces at sub-zero temperatures. Consequently a programme of characterization of optical fibre's RIA in cold environments is essential for identification of acceptable components and qualification of the final data links.

We report temperature dependent radiation induced absorption from cold tests of optical fibres which are candidates for a future high energy physics detector. The optical fibre was exposed to ionizing radiation at -20 deg. C.

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Optical fibres experience significant differences in Radiation induced absorption (RIA) depending upon the temperature environment. At the LHC upgrade there are plans in some cases to mount optical fibres on or near to cold surfaces at sub-zero temperatures. Consequently a programme of characterization of optical fibre's RIA in cold environments is essential for identification of acceptable components and qualification of the final data links.

We report temperature dependent radiation induced absorption from cold tests of optical fibres which are candidates for the future ATLAS and CMS detectors at the LHC. The optical fibre was exposed to ionizing radiation at -20 deg. C.

Parallel session A4 - Trigger / 9

The GCT µTCA Matrix Card and its Applications

Author: John Jones[1]

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The Matrix card is the first in what is expected to be a series of xTCA cards produced for a variety of projects at CERN, Trieste and LANL. Developed as a joint collaboration between colleagues at Princeton, Imperial College, LANL and CERN, the device comprises the latest generation of readily-available Xilinx FPGAs, crosspoint-switch technology and optical links in a 3U form factor. In this presentation we will discuss the development and test results of the Matrix card, followed by some of the tasks to which it is being applied.

Summary:

The Matrix card was originally designed as part of the CMS GCT Muon and Quiet Bit system. As such it was developed to provide a combination of reconfigurable optical links and firmware that can be adapted to different tasks without the redesign of the hardware itself. In addition to this, the board includes a microcontroller for host management and DDR memory.

In this presentation we will discuss the board's design in detail, and the prototype testing of the various systems on board . This includes the infrastructure required to control the board (based on 10/100Mb Ethernet). The I/O and computing performance of the Matrix card have been studied in detail and the results of these studies will also be presented and discussed.

Since the production of the original design, the board has been used by a number of projects, such as the LLRF control system for the FERMI free electron laser at Trieste, the calorimeter trigger upgrade at CMS. In the FERMI project, the Matrix card provides a central control point for the RF system, as well as a centralized timing and control system. For the calorimeter trigger, its flexibility allows for changes in the algorithms without modification of the basic hardware. These different applications will be briefly reviewed.

POSTERS SESSION / 10

CMD-3 First Level Trigger Infrastructure

Author: Alexey Kozyrev[1]

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The cryogenic magnetic detector CMD-3 developed for experiments on elektron-pozitronnom collider VEPP-2000 is under construction at Budker Institute of Nuclear Physics now. This paper describes the modules which are forming an infrastructure and datapath of the First Level Trigger (FLT) of CMD-3. There are few types of modules specially developed for detector subsystems. These modules are intended for data gathering and processing of arguments of FLT, support of testing and precision calibration of FLT efficiency. The special attention is devoted to transmission synchronization of data pipelining, FLT reliability and efficiency on-line checks.

Summary:

The CMD-3 detector is now under construction at Budker Institute of Nuclear Physics. The detector includes a magnetic spectrometer and electromagnetic calorimeter. In this paper the modules forming an infrastructure First Level Trigger (FLT) of CMD-3 are described.
Modules of the Interface of the First Level Trigger (IFLT) Drift and Z the chambers, focused on interaction with information payments in the environment of Data Acquisition System (DAQ) CMD-3 are described. One of feature of CMD-3 FLT is using standard CAMAC bus lines for arguments gathering. The collected data are processed to arguments of the First Level Trigger (FLT) and transferred by the fast serial channel with standard LVDS level ("fast link"). The module is produced and tested with Drift chamber, and the full performances are achieved.
It is described Amplitude Discriminators and the Adder (ADAM) which is interface for FLT of calorimeters. ADIS accept analogue signals of calorimeters and then produce this to logic signals - arguments for FLT. The module contains A/D converter and digital processing logic, and "fast link" for transfer of arguments to FLT. The module is produced and tested with CsI calorimeter. Good performance is shown, but addition software development is required.
The special attention is devoted to transmission synchronization of data pipelining, FLT reliability and efficiency on-line checks. Possibility of imitation of events for check of efficiency FLT is provided.

POSTERS SESSION / 11

A low-cost multi-channel analogue signal generator

Authors: Felix Müller[1]; Klaus Schmitt[1]; Rainer Stamen[1]; Wei Shen[1]

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A scalable multi-channel analogue signal generator is presented. It uses a commercial low-cost graphics card with multiple outputs in a standard PC as signal source. Each color signal serves as independent channel to generate an analogue signal. A custom-built external PCB was developed to adjust the graphics card output voltage levels for a specific task, which needed differential signals. The system furthermore comprises a software package to program the signal shape.
The signal generator was successfully used as independent test bed for the ATLAS Level-1 Trigger Pre-Processor, providing up to 16 analogue signals.

Summary:

The presented signal generator provides up to 12 independent analogue signals on a low-cost basis. It consists of a standard PC hosting a commercial multi-monitor graphics card that acts as source for the analogue signals. It furthermore comprises a software package to program the signal and an external device for conditioning of the signal.

Each color channel of the graphics card serves as independent signal source. It is an unipolar signal with an 8-bit resolution of the output voltage at a time resolution ("pixel clock") of up to 5ns. This can be considered sufficient to represent an analogue signal for systems operated at a lower speed, like e.g. many 40MHz systems at the LHC.
The signal is represented by a fixed image consisting of three signals at a time (red, green, blue). The longest possible continuous signal is in the order of 10us, which corresponds to one line on the screen. The total signal length is up to 10ms, the minimal frequency about 100Hz ("monitor frequency").
It is an intrinsic effect of the graphics card that the signal features a blanking space at the end of each line and each screen, where the electrical output is zero. This typically takes 20% of the total time.
In order to maximize the number of channels, graphics cards with multiple monitor outputs were tested, from which the model with the best electric properties was chosen.

A software package was developed to program and create the signals. A graphical tool offers basic pulse shapes and the possibility to import external data. It stores pulse shapes in a generic file format. Three signals are merged into a fixed image which at the output correspond to the desired signal shape. Thus the program drives the graphics card, using a dedicated linux X window server.

An external device was developed to condition the output signal to the voltage levels for a specific task. It is a PCB that consists of several buffer stages to calibrate for gain and offset. Up to six monitor outputs can serve as inputs. One channel is explicitly used to apply a global offset on all other signals in order to also allow negative signals. The output are 16 differential signals, which can be configured by an upstream fan-out stage.

The signal generator was used in a test bed for the analogue parts of the ATLAS Level-1 Calorimeter Trigger Pre-Processor in a setup with 8 independent channels that are fanned out and converted to 16 differential signals. An additional device was developed to provide a clock synchronous to the 16 channels on the basis of another dedicated channel of the graphics card. It uses a PLL to bridge the intrinsic blanking space of the graphics card signal.

The presented signal generator is applicable in all fields with need for multiple analogue signals where a blanking space is no drawback, or can be compensated as shown. The advantages are multiple, easily programmable signals with acceptable quality at very low expenses.

Parallel session B1 - Systems, Installation and Commissioning / 12

Commissioning and performance of the Preshower off-detector readout electronics in the CMS experiment

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The CMS Preshower is a fine grain detector that comprises 4288 silicon sensors, each containing 32 strips. The raw data are transferred from the detector to the counting room via 1208 optical fibres producing a total data flow of ~72GB/s. For their readout, 40 multi-FPGA 9U VME readout boards are used. This article is focused on the commissioning of the VME readout system using two tools: a custom connectivity test system based on FPGA embedded logic analyzers read out through JTAG; an FPGA-based system that emulates the data-traffic from the detector. Additionally, the performance of the VME readout system in the CMS experiment, including the 2009 CRAFT run (Cosmic ray at Four Tesla), is discussed.

Summary:

The CMS Preshower is a fine grain detector that comprises 4288 silicon sensors, each containing 32 strips. The raw data are transferred from the detector to the counting room via 1208 optical fibres producing a total data flow of ~72GB/s. For their readout, 40 multi-FPGA 9U VME readout boards known as “ESDCC” have been produced. The ESDCCs also perform significant data reduction since the the total available downstream bandwidth of the central DAQ system is ~8GB/s. The required level of data reduction is feasible since the maximum occupancy is relatively low in the Preshower - an average of about 2%. This article is focused on the commissioning of the VME readout system as well as its performance in the CMS experiment.

The first stage of commissioning of the system was the connectivity test of the major FPGA-based components comprising the ESDCC: up to 3 multi-channel optical receiving plug-in modules (known as the “optoRx”) and their 9U VME “host board”. The tool used to verify the connections is a custom connectivity test system based on FPGA embedded logic analyzers. The concept of the testing method is

the following: In order to verify one connection line, the line must be toggled from the one end and read/verified on the other end. To do so, one or more FPGAs of the unit under test are generating certain patterns that are received by other FPGAs of the same unit. In case of open connections (e.g. from an FPGA to a connector), special PCBs are attached to the connectors and redirect the signals to other FPGA IO lines. The patterns are triggering the embedded logic analyzers in the receiving end, being recorded and readout through JTAG. A LabVIEW application that compares the expected results with the ones received from the unit under test as well as presents the pin locations of the faulty connections has also been developed.

By combining existing modules, a second FPGA-based test system known as the "ESDTE" (Preshower Data Traffic Emulator) has been developed. This serves as the primary ESDCC evaluation tool in the laboratory. As its name suggests, the ESDTE emulates the front-end of the Preshower, providing user-programmable data patterns combined (or not) with real previously recorded data from the detector. The ESDCC can thus be commissioned without the need for the real detector hardware as a data source. In addition, the ESDTE is able to generate rare (but possible) error conditions that are not easily reproducible with the real detector, such as synchronization problems, missing or spurious events, corrupted data packets etc. Flexible software tools have been developed to accompany this hardware, enabling easy control of both the ESDTE and ESDCC (C++ programs) as well as the subsequent data analysis (based on MatLab).

The last part of the article is focused in the performance of the ESDCC in realistic conditions, both during detector assembly and in-situ in CMS, including the 2009 "CRAFT" run (Cosmic Rays At Four Tesla). The maximum event rates with and without data reduction, the data reduction factor achieved, synchronicity issues, time needed for the loading of operating parameters, time needed for the FPGA configuration through VME, operating temperatures etc. are all discussed.

Parallel session A4 - Trigger / 13

Design of a module providing trigger information from the CMS Tracker at SLHC

Author: Geoff Hall[1]

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The CMS experiment is planning a major upgrade of its tracking system to adapt to an expected increase in luminosity of the LHC accelerator to 1035 cm-2.s-1. The CMS Tracker will then have to cope with several hundred interactions per bunch crossing and fluxes of thousands of charged particles emerging from collisions.
CMS requires tracker data to contribute to the first level trigger, which must maintain the present 100kHz rate for compatibility with existing sub-detector systems while increasing the trigger decision latency by only a few μs. It must be achieved if possible without significantly compromising the tracking performance which is very sensitive to the material budget. A key part of a system to achieve this will be the design of a suitable module to generate trigger primitives.
A module which might allow to provide suitable track trigger primitives is described and implications for the system are discussed.

Summary:

The CMS experiment is planning a major upgrade of its tracking system for the SLHC, to adapt to the expected increase in luminosity of the LHC machine to 1035 cm-2.s-1. The CMS Tracker will then have to cope with several hundred interactions per bunch crossing and fluxes of thousands of charged particles emerging from the 40MHz collisions.
CMS has identified a requirement to provide tracker data to contribute to the first level trigger, which must maintain the present 100kHz maximum rate for compatibility with existing sub-detector systems while increasing the trigger decision latency by only a few μs. This must be achieved if possible without significantly compromising the performance for tracking, which is expected to be very sensitive to the material budget, in a much more demanding environment than LHC. It is therefore important that the overall tracker system be designed to provide trigger information with as low power as possible, and a

system architecture must be developed which can achieve this.
One possible solution is based on so-called “stacked tracker modules” using closely spaced sensor layers. Such layers would be situated at intermediate radius within the tracker volume to ensure complete coverage of the maximum range of pseudorapidity. The sensors would be coarsely pixellated units, with typical dimensions of 2.5mm x 100μm so that a typical stacked layer would contain ~40million elements. The pattern of hits in each layer is compared to identify high pT track candidates. Simulations have been carried out which support the basic concept and allow to define suitable modules which could implement the required features. Spacings of 1-2mm between the layers should allow to reject low transverse momentum tracks, with a typical threshold of a few GeV/c and efficiency close to 100% for momenta above threshold
A basic readout architecture is proposed and the electronic implications are described, including an outline design of the readout ASIC, the combinatorial logic, and other components as well possible means to construct suitable modules using accessible manufacturing technologies, which should use advanced but inexpensive interconnection techniques to achieve adequate density. In this scheme, the power consumption is strongly influenced by the means by which data from the two layers within a stacked module are brought into coincidence, and it is essential to minimise the data traffic within the module. The largest contribution to the total power budget comes from data transmission from the tracker to the off-detector system where the first level trigger processing is carried out, so it is essential to deploy the tracker data in a very economical way.
Estimates of likely power consumption will be given, as well as data rates and link bandwidth requirements, and possible implications for the implementation of the trigger. These results will determine what type of system is affordable, both in terms of power consumption and financial cost.

Parallel session A1 - ASICs / 14

About 10000 frames per second readout MAPS for the EUDET beam telescope

Author: Christine HU-GUO[1]

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Designed and manufactured in a commercial CMOS 0.35 μm Opto process for equipping the EUDET beam telescope, MIMOSA-26 is the first reticule size pixel sensor with digital output and integrated zero suppression. It features a matrix of pixels of 576 rows and 1152 columns covering an active area of ~224 mm2. A single point resolution, better than 4 μm, is expected with a pixel pitch of 18.4 μm. Its architecture allows a fast readout frequency of ~10 k frames/s. The workshop contribution will present, in details, the chip design, test and its major characterisation outcome.

Summary:

A high resolution beam telescope, based on CMOS Monolithic Active Pixel Sensors (MAPS), is being developed within the EUDET collaboration a coordinated EU (FP 6) detector R&D program for the future International Linear Collider (ILC). The IPHC and IRFU team is involved in this Joint Research Activity (JRA) to develop a fast readout MAPS, called MIMOSA-26, for equipping the telescope. The latter will consist of 2 arms of 2x3 MAPS measurement planes, providing an extrapolated resolution better than 2 μm on the surface of the device under test.

The MIMOSA-26 architecture is based on the successful design of the two separate prototyping lines, completed with the MIMOSA-22 and SUZE-01 chips, respectively. The first line addresses the upstream part of the signal detection, analogue processing and analogue to digital conversion, while the second is dedicated to data sparsification and formatting. Combining the architectures of these two prototype circuits, MIMOSA-26 features a pixel matrix of 1152 columns and 576 rows with a pixel pitch of 18.4 μm. Each pixel hosts an N-well/P-epi charge collection diode, a preamplifier and a correlated double sampling (CDS) functionality minimizing the low frequency noise. The pixel array is read out in rolling shutter mode sweeping the array row by row. At the bottom of the pixel array, a stage of 1152 offset compensated discriminators, each one connected to a column, performs the analogue to digital conversion. The digital data are then treated by a zero suppression circuitry integrated on the same chip in order to restrict the chip output to useful information. The compressed data of a frame are buffered

alternatively in 2 SRAM allowing a continuous readout. They are then sent out during the acquisition of the next frame via one or two 100 M bits/s LVDS transmitters. The on-chip programmable biases, the voltage references and the selection of the test modes are set via a JTAG controller.

The MIMOSA-26 architecture is the outcome of a ten years long R&D activity. It is expected to be the cornerstone of the design of various CMOS pixel sensors foreseen to equip vertex detectors of several subatomic physics experiments, such as the STAR Heavy Flavour Tracker (HFT) upgrade or the CBM Micro Vertex Detector (MVD). It is also proposed for the ILC vertex detector.

MIMOSA-26 returned from foundry in February 2009. Extensive tests are going on in the laboratory; those preliminary results indicate that the sensor is likely to meet the EUDET telescope specifications. A temporal noise of 0.64 mV and a Fixed Pattern Noise (FPN) of 0.29 mV have been observed, for one quarter of the pixel array with its associated discriminators. These values are fully compatible with those obtained with MIMOSA-22. The remaining three quarters of the matrix exhibit similar performances, showing a good uniformity of the whole 576 x 1152 pixels associated to the 1152 discriminators.

Details of the MIMOSA-26 chip design and preliminary characterisation results will be presented. Possible upgrades and extensions to improve the device performances will be discussed.

Parallel session A4 - Trigger / 15

Trigger Platforms for CMS at the SLHC

Author: Gregory Michiel Iles[1]

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CERN has made public a comprehensive plan for upgrading the LHC accelerator to provide increased luminosity commonly referred to as SuperLHC (SLHC). The plan envisages two phases of upgrades during which the LHC luminosity increases gradually to reach 6-7×1034 cm-2sec-1. Over the past year CMS has responded with a series of workshops and studies which have defined the roadmap for upgrading the experiment to cope with the SLHC environment. Increased luminosity will result in increased backgrounds and challenges for CMS and a major part of the CMS upgrade plan is a new Level-1 trigger system which will be able to cope with high background environment at the SLHC. Two major CMS milestones will define the evolution of the CMS trigger upgrades: The change of the Hadronic Calorimeter electronics during phase-I and the introduction of the track trigger during phase-II. This paper outlines different alternative designs for a new trigger system. In particular, it looks at different algorithms and how they might be best implemented on different hardware platforms and the consequences for cost, latency, complexity and flexibility. The hardware platforms used to evaluate the performance of the algorithms are based on Xilinx V5 FPGAs.

Summary:

Plans are already well advanced for upgrades to the LHC machine that will provide increased luminosity. The current CMS experiment will fail to reap the full benefit of these upgrades for a number of reasons. One of these is that the current trigger system will be overwhelmed. It will not be possible to set sensible energy thresholds without the trigger rate exceeding the maximum L1A rate of 100kHz. Hence the Global Trigger would be forced to restrict the trigger rate by simply pre-scaling the trigger and thus effectively negating any benefit from increased luminosity. It is for this reason that work has started on trying to integrate a tracking trigger in a future trigger system.
This would help identify the most interesting events and bring the trigger rate back below 100kHz. A new trigger system could potentially have several others benefits such as improved flexibility because it would be based solely on FPGAs. It could also be much simpler and thus be easier to design, build

and maintain, which could have a substantial impact not just in the cost of the hardware, but also on the manpower cost to test and operate it.

The upgrade of the Hadronic Calorimeter (HCAL) electronics will precede that of the tracker and will provide lateral information of the energy depositions within the HCAL already at phase-I. An upgraded trigger system implemented at the same time as the HCAL upgrade would provide improvements to cluster based triggers such as the tau trigger while at the same time prepare the trigger to receive tracking trigger information. This will enable CMS to make more stringent isolation cuts and provide triggers of higher purity early in the upgrade program.

Consequently, the time seems ripe to begin consideration of a new trigger system that would take advantage of the latest advances in programmable technology and high speed serial interconnects. This paper outlines various alternatives for a new trigger system. In particular, it looks at different algorithms and how they might be best implemented in a real system and the consequences for cost, latency, complexity and flexibility. It also reflects on both the good and bad decisions made in the current Global Calorimeter Trigger and its predecessor.

The Optical Global Trigger Interface card (OGTI) has been designed and produced to replace the high speed serial copper links between GCT and GT. As such it represents the first upgrade to the calorimeter trigger system. It is based upon a Xilinx Virtex 5 LX110T with 16 bi-directional optical links running at up to 3.2Gb/s. It has a large parallel interface of 320 I/O in a dual CMC form factor. Results on the performance of the OGTI are presented. The optical link and FPGA technology of this card is similar to the technology that will be used at the SLHC trigger. For this reason the OPTO GTI is used here as a test platform for several of the triggering schemes and algorithms in this paper as well as for investigations in optical link technology.

To avoid reinventing the wheel in each sub system there are several areas where it might be useful cooperate. An area worthy of cooperation, or perhaps standardisation, would be on a simple high speed serial link protocol that would allow different systems to automatically lock the link to a particular latency and verify the integrity of the data. An example of this exists within the GCT and it includes a CRC check, however the protocol will be reviewed in light of experience gained over the last few years.

Parallel session A2 - ASICs / 16

Gossipo-3: a prototype of a Front-end Pixel Chip for Read-out of Micro-Pattern Gas Detectors.

Author: Vladimir Gromov[1]

Co-authors: Harry van der Graaf [1]; Ruud Kluit [1]

[1] *NIKHEF*

In a joint effort of Nikhef (Amsterdam) and University of Bonn, the Gossipo-3 IC is being developed. This circuit is a prototype of a full-reticle chip dedicated for read-out of various types of position sensitive Micro-Pattern Gas detectors.
The chip is defined as a high granulated (55um) array in which every readout pixel is equipped with a high resolution TDC (1.6ns) covering dynamic range up to 100us. This feature allows for a high precision 3D track reconstruction originated by particles passing through the gas volume.
The circuit is also optimized for low power consumption (100mW/cm^2) required to avoid the need for massive power transport and cooling systems in the construction of the detector.
In the presentation the detector principle will be explained and various design aspects of the on-pixel circuits will be discussed.

Summary:

A number of features make Micro-Pattern Gas Detectors (MPGD) attractive to be used in particle-physics experiments, astro-particle research and medical imaging. Among those are high spatial resolution, radiation hardness and inherent low material budget. The availability of highly integrated readout electronics allows for the design of gas-detector systems with channel densities comparable to that of modern

silicon detectors.
Gossipo-3 is a small-size prototype of a future ASIC dedicated for readout of MPGD's. Main specifications of such an IC will be compatible with requirements imposed upon ATLAS Pixel System for Upgraded Luminosities.
The prototype comprises a 32 by 32 active pixels readout array with a sensitive area of 3.1mm^2. The on-pixel part includes an analog-to-digital front-end circuit, a 4-bit threshold DAC and a high resolution Time-to-Digital Converter (TDC). The TDC-per-pixel architecture allows for the measurement of the drift time of individual primary electrons originated by MIP particles crossing the gas volume.
The main goal of this prototype is to optimize the design of the on-pixel circuits.
In order to be suitable for different applications (Trackers and TPC's) the readout chip has to have different functionalities and modes of operation.
In TIME mode the arrival time of the hit signal will be measured in the range from 1.6ns to 100us as well as the size of the charge deposited on the pixel in the range from 400 electrons to 30 000 electrons. We have chosen a hit signal-controlled TDC solution for digitization of the time information. In this scheme each pixel has an individual fast (Fosc≈600MHz) oscillator circuit connected to a fine time counter and a clock synchronous counter for coarse time measurements. The oscillator will be started every time the pixel is hit and will be stopped by the first leading edge of the clock signal (freq=40MHz). The clock synchronous counter gives a number of full clock periods between the Hit signal and the external Trigger signal [1].
In IMAGE mode the number of hits will be counted on each pixel in the range up to 24 bits.
Two triggering options will be available in the chip. These are external common Stop and internally generated Stop (fast OR).
In the Gossipo-3 prototype, the pixel array will be read-out serially. The output data of the pixel will be shifted out to the buffer of the adjacent pixel and thus on to the periphery. A final readout architecture will be worked out in the next prototypes.

[1] V.Gromov, R.Kluit, H. van der Graaf "Development of a Front-end Pixel chip for Readout of Micro-Pattern Gas Detectors" Proceeding of Topical Workshop on Electronics for Particle Physics (TWEPP-08), pp.76-79, Naxos, Greece, September 2008.

Parallel Session B3 - Packaging and Interconnects / 17

The First Vertically Integrated MPW Run for HEP

Author: Ray Yarema[1]

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In 2008 a consortium of 15 international institutions was formed to pursue the development of 3D integrated circuits at a commercial foundry. The first MPW run from the consortium was submitted to Tezzaron. Wafers were fabricated at Chartered Semiconductor in the 130 nm process. These wafers were then assembled by Tezzaron into vertically integrated circuits. More than fifteen designs were submitted. Designs include custom analog and digital circuits for particle detection in ATLAS, CMS, ILC and other experiments. Issues related to the submission of the MPW run and initial results will be presented.

Summary:

Interest in 3D integrated circuits for HEP has grown steadily since talks at Perugia and Ringberg in 2006. Early 3D work utilized the MIT Lincoln Lab SOI process. Based on that early work a group of international institutions has come together to explore and develop 3D integrated circuit concepts for HEP.

One of the first truly commercial processes for 3D integrated circuits is offered by Tezzaron Semiconductor. Tezzaron has been in the business of offering 3D integrated circuits for commercial customers for a number of years. Although their main business is in 3D stacked memories, they have also produced 3D chips for imaging, FPGAs, and microprocessors. Recently Tezzaron has agreed to host MPW runs

for HEP and a separate DARPA funded program. The MPW runs allow a large number of customers to explore 3D circuits using a commercial foundry at a reasonable cost.

In 2008, a consortium of 15 institutions was formed with members from France, Italy, Germany, Poland, and the United States. The consortium placed a purchase order with Tezzaron to produce vertically integrated circuits using the Chartered 130 nm low power process. The circuits have two tiers of electronics fabricated in a via first process using a single set of masks. The two tiers are bonded together using copper to copper bonding. More than fifteen circuit designs and dedicated test circuits were submitted in ten major sub reticules. Two of the designs are for ATLAS pixel upgrades that would separate analog and digital electronics on to two different tiers, allowing for higher circuit density and separate substrates for analog and digital circuits. Another design explores a new trigger concept for the CMS upgrade that uses two closely spaced sensor layers, an interposer, and separate tiers of a 3D circuit for each sensor layer. Other designs explore pixel designs for the ILC, and various MAPS designs. There are numerous test structures and circuits for evaluating the 130 nm process for radiation tolerance and viability for cryogenic operation.

The designs were completed in a relatively short period of time in part due to the sharing of designs and code developed by various members of the consortium. Thus in addition to the cost savings for chip fabrication afforded to each member by means of the MPW run, significant manpower saving was also realized. Initial test results from some of the circuits will be presented. Future MPW runs are planned. Although it is still early, both CMP and MOSIS have shown interest in our Tezzaron/Chartered MPW runs which could have significant long term benefits for HEP.

1) R. Yarema, Fermilab Initiatives in 3D Integrated Circuits and SOI Design for HEP, ILC Vertex Workshop, Ringberg Castle, Tegernsee, Germany, May 29-31, 2006

POSTERS SESSION / 18

Detector Control System for the Electromagnetic calorimeter in CMS Experiment

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Co-authors: Alexander Inyakin [2]; Angela Brett [3]; Dragoslav Jovanovic [4]; Emanuele Di Marco [5]; Francesca Cavallari [6]; Georgi Leshev [7]; Guenther Dissertori [1]; Jovan Puzovic [4]; Peter Adzic [8]; Predrag Milenovic [9]; Robert Gomez-Reino [10]; Serguei Zelepukin [7]; Thomas Punz [1]; Xavier Pons [10]

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The challenging constraints on the design of the Electromagnetic Calorimeter (ECAL) of the Compact Muon Solenoid (CMS) experiment, such as rigorous temperature and voltage stability, imposed the development of a complex Detector Control System (DCS). In this paper the final layout and functionality of the CMS ECAL DCS are presented and the operational experience during the detector's commissioning and cosmic runs is discussed.

POSTERS SESSION / 19

A Radiation Tolerant 4.8 Gb/s Serializer for the Giga-Bit Transceiver

Author: Ozgur Cobanoglu[1]

Co-authors: Federico Faccio [1]; Paulo Moreira [1]

[1] *CERN, PH-ESE-ME*

This paper describes the data serializer of the GigaBit Transceiver (GBT) which has been under development for the LHC upgrade (SLHC). The circuit operates at 4.8 Gb/s and is implemented in a commercial 130 nm CMOS technology. The serializer occupies an area of 0.6 mm² and its power consumption is 300 mW. The paper focuses on the techniques used to achieve radiation tolerance and on the simulation method used to estimate the sensitivity to SETs.

Summary:

The GBT project aims at designing a radiation tolerant optical transceiver operating at 4.8 Gb/s within the framework of the luminosity upgrade of the LHC machine and the experiments. The GBT will replace the three communication links currently in use, namely the timing, trigger and control system (TTC), the data acquisition system (DAQ) and the slow control system (SC), therefore providing a single solution for all the communication needs at the LHC.

The GBT chip set will include a radiation tolerant serializer (SER) which converts 120-bit-wide, 40 Mb/s parallel data into 4.8 Gb/s serial stream. Operating from a single 1.5 V supply with a power consumption of 300 mW and occupying an area of 0.6 mm², the circuit accepts CMOS-level data and control signals. The SER outputs a pseudo-differential signal with a worst-case simulated pattern-dependent jitter of less than 6 ps at 4.8 Gb/s.

The SER architecture is based on dividing the 120-bit frame into 3 equal sized framelets stored in separate shift-registers with a conversion rate of 40 Mb/s and multiplexing these shift registers to the output at one third of the full speed. This architecture minimizes the number of components operating at full speed.

A fully integrated programmable charge-pump phase-locked loop (CP-PLL) synthesizes an internal 4.8 GHz bit clock from the 40 MHz LHC reference. Due to strong dependency of the SER output jitter on the CP-PLL behavior, the values of the loop filter resistor and the charge-pump current are controlled by D/As having 2 and 4-bit resolution, ranging from 1.5 KOhm to 6.0 KOhm and from 1 μA to 100 μA, respectively.

The CP-PLL is designed to be tolerant to single event transients (SET) via employing custom-designed devices for higher performance and triple-well structures for better isolation. Triple modular redundancy (TMR) is as well used in the feed-back divider of the CP-PLL for mitigating the single event upsets (SEU). The design performance of interest along all the processing corners is limited to the temperature range of [-20 C°, 100 C°] and the power supply variation of pm 10%.

A GBT prototype has been designed in a commercially available 130 nm CMOS technology as a flip-chip. By the time of this writing, it is in the process of being submitted to the foundry for fabrication.

Full text focuses on the functional architecture of the SER, the techniques applied to achieve radiation tolerance and the simulation method used for estimating the circuit sensitivity to SETs.

POSTERS SESSION / 20

Novel charge sensitive amplifier design methodology suitable for large detector capacitance applications

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Alternative current mode charge sensitive amplifier (CSA) topology and related methodology for use as pre-amplification block in radiation detection read out front end IC systems is proposed. It is based on the use of a current conveyor architecture providing advantageous noise performance characteristics in comparison to the typically used CSA folded caccode structure. In the proposed architecture the CSA output noise is independent of the detector capacitance value, allowing the use of large area detectors without affecting the system noise performance. Theoretical analysis and simulation based results are confirmed by measurements on a prototype demonstrating the advantageous performance in relation to the traditional voltage mode structures mainly in terms of the noise performance dependency on the detector capacitance value.

Summary:

In charge sensitive amplifiers, the minimum charge that can be detected by the detector-preamplifier system is limited by the noise level reducing the system resolution. It is therefore greatly important to reduce the noise sources contribution. In radiation detection systems the noise is dependent on the detector capacitance value, its associated leakage current and the noise produced mainly by the preamplification block. Using the folded cascode preamplifier typical amplification scheme, the total output noise, for a large detector capacitance applications, is proportional to the detector capacitance value. While large area detectors can offer increased sensitivity, they also should be divided in pixels in order to minimise the total noise and each pixel needs its own readout circuit.
In this work we propose a current mode amplification scheme which can be used with large area detectors without affecting the noise level. This configuration is based on the use of second generation current conveyor (CCII) providing output noise independent to the detector capacitance value, allowing the use of large area detectors without affecting the system noise performance. Theoretical analysis and simulation results are confirm the operation – performance of the proposed topology. Measurement results on a current mode CSA prototype fabricated in a 0.35 μm CMOS process by AMS are provided supporting the theoretical and simulation analysis and confirming the advantageous performance in relation to the traditional voltage mode structures mainly in terms of the noise performance dependency on the detector capacitance value.

POSTERS SESSION / 21

Readout and Data Processing Electronics for the Super-Belle Silicon Vertex Detector

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A prototype readout system has been developed for the future Super-Belle Silicon Vertex Detector at the Super-KEK-B factory in Tsukuba, Japan. It will receive raw data from double-sided sensors with a total of approximately 250,000 strips read out by APV25 chips at a trigger rate of up to 30kHz and perform strip reordering, pedestal subtraction, a two-pass common mode correction and zero suppression in FPGA firmware. Moreover, the APV25 will be operated in multi-peak mode, where (typically) six samples along the shaped waveform are used for precise hit-time reconstruction which will also be implemented in FPGAs using look-up tables.

Summary:

The Belle experiment at KEK will finish in early 2010, followed by a major upgrade of both the KEK-B machine as well as the detector. The ultimate luminosity target is up to 8 x 10^35 cm^-2s^-1, or a factor of 50 higher than now. The present Belle detector and its Silicon Vertex Detector (SVD2) in particular must be completely replaced for this challenging endeavor, as its innermost layer is already at the limit in terms of occupancy and dead time. Both are related to the readout chip, which is currently a slow-shaping VA1TA with moderate readout speed and no pipeline.

The future Super-Belle SVD will be equipped with APV25 readout chips (originally developed for CMS), which feature fast shaping (50ns), a 192-cell deep pipeline and a readout speed of 40MHz. As the occupancy observed in the detector scales with the peaking time of the shaping amplifier, we get a reduction factor of ~12.5 compared to the present system. In CMS, the APV25 chips are used in so-called deconvolution mode, where a switched capacitor filter narrows the pulse down to a single clock for unambiguous association with a certain bunch crossing. This feature requires a clock-synchronous beam and thus cannot be used with the quasi-continuous beam of (Super-)KEK-B. Nonetheless, a similar feature can be implemented outside of the APV25 chip by using its multi-peak mode where it samples several points along the shaped waveform of a single hit. These data can be processed in order to find the hit time with a precision of a few nanoseconds, depending on signal-to-noise. This method yields another gain of up to 8 in terms of occupancy, or up to 100 in total compared to the current system.

We have developed a prototype readout system consisting of repeater boxes in the front-end and VME-based Controller and FADC+Processor modules in the back-end. The connections are made by 30m of CAT7 cables and equalizers are used to compensate the cable loss for the multiplexed analog strip data being transmitted at a rate of 40 million samples per second.

The repeaters do not only buffer analog and control signals, but also perform the level translation between the front-end, which sits at the bias voltage of the detector, and the back-end which is grounded. This is achieved by capacitive coupling for fast signals (analog, clock, trigger) and optocouplers for slow controls.

The FADC+Processor VME boards perform digitization at an individually adjustable clock phase for each input and digital data conditioning in Altera Stratix FPGAs. Each channel has its own pipelined processing chain which runs at the same speed as data are received. After re-ordering, the silicon strip data are treated with the typical steps of pedestal subtraction, common-mode correction and zero suppression. Moreover, the APV25 will deliver 6 samples along the shaping curve, such that we can use three samples around the maximum together with pre-loaded look-up tables to quickly find the peak time for each hit. Together with a precise time reference from the trigger system, our electronics can reduce the amount of data such that only the hits which belong to the event in question are passed on to the DAQ system.

Parallel session B1 - Systems, Installation and Commissioning / 23

BAO radio electronic system

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The description of the electronic chain for the BArionicOscillation project
The BAO Radio project aims at mapping the H gas distribution in the universe using the 21 cm (1420 MHz) hyperfine transition of atomic hydrogen, up to red-shifts z ~ 1.5-2. The main goal of the project is to constrain the Dark Energy properties using the BAO (Baryon Acoustic Oscillation) cosmological probe, which can be considered as a "standard ruler". The large frequency range (0.5-1.5 GHz), large sky coverage (1/2 sky) and resolution (~ 10 arc") are the main observational constraints which have driven the electronics. The electronics chain is installed for test at the second biggest radio-telescope in the word at Nancay (France) and foreseen to be installed at Pittsburgh (USA). Its architecture can be separated in 3 segments: antenna/RF amplifier, digitization/signal processing/transmission, acquisition by PC. The analog signal coming from the dipole is amplified by a warm LNA then sent to the RF board on a 50-ohm copper cable. The latter behaves as amplifier/mixer: analog signal is filtered and thanks to a 1.2GHz local oscillator split in four 250 MHz bands to match the Nyquist condition of the 500 MHz digitization. This way the analog signal can directly enter the ADC, avoiding an anti-aliasing filter at its input. Nevertheless the possibility to work in down-conversion mode is foreseen, taking advantage of the 1500 MHz analog input bandwidth. The card is a 4-channel VME/USB board. It embeds two 500-MHz ADC, two StGX FPGA and 5-Gbits/s optical drivers. The FPGA perform the FTT in streaming mode, pack data, serialize it and encode it in a 8b/10b protocol and then send it on a 5 Gbit optical link. The PC server house a PCIExpress board based on a Actel STRATIXII, a raid controller board wich is able to manage 8 sata2 hard disk of 160GByte. The FPGA integrate: 128kByte of memory, a controller of the data integrity and a PCIExpress 4x interface. With this architecture we reach 500MByte/s of data transfer to the ram of the PCI and 360MByte/s from the ram to the disk.

POSTERS SESSION / 24

The ATLAS ReadOut System - improved performance with the switch-based architecture

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About 600 custom-built ReadOut Buffer INput (ROBIN) PCI boards are used in the Data-Collection of the ATLAS experiment at CERN. In the standard setup requests and event data are passed via the PCI interfaces. The performance meets the requirements, but may need to be enhanced for more demanding use cases. Modifications in the software and firmware of the ROBINs have made it possible to improve the performance by using the on-board Gigabit Ethernet interfaces for passing part of the requests and of the data. Details of these modifications as well as measurement results will be presented.

Summary:

The custom-built ReadOut Buffer INput (ROBIN) board is used in the ATLAS experiment at CERN to buffer the event data coming from the ReadOut Drivers (ROD) of the sub-detectors via ~1600 optical links. Per ROBIN three of those links can be connected. The maximum input event fragment rate is 75-100kHz (first level trigger rate). The about 600 ROBINs are plugged into the PCI slots of

rack mountable PCs (usually 4 per PC), which run the the software to manage the requests by the Level 2 Trigger (L2) and the Event Builder (EB) as well as delete requests. The connection to the Data Collection (DC) network is established via Gigabit Ethernet (GbE). About 150 of these PCs form the ReadOut System (ROS), which can service ~20 kHz rate of requests from L2 for data input via 2-3 optical links per ROS PC and ~3.5 kHz rate of requests from the EB for data input via all 12 links (4 ROBINs with 3 links each). Certain use cases include Full-Scan requests (similar to EB requests) by L2, which would go far beyond the capabilities of the standard ROS system with respect to the available bandwidth and processing power. For such demanding scenarios the message handling mechanism can be offloaded partially to the individual ROBINs in the so-called Switch-Based scenario, utilizing the on-board
GbE interface for a direct connection to the DC network. To make this possible the FPGA and software for the on-board processor of the ROBIN were modified, allowing the ROBIN to output responses to requests arriving via the network interface like a ROS PC. First measurement results show that a Full-Scan at 20 kHz would be
possible for fragments of ~1kB (which is the canonical size). Details of the implementation and results as well as further plans for improvement will be presented.

POSTERS SESSION / 25

Development of a high resolution transient recorder

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The GANDALF transient recorder with a resolution of 12bit@1Gsps has been developed to sample analog signal pulses with fast rising edges (3ns) and large dynamic ranges at the COMPASS experiment. Signals are digitized and processed by fast algorithms to extract pulse arrival times and amplitudes in real-time and to generate experiment trigger signals.
With 8 analog channels, deep memories and a high data rate interface, this 6U-VME/VXS module is not only a dead time free readout system but also has huge numerical capabilities provided by the implementation of a Virtex5-SXT FPGA to disentangle possible pile-up pulses and determine timing information with a time resolution in the picosecond range.

POSTERS SESSION / 28

e-link: A Radiation-Hard Low-Power Electrical Link for Chip-to-Chip Communication

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[1] *CERN*

the e-link, an electrical interface suitable for transmission of data over PCBs or electrical cables, within a distance of a few meters, at data rates up to 320 Mbit/s, is presented. The e-link is targeted for the connection between the GigaBit Transceiver (GBTX) chip and the Front-End (FE) integrated circuits. A commercial component complying with the Scalable Low-Voltage Signaling (SLVS) electrical standard was tested and demonstrated a performance level compatible with our application. Test results are presented. A SLVS transmitter/receiver IP block was designed in 130 nm CMOS technology. A test chip was submitted for fabrication.

Summary:

With the future upgrade of the LHC and its associated experiments the number of detector channels will increase and it is thus necessary to envisage new low-power interconnections schemes among the on detector ASICs which will allow to reduce the material budget due to cabling and cooling. For this purpose, numerous slow data links could be aggregated into fewer faster and more efficient links.
The GBT project was started to design the future optical data link for the experiments, which brings together the functions of data readout, trigger and control. The GBT will be connected to a number of up to 32 FE Application-Specific Integrated Circuits (ASICs), requiring each one a dedicated electrical link, in a star-point topology. These links target short distance transmission (typically up to 2 meters on PCB, and up to 4 meters on cable) and shall not inject noise in the FE detectors and ASICs. In addition, the links should be designed to minimize crosstalk, sensitivity to common-mode and power supply noise.
For these reasons, the study of a low-power low-voltage-swing electrical link was carried out. Among the several link examined, the Scalable Low-Voltage Signaling (SLVS) industry standard was chosen and tested. The standard describes a differential current-steering electrical protocol with a 200 mV voltage swing on a 100 Ohm load and a common mode of 200 mV. The differential voltage is therefore 400 mV.
A commercial part which uses the SLVS standard was tested with several media types and lengths (5 m Ethernet cable, 30 cm kapton, 2 m PCB and others) and demonstrated bit error rates of less than 10-13 at 480 Mbps on PCB and kapton links, while less than 10-10 on Ethernet STP cable. The article will present the results of the tests.
A transmitter/receiver IP block for integration in the FE ASICs, complying with the SLVS protocol, was designed. In order to minimize the power consumption, the current output of the transmitter is adjustable from 0.5 mA to 2 mA, with a 60% power reduction and thus proportional lowering of crosstalk. Both transmitter and receiver can also be set into a power-down state when unused. The receiver is implemented by a rail-to-rail differential amplifier such that it guarantees a wide common-mode voltage range. The e-link can operate at any speed up to 320 Mbps. The transmitter/receiver block is designed to work in the harsh environment of the experiments characterized by high level of radiation (up to hundreds of Mrd) and intense magnetic field (up to 4 T). The article will presents in detail the design of the transceiver circuit.
Though this IP block is targeted for the implementation of the GBTX-FE connection, it is also suitable for general chip-to-chip communication within the LHC experiments.

POSTERS SESSION / 29

A Zero Suppression Micro-Circuit for Binary Readout CMOS Pixel Sensors

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The EUDET-JRA1 beam telescope and the STAR vertex detector upgrade will be equipped with CMOS pixel sensors allowing to provide high density tracking adapted to intense particle beams. The EUDET sensor Mimosa26, is designed and fabricated in a CMOS-0.35µm Opto process. Its architecture is based on a matrix of 1152x576 pixels, 1152 column-level analogue-to-digital conversion by discriminators and a zero suppression circuitry. This paper concentrates on the data sparsification architecture, allowing a data compression factor ranging from 10 to 1000, depending on the hit density per frame. It can be extended to the final sensor for the STAR upgrade.

Summary:

CMOS Monolithic Active Pixel Sensors (MAPS) are characterized by their detection efficiency close to 100 %, high granularity (~µm), fast read-out frequency (~k frame/s), low material budget (~30 µm Si) and radiation tolerance (~1 Mrad, ~10e13 neq/cm2). They are foreseen to equip new generation vertex detectors in subatomic physics experiments. Their first application coincides with the upgrade of the Heavy Flavor Tracker (HFT) in the STAR (Solenoidal Tracker at RHIC) experiment. They will also equip the beam telescope of the European project: EUDET. Both of these two applications need sensors with digital output and with integrated zero suppression circuit in order to increase the read-out frequency per frame with the aim to reduce the frame occupancy.

The zero suppression circuit integrated in a CMOS pixel sensor is located at the bottom of a matrix and after an analogue to digital conversion circuit. Mimosa26 designed for the EUDET telescope, implements such architecture. It consists of a pixel array of 576 row and 1152 columns with a pixel pitch of 18.4 μm. Each pixel includes an amplification and a Correlated Double Sampling (CDS). The sensor is read out in a rolling shutter mode, each column of pixels ends with a discriminator performing the analogue to digital conversion. The data from 1152 discriminators are processed by the zero suppression circuit.
Before its integration into a final sensor, the concept of the zero suppression logic has been validated. SUZE-01, a reduced scale, fully digital circuit, able to treat and format 128 emulated discriminator outputs, has been successfully fabricated and tested in 2007. The test shows that the algorithm of hits pixel selection is fully operational. This concept is now implemented into the Mimosa26 chip. The zero suppression circuit is structured in a 3 stage pipeline. In the first stage, the 1152 discriminator outputs will be distributed over 18 parallel banks, where a sparse data scan algorithm on hit pixels is performed. Up to 4 contiguous pixel signals above threshold (string) will be encoded in a 2 bit state word. Up to N states per bank can be memorised with column addresses. The column address of a string shared by two neighbouring banks will be transferred only once. The second stage will combine the outcomes of the 18 banks of the first stage. Its multiplexing logic accepts up to M states per pixel row and adds bank address information. N and M will respectively be equal to 6 and 9, according to the hit density defined by the estimated (simulated) amount of events. These values are taking into account a safety margin for the EUDET telescope. The results of the second stage will be stored in the third stage, i.e. a 96 kbit memory split in 2 buffers, allowing a continuous read-out via one or two LVDS links at up to 100 MHz. The contribution to the workshop includes a description of different steps of the architecture. The validation tests of Mimosa26 will also be presented.

POSTERS SESSION / 30

A Digitally Calibrated 12 bits 35 MS/s Pipelined ADC with a 32 input multiplexer for CALICE Integrated Readout

Author: Fatah Rarbi[1]

Co-authors: Daniel Dzahini [1]; Jean-Yves Hostachy [1]; Laurent Gallin-Martel [1]

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The necessity of full integrated electronics readout for the next ILC ECAL presents many challenges for low power mixed signal design. The analog to digital converter is a critical stage for the system going from the very front-end stages to digital memories. We present here a high speed converter configuration designed to multiplex 32 analog channels through one analog to digital converter. A CMOS 0.35μm process is used. The dynamic range is 2V over a 3.3V power supply, and the total power dissipation at 30 MHz is approximately 50mW. An analog power management is included to allow a fast switching into a standby mode that reduces the DC power dissipation by a ratio of three orders of magnitude (1/1000).

Summary:

For the next International Linear Collider (ILC), the front-end electronics for the electromagnetic calorimeter is really challenging. Mechanical constraints lead to the necessity to integrate in the same chip many different critical stages of the read-out electronics: charge preamplifiers, multi gain shapers, analog memories, ADC, and digital back-end. The average power consumption budget is limited to only 25μW per channel. This objective is reachable taking advantage of a power pulsing system with a 1/100 duty cycle, thanks to the beam timing of ILC. The design of the converter must deal with the power dissipation constraint which is one of the main concerns for the electronics. We present here a high speed converter configuration designed to multiplex many analog channels to one ADC. The chip is composed by an ADC and a 32 to 1 analog multiplexer. This design makes the assumption that a high speed converter helps to minimize the cross talk and the equivalent power dissipation related to each channel.
The ADC is composed by a set of pipelined stages. Each stage produces a digital estimate of an incoming held signal, then converts this estimate back to the analog, subtracts the result from the held input. This residue is then amplified before being transferred to the next stage. Eventually the last stage is a full

flash that determines the least significant bit. The successive digital results from the pipelined stages are appropriately delayed throughout a bit alignment network. Then a digital correction stage helps to recover the errors due to the offset of the comparators. A dynamic comparator is sufficient and the total power consumption is reduced.
In this new design, the ADC is composed by a first multi-bit stage followed by a set of 1.5 bit pipelined stages as back-end stage. Increasing the number of bits in the front-end stage, relaxes the matching conditions necessary for the back-end; but it makes the amplifier more power consuming to deal with the gain bandwidth product requirements. The gain errors in this first stage are digitally controlled by means of a butterfly dynamic element matching (DEM) algorithm for a random choice of the DAC capacitors cells. This algorithm helps to minimize the non linearity.
An analog multiplexer is also designed to link the analog channels to the high speed ADC. It uses a pseudo-differential and flip-flop architecture to overcome the capacitor's matching problem. The multiplexer has 12 bits accuracy and a crosstalk between several channels about less 1 LSB. The power consumption of one multiplexer is approximately 7mW according to our simulations up to 30 MHz.
The ADC and multiplexer power consumption per chip is about 4 µW by using power pulsing concept. This leads to an equivalent power consumption about only 125nW per channel. These results show a power consumption for both the multiplexer and the ADC of only 0.5% of the total power consumption which was estimated to 25µW per channel.

Parallel Session B4 - Power, Grounding and Shielding / 31

System Integration Issues of DC to DC converters in the sLHC Trackers

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The upgrade of the trackers at the sLHC experiments requires implementing new powering schemes that will provide an increased power density with reduced losses and material budget. A scheme based on buck and switched capacitors DC to DC converters has been proposed as an optimal solution. The buck converter is based on a power ASIC, connected to a custom made air core inductor. The arrangement of the parts and the board layout of the power module are designed to minimize the emissions of EMI in a compact volume, enabling its integration on the tracker modules and staves.

Summary:

1. Introduction.

A power distribution scheme based on the use of on-board DC to DC converters has been proposed to efficiently distribute power to the front-end electronics of the sLHC trackers. The scheme consists of a first stage buck converter located on the front-end modules or staves, followed by a second-stage switched capacitor converter embedded in each front-end ASIC. An overall efficiency above 80% is expected. Beyond the challenge of developing radiation and magnetic field tolerant converters, the proposed buck converter has to be integrated within the front-end modules minimizing the material budget and the board area. At the same time, the converter must be designed such that the emission of electromagnetic interferences is minimized down to a level that is compatible with the front-end noise requirements.

1. Integration of the power converters.

The environmental constrains and the need for a reduced material budget both imposes the need for a custom, integrated design of DC to DC converters. The integration of the first stage buck converter is

achieved through the development of a power ASIC that embeds most of the functions and components. The output inductor and the large input and output decoupling capacitors can't be integrated in the ASIC and they required an appropriate optimization of material and size without compromising the need for reduced EMI emissions. Because the second stage handles less power and is inductor-less, it is directly embedded in the front-end ASICs, requiring only a reduced set of external capacitors.

1. Air core inductors.

The output inductor of the buck converter is a critical component that has to meet specific requirements: achievable inductance values, DC and AC series resistance, emission of electromagnetic interferences, component dimensions and effective implementation. To be compatible with the DC magnetic field to which it will be exposed, only air-core inductors were considered. Solenoid and toroid topologies were analyzed and compared by means of electromagnetic simulations and modeling. The optimal solution is represented by PCB air-core inductors, that are easy to manufacture and to shield; DC and AC resistances are expected to be at the same level as for the solenoid inductors. The properties of the selected geometries will be presented.

1. Board layout considerations.

The buck controller ASIC is designed such that it requires very few peripheral components on the board. The integration of the PWM controller, with the power switches, the feedback and the compensation circuits in the ASIC limits the need for external components to only few capacitors and one inductor. The pin assignment of the buck controller ASIC is such that the copper traces are shortened as much as possible, in benefit of a reduced board area and of the subsequent reduction of EMI emissions. With this, the converter finds naturally its place on the edge of the hybrid modules and at the head of staves.

1. EMC performance.

The front-end electronics commonly used in the trackers are sensitive to electromagnetic interferences. Those are minimized with careful board layout. A compact power module that encloses the EMI sources within a shielded enclosure with reduced material budget is proposed, further reducing the noise sources. The noise characteristics are determined, critical distances are defined between the converter and the front-end circuits, and quantitative measurements are performed.

Parallel Session A3 - Trigger / 32

A digital calorimetric trigger for the COMPASS experiment at CERN

Author: Markus Krämer[1]

Co-authors: Alexander Mann [1]; Igor Konorov [1]; Jan Friedrich [1]; Stefan Huber [1]; Stephan Paul [1]

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In order to provide a trigger for the Primakoff reaction, in 2009, the trigger system of the COMPASS experiment at CERN will be extend by an electromagnetic calorimeter trigger. Since it was decided to gain from various benefits of digital data processing, a FPGA based implementation of the trigger, running on the front-end electronics, which are used for data acquisition at the same time, is foreseen. This, however, includes further modification of the trigger system to combine the digital calorimeter trigger, with its higher latency, and the analogue trigger signals, which will although make use of digital data processing.

Summary:

The COMPASS experiment is a fixed target experiment at CERN, which, since 2002, uses Muon and Hadron beams from the Super Proton Synchrotron to address widely spread tasks of Muon and Hadron

spectroscopy. In December 2008, in favor of a possible Primakoff measurement, the decision to include the downstream electromagnetic calorimeter into the trigger system was taken. Investigating all possible option, the implementation of the calorimetric trigger was chosen to be a digital one. Respecting the requirements of the foreseen Primakoff measurement and its expected signature the scheme of the first implementation of the digital electromagnetic calorimeter trigger is a simple summation scheme, which uses the central part of the calorimeter. The design of the trigger system, thereby, make use of the FPGA based readout electronics by adding an additional data processing path into the FPGA. Thus the development and production of new hardware for the electromagnetic calorimeter trigger is limited to a custom VME backplane, which is designed to make the trigger system scalable up to the complete calorimeter. Most efforts are spend in signal detection and noise rejection on channel level. Thus the calorimeter does not need to be divided into relatively small trigger towers containing only a few cells, as it is done for analogue calorimetric triggers, but can use a global sum, to which a energy threshold is applied. Applying energy correlation coefficients on cell level the uncertainty of the energy sum is reduced.
Additional efforts have to be taken to combine the existing analogue trigger signals and the digital one with its by approximately 500 ns higher latency. Thereby the delay of the analogue trigger signals will be applied in a digital way using a FPGA, which also make up the final trigger decision. Thus the whole trigger setup will be an hybrid of analogue and digital electronics.
First simulations of the trigger scheme based on 2008 raw data show promising results regarding temporal and energy resolution. Especially the temporal resolution, which is measured to be 1.1 ns for cells, is of special interest to form a trigger decision using coincidence of measured signals. Due to the good noise suppression of the used algorithm the expected trigger rate at an energy threshold of between 20 and 40 GeV is in the order of 20 to 40 kHz, which is compatible with the limits implied by the data acquisition system of the experiment. Compared with the analogue ECAL trigger, which was used for a first Primakoff measurement in 2004, which had a energy threshold of about 80 GeV using 4x4 trigger towers, this is a major improvement. Thereby the uncertainty of the calculated energy, dominated by rounding errors, which are enrolled by communication limits of the existing front-end electronics, are in the order of only a few GeV.
The trigger concept and implementation as well as monitoring should be present. The performance of the trigger system during the data tacking in 2009 in comparison to the expectations gained from the simulations will although be part of the presentation.

POSTERS SESSION / 33

Wafer Screening of ABCN-25 readout ASIC

Author: Peter Phillips[1]

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The ABCN-25 chip was fabricated in 2008 in the IBM 0.25 micron CMOS process. One wafer was immediately diced to make chips available for evaluation with test PCBs and hybrids, programmes which are reported separately. Early indications based on the diced wafer suggested a percentage yield in the high nineties, however the community decided to screen the remaining wafers such that faulty die could be excluded from the module construction programme.

This paper documents the test hardware and software, the procedures used to perform the screening and gives a brief overview of results.

Summary:

The ABCN-25 chip was fabricated in 2008 in the IBM 0.25 micron CMOS process. One wafer was immediately diced to make chips available for evaluation with test PCBs and hybrids, programmes which are reported separately. Early indications based on the diced wafer suggested a percentage yield in the high nineties, however the community decided to screen the remaining wafers such that faulty die could be excluded from the module construction programme.

The objective of the screening is to identify ASICs for which all features needed for operation on a hybrid are functional. In addition to detailed (but not parametric) testing of the digital functionality,

DAC characterisation and verification of the Serial Powering functions of the chip, basic analogue tests will also be made.

The wafers will be screened using a Cascade S300 automatic probe station at the STFC Rutherford Appleton Laboratory. This system has a 12" chuck, so may easily accommodate the 8" ABCN-25 wafers. A custom probe card has been produced to our specifications by Rucker and Kolls. This card does not use an edge connector, instead 0.1" headers are used to connect directly to ribbon cables. This allowed the probe card to be shortened, whilst giving improved vertical clearance over the wafer surface.

The readout hardware utilises commercial units. Fast LVDS signals are generated and received by a National Instruments 6562 PCI card, with 16 LVDS channels running at up to 200MHz. Slow TTL signals are generated by a National Instruments 6509 PCI card. An Agilent 34401A DVM is used to measure the DAC characteristics of the ABCN-25 chip, and a Thurlby Thandar TSX3510P programmable power supply is used to power the chip and to perform basic tests of its serial powering features.

A custom driver board was made by the University of Cambridge to link the hardware together. Based around a Xilinx Spartan 3 series FGPA, it performs the necessary signal buffering and level translation, connecting to the probe card (or a single chip test PCB) using short lengths of twisted pair cable. The FPGA firmware also enables some of the "slow" control signals to be driven under control of the "fast" interface, a useful means to improve the speed of certain digital test vector blocks, for example those involving changes of the chip's address lines. The card has also been designed such that all single ended CMOS control lines which go to the chip may be driven at 2.5V to suit ABCN-25 or at a lower voltage to suit future generations of the ATLAS strip readout ASIC.

The software used for wafer screening is a development of the SCTDAQ software used during the hybrid and module production phase of the present SCT detector. It has been extended for use with ABCN-25 and, optionally, to use the hardware outlined above in place of the custom VME modules used previously. ROOT is used to handle graphics, analysis, and the persistent storage of data.

POSTERS SESSION / 34

A 12 µm pitch CMOS Pixel Sensor Designed in the 3DIT for the ILC Vertex Detector

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CMOS Monolithic Active Pixel Sensors (MAPS) combined with 3D Integrated Technologies (3DIT) offer new opportunities to meet the challenging requirements of the next generation pixel technologies. This paper presents a 3D CMOS pixel sensor design adapted to the innermost layer of the ILC vertex detector. It contains a matrix of 96x256 pixels; each integrating, in a 12µm pitch, a sensing element, a preamplifier, a shaper, a discriminator, a 5-bit Time-to-Digital-Converter (TDC) and a delayed readout microcircuit. It was realised in a commercial CMOS-130nm technology. The paper describes its architecture and expected advantages with respect to the 2D CMOS MAPS.

Summary:

2D CMOS MAPS are foreseen for several applications, ranging from subatomic physics experiments to bio-medical imaging devices. They provide an attractive trade-off between granularity, material budget, readout speed, radiation tolerance and power consumption. The vertex detector upgrade of the STAR (Solenoidal Tracker At RHIC) experiment and the EUDET beam telescope, an EU R&D program, are the first places where MAPS will be operated in real experimental conditions. However, the innermost layer of the ILC vertex detector requires pixel sensors with a high single point resolution of 2-3 µm associated to a very demanding readout speed of a few microseconds per frame only. This makes the design of 2D CMOS MAPS particularly tedious. Based on vertical interconnects between IC layers, 3DIT allow combining in a single chip several thinned and bonded silicon microcircuits. They provide better electrical

performance, low power consumption, highly miniaturised functionalities, improved form factor and lower fabrication cost. They are particularly well suited to CMOS MAPS since they integrate different CMOS manufacturing processes, each optimised for a given sequence of the charge generation and signal processing chain.
The general idea consists in reproducing a pixel matrix in three IC layers (called tiers). In the bottom tier, each pixel contains a sensing element and a preamplifier. In the intermediate tier, it is composed of an amplifier, a shaper and a discriminator. The top tier is a digital circuit layer, which performs, in each pixel, a time to digital conversion for the first hit detected with a time resolution of about 30 μs and flags a potential second hit. For the sake of power consumption, the tier features a delayed readout, adapted to the ILC beam time structure. All these parts should be integrated in a 12 μm pixel pitch.
For the first prototyping step, the circuits foreseen to be integrated in the bottom and middle tiers are laid out in a single tier. The design features a matrix of 96 x 256 pixels, with a 12 μm pixel pitch. Aside of the pixel matrix, the chip hosts test auxiliary blocks such as PLL and 8b-10b encoder to serialize and transmit data out of the chip at a rate of 25 MHz.
The contribution to the workshop will expose prominent design features of the 3D chip architecture and will provide simulation results illustrating its expected operation performances, and highlight its benefits as compared to 2D pixel sensors.

POSTERS SESSION / 35

Charge Pump Clock Generation PLL for the Data Output Blocks of the Upgraded ATLAS Front-End in 130nm CMOS

Author: Andre Konrad Kruth[1]

Co-authors: Abderrezak Mekkaoui [2]; Dario Gnani [2]; David Arutinov [1]; David Elledge [2]; Denis Fougeron [3]; Gabriel Ahluwalia [1]; Giovanni Darbo [4]; Hans Krueger [1]; Jan David Schipper [5]; Markus Gronewald [1]; Marlon Barbero [1]; Maurice Garcia-Sciveres [2]; Michael Karagounis [1]; Mohsine Menouni [3]; Norbert Wermes [1]; Roberto Beccherle [4]; Ruud Kluit [5]; Sourabh Dube [2]; Tomasz Hemperek [1]; Vladimir Gromov [5]

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FE-I4 is the 130nm ATLAS pixel IC currently under development for upgraded LHC luminosities. FE-I4 is based on a low-power analog pixel array and digital architecture concepts tuned for higher hit rates. An integrated PLL has been developed that locally generates a clock signal for the 160 Mbit/s output data stream from the 40MHz bunch crossing reference. This block is designed for low-power, low-area and handles high radiation levels. After a general FE-I4 introduction, the presentation will focus on FE-I4 output blocks and a first prototype submitted early 2009.

Summary:

A new ATLAS Front-End chip, FE-I4, is being developed in a 130 nm standard CMOS technology for use for upgraded LHC luminosities, both for the Insertable B-Layer upgrade project and the outer layers of Super-LHC. FE-I4 is based on a low-power analog pixel array and new digital architecture concepts. A general overview on the FE-I4 architecture will be presented with focus on the challenges of the output stages.

In order to handle the expected hit rate, the front-end will stream data out at 160 Mbit/s. A type-II phase-locked loop (PLL) consisting of a phase frequency detector, a charge pump, a loop filter (LF), a voltage-controlled oscillator (VCO), frequency dividers and buffers has been developed to generate the necessary clock signal with a well-defined duty cycle from the available 40 MHz bunch crossing reference clock of the detector.

The PLL core is designed with a low power budget of 3.9 mW and small die area consumption of 255 um by 225 um. The VCO of the PLL is based on a three-stage differential ring oscillator working at a nominal

frequency of 640 MHz. The design trade-offs involved with the choice of a ring oscillator in terms of area, noise and locking range are elaborated. Choosing an oscillation frequency higher than the output frequency for the VCO guarantees a lower area consumption of the LF capacitors and a well-defined duty cycle handling at the expense of slightly increased power consumption for the VCO and the four-stage dividing chain. Throughout the design, triple-well NFETs are used in all analog blocks for good isolation of the active devices from substrate noise.

In the ATLAS experiment, the PLL will be placed in a hostile radiation environment. In case of single-event transients due to severe charge injections, a short settling time to recover from a loss of lock is important. The presented PLL recovers from any given upset in less than 3 us.

A stand-alone PLL test chip that has been submitted for fabrication early in 2009 will offer output clocks of both 80 MHz for double data rate transfer and 160 MHz for conventional single-edge data stream out at 160 Mbit/s. The differential clock output lines are driven by integrated LVDS drivers. This test chip is scheduled for intense performance measurements and irradiation tests. For these irradiation tests, the PLL is equipped with an on-chip loss-of-lock detection circuit. Furthermore, the demonstrator includes a built-in test structure for 160 Mbit/s double data rate output streaming, consisting of an 8 bit pseudo random binary sequence generator, an 8 bit to 10 bit coder and a serializer.

In September 2009 simulation results will be backed-up by first measurement results on the demonstrator.

POSTERS SESSION / 36

On-chip Phase Locked Loop (PLL) design for clock multiplier in CMOS Monolithic Active Pixel Sensors (MAPS)

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Co-authors: Christine Hu-Guo [1]; Gilles Claus [1]; Kimmo Jaaskelainen [1]; Yann Hu [1]

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In a detector system, clock distribution to sensors must be controlled at a level allowing proper sensors synchronisation. In order to reach theses requirements for the HFT (Heavy Flavor Tracker) upgrade at STAR (Solenoidal Tracker at RHIC), it has been proposed to distribute a low frequency clock at 10 MHz which will be multiplied in each sensor by a PLL to 160 MHz. A PLL was designed for low period jitter less than 20 ps rms and low power consumption of 7mW. This paper presents the architecture and the measurement results of the PLL fabricated in a 0.35µm CMOS process.

Summary:

CMOS MAPS are foreseen to equip the HFT of the vertex detector upgrade of STAR experiment at RHIC (Relavistic Heavy Ion Collider). In order to achieve a vertex pointing resolution of about, or better than, 30 µm, two nearly cylindrical MAPS layers with average radii of about 2.5 cm and 8 cm will be inserted in the existing detector. These two layers will consist in 10 inner ladders and 30 outer ladders respectively. Every ladder contains 10 sensors of 2 cm x 2 cm each.
The sensor for the HFT final upgrade at STAR named Ultimate will integrate on the same substrate a large area pixel array with column-level discriminator, data sparsification circuit and serial data transmission. The sensors readout path to be used in the HFT upgrade requires sending data over a 6-8 meters LVDS link at a clock rate of 160 MHz. Inter sensors data skew and clock jitter have to be controlled precisely in order to ensure sensors synchronization.
A PLL clock multiplier, which allows generating the 160 MHz clock frequency from a relatively low frequency input clock at 10 MHz, will be implemented on each sensor. Using a low frequency input clock allow to reduce the problems of electromagnetic compatibility (EMC) related to the integration density, high speed transmission and coupling with the environment. The same PLL will also equip an optional 8B/10B data transmission block implemented in Ultimate.
The choice of the 10 MHz input clock results of a compromise between the jitter requirement and the complexity for developing a frequency multiplier. The input clock will be multiplied by 16 on chip.
A first prototype of charge-pump PLL circuit was designed and fabricated in a 0.35µm CMOS process.

In order to reduce the PLL jitter coming from supply noise, on-chip voltage regulator is implemented to provide two stable power supplies to the VCO (Voltage controlled oscillator) and the Charge-pump blocks. This technique allows reducing the PLL jitter as long as the voltage regulator has a very good PSNR performance.
The preliminary results show that a period jitter of 13.6 ps rms was measured for the 160 MHz output. The period jitter increases slightly at 16.2 ps rms when the power supply is modulated with 400 mV, 10 kHz square wave. The power dissipation of the PLL including voltage regulator is estimated to 7 mW at 160 MHz.
The contribution to the workshop includes the PLL overview with a focus on the measurement results and future developments.

POSTERS SESSION / **37**

Standalone radiation monitors for electronics in High Energy Physics

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[1] *CERN*

Based on the principle of the RADMON on line radiation monitoring system for the LHC, a new type of low cost, battery powered radiation monitors has been designed that do not need external cabling. In this paper we will outline the hardware design, summarise on the radiation tolerant components and tests and describe the associated usb interace and labview software. First operational data from the CERN accelerators will be given and compared to monte carlo simulations.

Summary:

A new type of radiation monitors is presented that does not need any external cabling. Using special selected Li batteries, integrated levels of the total dose, 1 MeV n and h > 20 MeV are continiously stored for a period of maximum 680 days. The data is stored in triplicated, sepreately powered registers for a maximum of 10 years and can be read out at any time. The key points in the design were to lower the current consumption of the entire device to 1.6 mA, to make it radiation resistant up to 200 Gy and to make it operate reliable in the magnetic fields of CMS/ATLAS. To retrieve the data from a device, a USB interface in combination with a Labview application is used that can be installed on mini-PCs and on handhold computers. The readout operation takes only a few seconds which means a considerable improvement with respect to classical passive dosimeters.

Parallel Session B4 - Power, Grounding and Shielding / **38**

Performance and comparison of custom serial powering regulators and architectures for SLHC silicon trackers

Authors: Marc Weber[1]; Tomas Tic[2]

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Serial powering is an elegant solution to power the SLHC inner trackers with a minimum volume of cables. So far R&D on serial powering for silicon strip modules was based on discrete commercial electronics. With the delivery of the first iteration of the ABCN-25 readout chip and the SPi serial powering interface chip, custom elements of shunt regulators and transistors became available. The

combination of ABCN-25 and SPi can be used to implement three complementary serial powering architectures. The performance and features of the three architectures obtained with 20 chip and 10 chip ABCN-25 hybrids will be presented.

Summary:

Serial powering is one of the few practical approaches to distribute power to the SLHC inner trackers with a minimum volume of cables. A number of integrated test structures (supermodules) with serial powering circuitry have been built and investigated over the last years with very promising results. The serial powering circuitry (shunt regulator, shunt transistors and LVDS buffers for AC coupling) was so far based on discrete commercial electronics.

To overcome this limitation in radiation-hardness and real-estate, various serial powering and power management blocks have been implemented in the first version of the ABCN-25 chip. In addition a dedicated serial powering chip, the serial powering interface (SPi) became available. Both ABCN-25 and SPi are realized in 0.25 um CMOS processes.

With these chips three complementary serial powering architectures can be realized. In one architecture the SPi regulator and shunt transistor act as a local power supply on the hybrid and the ABCN-25 internal shunt regulators are not used. This is conceptually the simplest implementation. It requires a robust shunt transistor layout. In another architecture, the SPi shunt regulator controls not a single shunt transistor but distributed shunt transistors in each ABCN-25. Finally, in a third architecture, SPi is not used and the shunt regulators and transistors implemented in ABCN-25 are operated in parallel.

These architectures are implemented on conventional copper Kapton flex hybrid prototypes with up to 20 ABCN-25 chips each. The hybrids were designed at Liverpool University for R&D on the ATLAS SLHC short strip tracker.

After a brief discussion of the architectures and their theoretical features, the characterization results will be presented and discussed. This includes regulator output voltage noise, dynamic impedance, and hybrid noise and noise occupancy as a function of temperature and current. Depending on the status of the measurements at the time of the conference, results on a full module or with a limited number of hybrids in series will be shown as well.

POSTERS SESSION / 39

A programmable 10 Gigabit injector for the LHCb DAQ and its upgrade

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The LHCb High Level Trigger and Data Acquisition system selects about 2 kHz of events out of the 1 MHz of events, which have been selected previously by the first-level hardware trigger. The selected events are consolidated into files and then sent to permanent storage for subsequent analysis on the Grid.

The goal of the upgrade of the LHCb readout is to lift the limitation to 1 MHz. This means speeding up the DAQ to 40 MHz. Such a DAQ system will certainly employ 10 Gigabit or technologies and might also need new networking protocols: a customized TCP or proprietary solutions.

A test module is being presented, which integrates in the existing LHCb infrastructure. It is a 10-Gigabit traffic generator, flexible enough to generate LHCb's raw data packets using dummy data or simulated data.

These data are seen as real data coming from sub-detectors by the DAQ. The implementation is based on an FPGA using 10 Gigabit Ethernet interface. This module is integrated in the experiment control system.

The architecture, implementation, and performance results of the solution will be presented.

Parallel Session B3 - Packaging and Interconnects / **40**

Construction and Performance of a Double-Sided Silicon Detector Module using the Origami Concept

Authors: Christian Irmler[1]; Manfred Pernicka[1]; Markus Friedl[1]

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The APV25 front-end chip with short shaping time will be used in the Super-Belle Silicon Vertex Detector (SVD) in order to achive low occupancy. Since fast amplifiers are more susceptible to noise caused by their capacitive input load, they
have to be placed as close to the sensor as possible. On the other hand, material budget inside the active volume has to be kept low in order to reduce multiple scattering. We currently construct a low mass sensor module with double-sided
readout, where thinned APV25 chips are placed on a single flexible circuit glued onto one side of the sensor. The interconnection to the other side is done by Kapton fanouts, which are wrapped around the edge of the sensor.

Summary:

A major upgrade of the KEK-B factory (Tsukuba, Japan) and the Belle detector is foreseen until 2013/2014. The target luminosity is 5 to 8 x 10^35 cm^-2 s^-1, which is about 30 - 50 times the present value. In the course of this upgrade
the Silicon Vertex Detector (SVD) will be completely replaced, since the present one, particularly its innermost layer, has already reached its limit in terms of occupancy and dead time.

In order to achieve low occupancy the APV25 front-end chip (originally developed for CMS) will be used to read out the Super-Belle SVD. Thanks to its short shaping time of nominally 50 ns an occupancy reduction by a factor of ~12.5 can be
achieved compared to the VA1TA chip of the present system. However, fast amplifiers are more susceptible to noise, which is mainly caused by the capacitive load at the inputs. Hence, the APV chips have to be placed as close to the sensor as possible. On the other hand, Belle operates at comparatively low energies of 3.5 and 8 GeV for positrons and electrons, respectively, and thus the material budget inside the active volume has to be kept low to minimize multiple scattering.
In the present SVD all sensors are read out from the edge of the ladders using long flex circuits and sensor ganging in the outer layers. Regarding the huge capacitive load and the fast shaping, such construction is not feasible together
with APV25 front-end chips.

We present a concept for double-sided readout of a silicon strip detector, covering both low material budget and short connections between sensor and front-end amplifiers. In that scheme the APV25 chips of both sides are placed on a single flexible circuit, mounted onto one side of the sensor. This flex-hybrid is made of only three copper layers and contains integrated pitch adapters to connect the strips on the same side as the hybrid. The channels of the
opposite side are attached by small flexible fanouts wrapped around the edge of the sensor, hence the name Origami Concept. Thermal and electrical insulation between hybrid and sensor is given by a 1 mm Rohacell (low mass styrofoam)
layer. Arranging all front-end chips in a row allows cooling by a single aluminum pipe, which is also used as a mechanical support. To achieve lowest possible material budget, the APV chips will be thinned down to approximately 100 μm.

Presently, the design of the hybrid and the flex fanouts is already finished. A few pieces of them are currently in production and will be delivered until mid of May. After receiving them, we will start to

build a module using the Origami Concept as described above. By the time of the TWEPP workshop we will be able to present results of source measurements and a beam test, which is scheduled in August 2009.

Key words:
APV25, Silicon Detector, DSSD, Chip-on-Sensor, Origami, Belle

POSTERS SESSION / 41

Low power discriminator for ATLAS pixel chip

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The design of the front-end (FE) pixel electronics requires high speed, low power, low noise and low threshold dispersion. In this work, we propose a new architecture for the discriminator circuit. It is based on the principle of dynamic biasing and developed for the FE chip of the ATLAS pixel upgrade. This paper presents two discriminator structures where the bias current depends on the presence of a signal at the input of the discriminator. Since the activity in the FE chip is very low, the power consumption is greatly reduced.

Summary:

A pixel FE pixel chip is developed in a 130nm CMOS technology for the B-layer replacement. The chip contains around ~27,000 pixels of 50μm×250μm each. The pixel contains a fast charge preamplifier, a second stage amplifier, a discriminator and a logic bloc to transfer the hit information to the chip periphery.
The current pixel design uses a continuous biased discriminator where the bias current is defined in order to reach the required speed and to minimise the time walk. This allows assigning the hits to their corresponding bunch numbers with high probability. In the main analog pixel architecture flavour studied, the discriminator power consumption can reach 20% of the total pixel power budget.
Since the average counting rate for one pixel is low, it is possible to greatly reduce the power consumption of the pixel if the discriminator is biased only when a hit is present.
This paper proposes an efficient way to design very low power discriminators for pixel detectors. Two different architectures based on the dynamic biasing principle are proposed.
In the first one, an input differential stage controls the bias of the main comparator stage. The input voltage signal is converted to a current signal used to bias the second stage after applying a multiplicative factor.
The second architecture uses two stages. An auxiliary comparator with a low threshold value powers up selectively the main comparator stage.
A prototype test chip has been designed as an array of ~300 pixels. Different discriminator architectures were implemented in this design. The chip is submitted for fabrication in 130 nm CMOS technology. We will be able to compare power consumption, noise and dispersion performances, as well as timing and crosstalk performances for the implemented architectures.

Parallel session B1 - Systems, Installation and Commissioning / 42

Data acquisition system for a proton imaging apparatus

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New developments in the proton-therapy field for cancer treatments, leaded Italian physics researchers to realize a proton imaging apparatus consisting of a silicon microstrip tracker, to reconstruct the proton trajectories, and a calorimeter, to measure their residual energy. For clinical requirements, the detectors used and the data acquisition system should be able to sustain 1 MHz proton rate. The tracker read-out, using an ASICs, acquires the signals detector and sends data in parallel to an FPGA. The YAG:Ce calorimeter generates also the global trigger. The data acquisition system and the results obtained with a 60MeV proton beam are presented and discussed

Summary:

The proton therapy is a good clinical treatment for cancer as it permits to obtain a dose distribution extremely conform to the target volume. In order to fully exploit the potential of proton dose release, the dose calculation should be performed with high accuracy. This issue requires the knowledge of proton stopping power inside the tissues. Up to now this information is deduced from X-Rays Computed Tomography, but the error related to this procedure is relevant. To overcome this problem, proton imaging can be used as a direct method for stopping power determination. Moreover, the same imaging system can be useful in the patient positioning verification. The aim of the project is to develop a proton imaging system with density and spatial resolution less than 1% and 1 mm respectively. The apparatus that will be presented reconstructs the map of the electron density by tracking the single proton through the traversed tissue and by measuring its residual energy. In order to cross the entire patient thickness, proton energy must be 200-250MeV . The need for tracking the single particle derives from the Coulomb multiple scattering of protons inside the matter. In order to acquire an image in a fraction of a second, following clinical requirements, the system should be able to sustain 1MHz proton beam. Our apparatus includes a tracker with eight x-y planes based on position sensitive microstrip detectors to determine particle entry and exit point and direction. Downstream the tracker, a calorimeter is used for residual energy measurement. Each tracker plane consists of two module with sensors positioned at 90° to each other. The tracker module includes a front-end board and a digital board. The microstrip silicon detector, positioned in the front-end board, is coupled with eight ASICs each serving 32 front-end channels. The integrated circuit, developed by the collaboration, via a charge sensitive amplifier, a shaper and a comparator, converts the fast current signal from the microstrip crossed by the particle, in a digital pulse of 300-800ns. The duration of the pulse depends on the amount of energy released by the proton and on the threshold value used. So, for fixed threshold value, by the Time Over Threshold (TOT) technique it is possible also to measure the charge released into the silicon detector. The outputs signals are sent in parallel to an FPGA located on the digital board which performs zero suppression and moves data to a buffer memory. An Ethernet commercial module is use both for data transfer to the central acquisition PC and to control the tracker module DAQ parameters. Results about a single plane test performed at Laboratori Nazionali del Sud (LNS) with 60MeV proton beam will be presented. The calorimeter consists of four YAG:Ce scintillating crystals, coupled with commercial photodiodes. The read-out system acquires the information about the residual energy of the particle and generates the trigger signal and the system global event number. Thanks to the fast scintillating light decay constant the YAG:Ce crystal is able to sustain 1MHz proton rate. This apparatus was tested with 60MeV and 200MeV proton beams at LNS and Loma Linda University Medical Center (LLMC) respectively. Data analysis shows that this crystal meets high and spatially-uniform efficiency and energy resolution requirements.

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ALICE TPC CONTROL AND READOUT SYSTEM

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ALICE is a dedicated heavy-ion experiment at CERN LHC. It aims to reproduce the state of matter shortly after the Big Bang, i.e. the quark-gluon plasma. Each lead-lead collision will produce the order of ten thousand new particles. Detailed study of the event requires precise measurements of the particle tracks. An 95m3 Time Projection Chamber (TPC) with more than 500 000 read-out pads was built as the main central barrel tracker. Collisions can be recorded at a rate of up to about 1 kHz. The front-end electronics, designed from FPGAs and custom ASICs, performs shaping, amplification, digitalization and digital filtering of the signals. The data is forwarded to DAQ via 216 1.25 Gb/s fiber-optical links. Configuration, control and monitoring is done by an embedded Linux system. The close proximity of the electronics to the collisions exposes it to radiation, which required radiation tolerant design strategies.

First results on the performance of the front-end electronics and the distributed detector control system are presented.

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An integrated DC-DC step-up charge pump and step-down converter in 130 nm technology

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After the LHC luminosity upgrade the number of readout channels in the ATLAS Semiconductor Tracker will be increased. Therefore a new solution for powering the readout electronics has to be found.

The two main approaches for power distribution are under development, the serial powering of a chain

Summary:

The High Luminosity Upgrade sets very demanding requirements on the granularity of the ATLAS Inner Detector resulting in an increase of the number of readout channels. Therefore two new approaches for power distribution are currently under development, the serial powering of a chain of detector modules and the parallel powering with DC-DC conversion on the modules.

In the serial powering schema, the chain of modules is powered from a current source, while the voltage is stabilized by the shunt regulator integrated on each readout chip. This solution improves overall power efficiency of the system by significant reduction of the number of power cables. There are several possible options for power management on the module level in the serial powering schema. Some of them require switched capacitors DC-DC converters integrated in the readout chips.

In the parallel powering option the modules are supplied from a high voltage source and the voltage is then reduced in DC-DC converters mounted of each module. In case of two-stage DC-DC conversion scheme a switched capacitor DC-DC converter can be integrated in the readout chip.

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In the paper we present two designs of switched-capacitor DC-DC converters, a step-up charge p
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The switched capacitor step-up charge pump is based on the voltage doubler concept. The main part of the circuit consist of two low threshold voltage, cross-coupled NMOS transistors, four thick oxide PMOS transistors working as serial switches and four capacitors including three external SMD and one fully integrated on the chip. The circuit works at 500 kHz frequency and pump voltage on both clock edges. For the input voltage of 900 mV, it delivers an output voltage of 1.6 V at the output nominal current. The power efficiency extracted from SPICE simulations is up to 84%. To eliminate the effect of parasitic vertical bipolar transistors an auxiliary charge pump was added. It allows the bulk of PMOS serial switches to be put on the highest potential. Further improvements are related to switching capability, which can be significantly increased by adding a level shifter circuit.

An optional solution assuming input voltage of 2.0 V and a step-down DC-DC converter is considered as well. The core of the circuit is built of four transistors with thick gate oxide and three external SMD capacitors. The whole circuit is supplied with 2.0 V. Due to the better driving capability of the switch working with lower output voltage there is no need to use any level shifters. The output voltage is as high as 920 mV for nominal current which is 60 mA. The power efficiency calculated from SPICE simulations is up to 92%.

The power efficiency of different powering systems and different power management options in the readout chips will be estimated based on an analytical model including the parameters of the power cables, linear regulators integrated in the readout chips and expected supply voltages, and the power consumption of the readout chips in 130 nm technology.

POSTERS SESSION / 45

Error-free 10.7 Gb/s digital transmission over 2 km optical link using an ultra-low-voltage electro-optic modulator

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We demonstrate the feasibility of 10.7 Gb/s error-free (BER < 1e-12) optical transmission on distances up to 2 km using a recently developed ultra-low-voltage commercial electro-optic modulator (EOM) that is driven by 0.6 Vpp and with an optical input power of 1 mW. Thus, the modulator could be driven directly from the detectors' board signals without the need of any further amplification reducing significantly the power dissipation and the material budget.

Summary:

In the high luminosity stage of the Large Hadron Collider, the so called SLHC, the bandwidth needed for data extraction from the detectors will grow significantly due to the huge particle content of events which will be generated at high repetition rates. Increase in bandwidth of the optical link is thus a key factor to allow fast data processing and to reduce latency times between events' detections. Actually, the trend is focusing on increasing the data rate of the optical link to around 5 Gb/s looking in perspective at a transfer rate of 10 Gb/s. The increase in the transmission bit rate not only would permit a higher speed data transfer, but could also significantly reduce the number of optical links per detector leading to volume and cost reduction.
To this extent, electro-optic modulators (EOM), in particular lithium niobate Mach-Zehnder modulators (LNM), are widely employed in the telecom industry and represent a standard de facto for 10 to 40 Gb/s transmissions. Besides being capable of high frequency modulation, LNM are also proven to be: very radiation hard, immune to high static magnetic field and operating at low temperatures (down to -20°C). All these features are close to the strict requirements of the SLHC and for this reason LNM can be attractive in the implementation of the next generation optical-links. Moreover, the possibility to use external CW laser as optical sources, presents many advantages since it lowers the power dissipation inside the detector and the risk for the laser integrity due to absence of transient instabilities caused by high radiation level, and it allows for higher bit rates (≈ 40 Gb/s).
In the context of the SLHC optical link, the typical driving voltage (3-4 V) of LNMs at high bit rate may create a serious issue requiring the use of amplifiers, and a general increase in the dissipated power. A recently developed ultra-low-voltage LNM, employed for transmission over the typical short distances (transmitter-to-receiver length < 1 km) covered by an optolink in High Energy Physics experiments, can represent a solution to this problem.
Indeed, in this work we demonstrate that error-free transmission (BER < 1e-12) at a bit rate of 10.7 Gb/s and for a 2 km optical-link is achievable by modulating a ultra-low-voltage LNM with 0.6 Vpp and having 1 mW of optical input power at a wavelength of 1550 nm. This result shows that it could be feasible for the LNM to be modulated directly with the detectors' board signals which can reach up to 1 V without the need for any further amplification, thus strongly reducing the components number and the power requirement for each optical link.

POSTERS SESSION / **47**

Design of the CMS-CASTOR sub detector readout system by reusing existing designs

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The CMS CASTOR detector is a small calorimeter located at 14.3 meters from the interaction point behind the HF detector. The CASTOR project was only approved mid of 2007. Cherenkov radiation in a sampling structure is used to measure the energy as the HF does. Logically one would use the same readout hardware as used for HF. But also other architectures were considered. Given the limited resources and time, developments from scratch were excluded. This talk presents an overview of the implementation of the readout chain as well as the considerations for the different choices. The HF front end system was finally chosen. It sends all the digitized samples via optical links to the counting room for further processing. The HF architecture of the data selection and processing didn't fit so well our requirements due to different segmentation and costs. A development by the TOTEM collaboration and by the CMS pre-shower was more close to our needs in respect to flexibility, availability and material cost. This architecture needed only a small hardware adaptation as well an adaptation of the requirements. The full CASTOR detector will be installed in June 2009 and we expect that in September we can present the results of the commissioning of the detector.

Parallel Session B3 - Packaging and Interconnects / **48**

Application of a new interconnection technology for the ATLAS

pixel upgrade at SLHC

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We present an R&D activity aiming towards a new detector concept in the framework of the ATLAS pixel detector upgrade exploiting vertical integration technologies developed at the Fraunhofer Institute IZM-Munich. A new Solid-Liquid-InterDiffusion technique is investigated as an alternative to the bump-bonding process. We also investigate the extraction of the signals from the back of the electronic chip through Inter-Chip-Vias to achieve a higher fraction of active area with respect to the present pixel module design. We will present the layout and the first results obtained with a production of test-structures designed to investigate the SLID interconnection efficiency as a function of different parameters, i.e. the pixel size and pitch, and the planarity of the underlying layers.

Summary:

Our R&D activity is focused to develop a new detector concept for the upgrade of the ATLAS pixel system at SLHC.
The Solid-Liquid-InterDiffusion (SLID) is a new interconnection technology between sensors and front-end electronics, developed by Fraunhofer IZM-Munich. SLID is investigated in this R&D activity because it can in principle overcome some limitations inherent to the present bump bonding process, namely the high cost and the minimum feature size required. Moreover SLID allows the stacking of different ASIC layers because the bonding process does not affect the SLID connections realized in a previous step.
Pixel sensors, with an active thickness of 75 and 150 um, produced at the MPI Halbleiterlabor (MPI-HLL) in collaboration with industrial partners, will be connected by the SLID process to the FE-I3 chips. The contact scheme in the passivation layer of the pixel sensors has been modified to be compatible with the SLID interconnection. In all the other details the design of the active area is unchanged with respect to the present ATLAS pixels. The SLID interconnection will be obtained in the "chip to wafer" approach. This offers the possibility of singularizing the chips thus helping to increase the process yield. On the other hand it introduces a placement uncertainty due to the chip positioning on the handle wafer needed to support the ASICs during the SLID interconnection. The signals that in the present layout are extracted via wire-bonding to the bonding pad in the cantilever will be routed through Inter-Chip-Vias from the ASIC backside where post-processing bonding pads will be created. For this purpose the ATLAS FE-I3 wafer will be thinned down to about 50 um.
We will present the layout and the first results obtained with a production of test-structures designed to investigate the performance of the SLID interconnection. The basic test devices are daisy chains with different pad sizes and pitches. In some of the chains we introduced a imperfect planarity of the surface beneath the SLID pads to study the effect on the interconnection efficiency. The "sensor" and "chip" structures, produced at MPI-HLL have been connected both "wafer to wafer" and "chip to wafer". The deposition of the metal system for SLID and interconnections have been performed at IZM-Munich. A good interconnection efficiency has been measured for all pad geometries. The size of the misalignment between sensors and chip structures has been evaluated. We will report on the results of the observations of the interconnected wafers with an infrared microscope to study the definition of the SLID metal system.

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The design of a low power, high speed phase locked loop

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Detector front-end readout upgrades for the ATLAS Liquid Argon Calorimeter call for radiation tolerant, high speed, and low power optical digital data links. In the development for a high speed, low power serializer ASIC, we have designed an LC-based phase locked loop (PLL) using a commercial 0.25-μm Silicon-on-Sapphire (SoS) CMOS technology. Post-layout simulation indicates that we can achieve a tuning range of 4.1 – 5.3 GHz with power consumption below 20 mW. The PLL will be submitted for fabrication in August, 2009. The design, optimization, and simulation results are presented.

Summary:

The upgrades of the ATLAS Liquid Argon Calorimeter call for radiation tolerant, high speed, low power, optical digital data links. In the development of a 16:1 serializer for the ATLAS detector front-end readout upgrade, we have designed an LC-based phase locked loop (PLL) using a commercial 0.25-μm Silicon-on-Sapphire (SoS) CMOS technology. We choose the SoS technology because of its high speed, low power, radiation tolerance, and availability of high quality analog devices like inductors. This technology has been evaluated to be suitable for development of radiation tolerant ASICs in the application of particle physics front-end readout systems. Post-layout simulation indicates that the PLL can work around 5 GHz with less than 20 mW power consumption. This PLL is a central part of a serializer working at 10 gigabit per second.

The PLL consists of a voltage control oscillator (VCO), a divider (divided by 8), a phase frequency detector (PFD), a charge pump, and a second-order low pass filter. A LC based VCO has been chosen because of its low power, high speed, and insensitivity to radiation. On-chip spiral inductors and MOSFET varactors are used as the LC tank. On-chip spiral inductors in the SoS CMOS technology have higher Q factor than those in conventional bulk CMOS silicon technologies. The varactors in the SoS CMOS technology have monotonic voltage capacitance curve and large tuning range. Six topologies of LC-based VCOs are compared and the inductors, the transistor size, the value of the current source, and the varactor size are optimized. Simulation indicates that we can achieve a tuning range from 4.1 to 5.3 GHz, a 2 V oscillation swing, a phase noise of -100 dBc/Hz at 1 MHz offset, and a power consumption less than 10 mW. The first stage of dividers is a common-current-logic (CML) divided-by-two circuit and the following two stages are CMOS. Simulation of the first stage divider indicates that the divider can work up to 5.4 GHz with less than 10 mW power consumption. The power consumption of the two CMOS dividers is very small compared with that of the CML divider. A conventional D flip-flop based PFD is implemented with dead-zone eliminated. An active unity buffer is used to minimize the charge sharing in the single-ended charge pump. We use a two-order passive low pass filter with programmable bandwidth (1.25 MHz, 2.5 MHz, and 5 MHz) to cope with different reference clock qualities

The PLL will be submitted for fabrication in August, 2009 and evaluated in the lab and in the radiation environment in the end of 2009 and in the beginning of 2010.

POSTERS SESSION / 51

High-Speed Serial Optical Link Test Bench Using FPGA with Embedded Transceivers

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Serial optical data transmission provides a solution to High Energy Physics experiments' readout systems with high bandwidth, low power, low mass and small footprint. It will commonly be used in

detector upgrades for the SLHC. In the meanwhile, commercial FPGAs with embedded multi-gigabit transceivers have become accessible. We develop a test bench with such a device at its core to verify link configurations, evaluate radiation tolerant components and automate test procedures. The prototype's applications in irradiation tests and characterization tests such as online data analysis, bit error rate (BER) sensitivity, jitter extraction and bathtub curve are discussed in detail.

Summary:

New High Energy Physics experiments impose ever more stringent demands on bandwidth and radiation tolerance of optical transmission links. The rapid increase in number of data channels and transmission speed justifies the exploitation of mature commercial silicon technologies. FPGAs with embedded multi-gigabit serial transceivers (MGT) such as Altera's Stratix II GX family and Xilinx's Virtex 5 FXT family offer comprehensive data interface designs that operate up to 6.5Gbps. The newest Stratix IV GX and Virtex 6 push the serial transceiver rate up to 10Gbps. A reference link deploying this proven solution serves as a configurable test bench as well as a custom design baseline. It can be used to verify various radiation tolerant optical links and test their components that are under development for detector upgrades for the SLHC. In this paper, we present a hardware system of commercial FPGA with MGT and a firmware/software platform to support its application in link characterization tests and component irradiation tests. The system's most basic function is BER testing. We investigate links using the FPGA test set with various optical transceiver modules and compare to links using a standalone Anritsu MP1763/4 bit error test set. The results show no significant discrepancy. Automated sensitivity test is also performed where a Labview program interfaces with the FPGA and a variable optical attenuator to obtain the BER vs. optical modulation amplitude curve. Single-event effects have been the major concern of the front-end readout electronics, especially in the inner most detector region. Both single bit and multiple bits upset are observed and need to be mitigated. We propose a scheme to further study such events in irradiation tests. A parallel BER tester is built using the FPGA system where the error detector records three types of errors: single bit flip, multi-bits flip in one parallel word and multi-bits flip in two or more consecutive words. In the last type of errors, link maybe lost and need to be reestablished. Bit location, flip type, time stamp and duration of frame loss in the last type are recorded. This scheme enables longer testing duration and provides complete data logging during a SEE test for offline data analysis. A BER bathtub curve can be scanned for link characterization. It is also the standard method for jitter extraction in Fiber Channel and Gigabit Ethernet standards. A timing delay scheme of 10ps resolution is required to acquire enough data points on the curve edge. The time-base shifting needs to be implemented before the clock recovery unit, in the analog domain. We report the bathtub scan with the clock recovery unit disabled, whose effect on link jitter can be taking into consideration through convolution using the vendor provided jitter report.

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Development of a 16:1 serializer for data transmission at 5 Gbps

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Radiation tolerant, high speed and low power serializer ASIC is used for optical digital data links systems in particle physics. Based on a commercial 0.25 μm silicon-on-sapphire CMOS technology, we designed a 16:1 serializer with a 5 Gbps serial data rate. We present the design details and post layout simulation results. This ASIC will be submitted for fabrication in August 2009. A shared PLL multi-channel serializer with a redundant scheme and ultra low power consumption is also discussed for applications with fibre ribbons to achieve a data throughput in tens of gigabit per second range.

Summary:

A commercial 0.25 μm silicon-on-sapphire CMOS technology has been evaluated to be suitable for development of radiation tolerant ASICs for particle physics' front-end readout systems. Based on this technology we developed a 16:1 serializer with a serial data rate at 5 Gbps. The serializing unit consists of a cascade of 2:1 multiplexing circuit based on a static D-flip-flop for its better SEE immunity. In this design only the last 2:1 multiplexing stage works at 5 Gbps or the highest speed. This provides the possibility of using dynamic circuit with majority voting in future designs for speeds above the static D-flip-flop. A simple divide-by-two divider chain is used in the clock system and this greatly simplifies the design especially at high speed. A differential ring oscillator based PLL provides the 2.5 GHz clock with 50% duty cycle, generated from the 312.5 MHz reference clock. The PLL loop bandwidth is programmable to cope with different reference clock qualities. In order to check the overall behavior of this PLL, a c++ based behavior model and a jitter analysis tool have been developed. A CML driver is developed for the electric output signal. Post layout simulation provides power consumptions for each function block to be 45 mW for LVDS receiver, 135 mW for the PLL, 102 mW for the serializing unit and 82 mW for the CML driver. The total power consumption is less than 400 mW, or 80 mW/Gbps.

In order to achieve data throughout in 25 Gbps range, for applications in the ATLAS liquid argon calorimeter front-end readout upgrade, we designed a 5-in-6-out serializer ASIC with a shared PLL and a redundancy scheme, for optical links with a 12-way fibre ribbon (two serializer chips and a total throughput about 50 Gbps). The redundancy improves system reliability, an issue in applications in particle physics where the front-end electronics are usually inaccessible for maintenance. The power consumption is estimated to be 1.5 W or 50 mW/Gbps. This idea will also be implemented in future designs based on a faster LC based PLL to boost the data throughput into 40-50 Gbps range to achieve a throughput of 80-100 Gbps with one 12-way fibre ribbon.

This design will be submitted in August 2009. We will evaluate this ASIC in lab and in radiation environment starting in the winter of 2009 and 2010.

Parallel Session A5 - ASICS / **54**

Smart Analogue Sampler for the Optical Module of a Cherenkov Neutrino Detector

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A transient waveform sampler/recorder IC has been developed and realized in AMS C35 technology to be used in the front-end of a neutrino detector. It is based around a switched capacitors array unit sampling its voltage inputs at 200MHz external clock rate and transferring them at its outputs at 1/10th of the sampling rate. This unit is replicated inside the ASIC providing 4 independent analogue sampling queues for signal transients up to 32 x 5ns and a fifth unit storing transients up to 128 x 5 ns. A micro-pipelined unit, based on Muller C-gates, controls the 5 independent samplers.

Summary:

The use of an analogue sampler/recorder for the purposes of the front-end electronics of a Cherenkov neutrino detector has been exploited and demonstrated its effectiveness in detectors as ANTARES, Nestor and IceCube. The readout system of those detectors must provide the time-stamping of Single PhotoElectron (SPE) signals produced by photomultipliers while separating them from background and bioluminescence events which mainly contribute to the dead-time.
The solution presented has been tailored to sustain an event rate of short pulse (less than 160 ns) events in excess of 300 kHz with a negligible dead-time, with an amplitude of one SPE signals of about 570 mV, while still providing a mean to record longer photomultiplier events (640 ns + 160 ns maximum length).

The ASIC have three buffered analogue input channels and a single analogue output: a record of 32 samples is acquired after a rising edge is detected on its Signal Over Threshold (SOT) digital input. This also strobes the content of a 200 MHz internal counter inside a digital FIFO which stores it along with the reference to the analogue sampling queue holding the voltage values. After a fixed delay of 100 ns the status of the SOT pin is checked and a decision is made whether to end the sampling process within the 160 ns window, or continuing it, storing the samples into a larger unit holding a 640 ns time window. At the end of the chosen sampling windows, the record formed by the counter time-stamp, the digital code classifying the three input signals and generated outside the ASIC and the stored samples for each of the three input channels, is put on hold and a Ready To Readout signal is issued on an output pin. Depending on the classification code, only one of the channels out of the three sampled ones will be multiplexed to the single analogue output pin for the external readout. The availability of four identical sampling units provides a buffer mechanism to the external data acquisition electronics able to deal with an event rate of SPE-like signals of about 300 kHz. The four units are independent the one from the other and the stored data could be readout from each unit while the next in the sequence is sampling its inputs. If a new rising edge is detected on the SOT pin when all 4 units still hold data (or a readout is being performed in one sampling unit) the three input channels are sampled by the fifth (longer) unit.

A full custom ASIC has been realized in a standard 0.35um CMOS technology: die area is about 12 mm2 and packaged samples should be available for testing by the end of May'09. The design is a full-custom mixed-signal circuit using switched-capacitors arrays and classAB rail-to-rail operational amplifiers in its analogue part, and Sutherland's micropipeline in the digital part: the supply voltage is 3.3V and the estimated power dissipation is less than 100 mW with a SNR better than 62 dB over 1V dynamic range.

Parallel Session A3 - Trigger / 55

Analogue Input Calibration of the ATLAS Level-1 Calorimeter Trigger

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The ATLAS Level-1 Calorimeter Trigger is a hardware-based pipelined system using custom electronics which identifies, within a fixed latency of 2.5 us, highly energetic objects resulting from LHC collisions. It is composed of three main sub-systems. The PreProcessor system first conditions and digitises approximately 7200 pre-summed analogue calorimeter signals at the bunch-crossing rate of 40 MHz, and identifies the specific bunch-crossing of the interaction using a digital filtering technique. Pedestal subtraction and noise suppression applied, and final calibrated digitised transverse energies are transmitted in parallel to the two subsequent processor systems. Several channel-dependent parameters require setting in the PreProcessor system to provide these digital signals, aligned in time and properly calibrated. The different techniques which are used to derive these parameters are described, along with the quality tests of the analogue input signals and the status of the energy calibration.

Parallel Session B4 - Power, Grounding and Shielding / 56

Experimental studies towards a DC-DC conversion powering scheme for the CMS silicon strip tracker at SLHC

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The distribution of power to the CMS tracker upgrade at SLHC is challenging, as the power consumption is expected to be similar as or higher than today, while the operating voltage will decrease and the cables must remain the same.
The CMS tracker has adopted parallel powering with DC-DC conversion as baseline solution to the powering problem.

The current status of the implementation of DC-DC converters into the CMS strip tracker at SLHC phase-2 will be presented. The presentation will include measurements with current tracker structures and custom converter PCBs, studies of the noise coupling and detector susceptibility (e.g. with the Bulk Current Injection method), and simulations of the effect of various powering schemes on the tracker material budget.

POSTERS SESSION / 57

The Control System for a new Pixel Detector at the sLHC

Author: Jennifer Boek[1]

Co-authors: Christian Zeitnitz [1]; Peter Kind [1]; Peter Maettig [1]; Susanne Kersten [1]

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For the sLHC upgrade a new ATLAS Pixel Detector is planned, which will require a completely new Control System.
The requirements, a first concept and a layout will be presented. We will focus on a control chip which necessarily has to be implemented in the new Detector Control System. A setup of discrete components has been built up to investigate and verify the chip's requirements.
First measurements with this setup will be presented.

Summary:

The detector control system (DCS) of the pixel detector has to cover three main tasks. It should ensure the safety of the detector at any time. For all use cases (production, installation, commissioning, calibration, tuning the detector or parts of it) the operator must be provided with tools for control and he should receive feedback. On request the operator should be supported with more detailed information for diagnostics.

Based on these requirements a concept for the Control System for a new pixel detector has been developed with respect to balance between the granularity, the level of reliability and the reduction of radiation length. As the control system depends strongly on the powering scheme of the detector, its development handles two powering options: the serial powering and the DC-DC conversion.

To cover all these needs, the system is structured into different parts. For reliability issues, the interlock path is a completely independent circuit which ensures the safety of the detector at all times. Information for debugging is provided by monitoring values which can optionally be transmitted by the front end electronics via the data path. Control and feedback is required for the supply voltages of the detector modules, and the status of the end of stave controller and of the opto electrical receiver units. The front end unit of this path will be a dedicated DCS chip.

To avoid the routing of all cables to the outside, the DCS chip has to be designed to measure the DCS values as close as possible to the load and to the control units where necessary. The goal is to have one DCS chip design which can fulfill all measurement and control tasks. The chips will be located at various positions in the pixel package for their
different purposes.

A setup of discrete components, the COntrol BOard for the stave emuLaTor (COBOLT) has been built up to investigate and verify the chip's requirements. Various measuring circuits were realized and different communication protocols studied. First results were presented.

POSTERS SESSION / 58

Measurement of the performances of a Low-Power Multi-Dynamics Front-End for Neutrino Underwater Telescope Optical Modules

Authors: Domenico Lo Presti[1]; Giovanni Valerio Russo[1]; Luigi Caponetto[2]; Nunzio Randazzo[3]

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A proposal for a system to capture signals in the Optical Module of an underwater neutrino telescope is described, with focus on power consumption and dynamics considerations. All considerations regarding the signals and their acquisition are made starting from the most general hypothesis possible, so that they will be valid for any underwater Cherenkov neutrino telescope.
A front-end board, the FE-ADC, using a commercial ADC, has been designed and realized. It is aimed at the demonstration of the advantages of the proposed architecture fitting the specifications of power dissipation, multi input dynamics and signal reconstruction has been realized.
The performances of this board have been accurately measured, both stand alone and coupled to the PMT foreseen by the NEMO collaboration, and are presented and discussed.
The results meet the requirements and establish the basis for the definitive design of the final front-end architecture employing the SAS (Smart Analogue Sampler) chip.

Summary:

In order to validate the proposed architecture, a front-end board has been designed. All the functionalities foreseen for the final front-end board have been implemented. The sampling and A/D conversion of the PMT interface output signal are performed by a commercial 200 MHz 12 bit ADC. The ADC output data are stored in a FIFO inside a FPGA only when a suitable validation signal occurs. In this way it is possible to perform zero suppression and minimize dead time. Together with the data, the classification and the 200MHz time stamp must be transferred. The data transmission mechanism is the same developed, and full working, in the front-end board used in NEMO Phase1 [1].
This FE-ADC board test is thought in order to measure the overall performances and to verify that the technological and architectural choices are fully compliant with the mechanical and experimental specifications. The total power dissipation is about 1 W measured with a 5 V power supply.
All the results are extremely important for the design of the front board containing the SAS chip. Actually all the architectural solution foreseen for the SAS front-end board have been implemented in the front end board.
The SAS chip will be sent to foundry for production in March 2009. The SAS chip will allow for a further power dissipation reduction of a factor 3.

Parallel session A1 - ASICs / 59

Front-End Electronics for Pixel Detector of the PANDA MVD.

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Co-authors: Angelo Rivetti [2]; Daniela Calvo [2]; Giovanni Mazza [2]; Marco Mignone [2]; Paolo De Remigis [2]; Richard Wheadon [2]

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ToPix 2.0 is a prototype in a CMOS 0.13 μm technology of the front-end chip for the hybrid pixel sensors that will equip the Micro-Vertex Detector of the PANDA experiment at GSI.

The Time over Threshold (ToT) approach has been employed to provide a high charge dynamic range (up to 100 fC) with a low power dissipation (15 μW/cell).
In an area of by 100 μm×100 μm each cell incorporates the analog and digital electronics necessary to amplify the detector signal and to digitize the charge information. ToPix 2.0 includes 320 pixel readout cells organized in four columns and a simplified version of the end of column readout.

Summary:

The PANDA experiment at the future FAIR facility under construction at GSI, Darmstadt, will exploit the antiproton-proton and antiproton-nucleus reactions for precise QCD studies.
The Micro Vertex Detector (MVD) is located in the innermost part of the experimental apparatus and will consist of silicon pixel and silicon strip detectors to obtain precise tracking of all charged particles. A custom solution for the readout of the pixel detector is motivated by the high track density (up to 12.3 MHz/cm²) and the absence of a trigger signal.
The front-end ASIC, named ToPiX, will provide the time position of each hit with a resolution of 6 ns rms and a measure of the charge released. The final implementation will consist of a matrix of 100x100 cells with a pixel size 100x100 μm², thus covering a 1 cm² active area.
A reduced scale prototype, ToPix 2.0, in a CMOS 0.13 μm technology has been designed and tested. The prototype includes two columns of 128 pixel cells, two columns of 32 cells and a simplified version of the end of column readout.
Each cell incorporates the analog and digital electronics necessary to amplify the detector signal and to digitize the charge information.
The Time over Threshold (ToT) approach has been employed to provide a charge dynamic range up to 625.000 electrons, corresponding to 2.25 MeV of energy lost in silicon, with a power dissipation of 15 μW/cell from a 1.2 V power supply.
The ToT technique permits to saturate the pre-amplifier but in this way the cross-talk increases. The small discharging feedback current (5 nA) has implication on the uniformity between the different channels. This two issues will be analysed in detail.
The pixel cell input stage is a gain-enhanced cascode amplifier with a feedback capacitor and a constant current discharge circuit. A low frequency differential amplifier in feedback with the input stage allows for leakage current compensation. The output signal time could be up to 18 μs, and this imposes a strong constraint of the low-frequency cut-off.
The input stage is followed by a comparator based on a folded cascode architecture. A configuration register is used to store the DAC values to adjust the comparator threshold voltage and configure the input amplifier to accept the selected signal polarity. The control logic receives the signal from the comparator and stores the value on the time stamp bus at the rising and falling edge in the 12 bit le and te registers.
The pixel matrix is organized into columns. Each column has its separate readout logic made in a fixed priority scheme to read the timestamps of the pixel cells and to read/write the configuration bits. The master clock frequency is 50 MHz.
The test results will be discussed in detail in the presentation and show that the key design goals have been achieved. Ongoing studies to improve further the analog performance will also be addressed.

Parallel session B2a - Production, testing and reliability / 60

Replacing full custom DAQ test system by COTS DAQ components on example of ATLAS SCT readout

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[2] *DPNC, University of Geneva*

A test system developed for ABCN-25 for ATLAS Inner Detector Upgrade is presented. The system presented is based on commercial off the shelf DAQ components by NI and foreseen to aid in chip characterization and module/hybrid development complementing full custom VME based setups. The key differences from the point of software development are presented, together with guidelines for developing high performance LabVIEW code. Some real-world benchmarks will also be presented

together with chip test results. The presented tests show good agreement of test results between the setups, as well as agreement with design specs of the chip.

Summary:

Characterization of the engineering run ASICs from first wafers as well as further testing detector modules need robust test systems, including both fast digital communication as well as intricate analogue measurements (analogue measurements being performed predominantly in R&D phase of the components' design). The key property of the system changes fluently from flexibility in the first test stages to speed and reliability for the commissioned collaboration approved test system in later stages. Previous generations of chips used in the LHC experiments were usually tested with state-of-the-art custom systems built specifically for this particular purpose, with significant fraction of total project work-hours being devoted to building accompanying electronics.

Few years ago there were no readily available commercial DAQ components with performance sufficient for extensive mixed-mode testing of components at 40 MHz. Using commercially available DAQ components for digital communication with device under test is now possible with relative ease with digital communication between the test system and DUT with frequencies well above the mentioned base LHC frequency of 40MHz. The electronics designed for the upgrade of ATLAS Inner Detector Readout is foreseen to transmit data with up to 160Mbps data rate, which is still achievable with relatively affordable off-the-shelf DAQ equipment.

This paper describes the system developed for testing prototype ABCN-25 chips with help of National Instruments high speed digital input-output card within LabVIEW environment. The heart of the system is NI6562 PCI/PXI module being in principle high speed (up to 200/400Mbps per channel SDR/DDR) 16 channel digital communication LVDS-standard board. The device is equipped with 32MB on-board memory and provides hardware timed, synchronous, hardware triggered generation and acquisition of LVDS signals, compatible with signals used by ABCN chip outside world communication. The performance of the NI6562 card is sufficient to test current prototype of ABCN chip with typical 80Mbps data rate (single edge) as well as future electronics (module controller chip) operating at 160 Mbps. Both the generation of stimuli and getting the response is done using the same device, without signal integrity and synchronization problems. The presented system provides base for testing both single chips as well as assemblies of up to 7 bidirectional data links in typical 80 MHz data transmission clock, 40 MHz master BC clock scenario. Each data link may read and drive many readout chains of many chips each, hence the suitability of the system to perform hybrid and module system level checks as well as in various unit test scenarios required (e.g. serial powering scheme testing).

The presented results show usability and flexibility of the COTS DAQ based setup. Agreement between the setups used is shown, as well as some benchmarks showing the pros and cons of COTS and custom based approach.

Parallel Session B3 - Packaging and Interconnects / **62**

Prototype flex hybrid and module designs for the ATLAS Inner Detector Upgrade utilising the ABCN-25 readout chip and Hamamatsu large area Silicon sensors.

Author: Ashley Greenall[1]

[1] *Department of Physics*

We will present the development of prototype flex hybrids and modules for the short strip layers of the ATLAS inner detector upgrade. The hybrid utilises the ABCN-25 front end readout chip, which has been optimised for the short 2.5cm strip sensor topology. The design and production choices for a high yield, low cost reliable device will be discussed. Preliminary results from the first prototype hybrids and the first short strip module demonstrator, featuring a 10cm x 10cm Hamamatsu sensor with 4 x 1280 strips read out by 40 readout chips, will be presented.

We will also discuss the future plans for the development of a mass-producible, non-rigidised flex circuit that can be glued directly onto the silicon sensor for integration onto a stave structure.

Summary:

For the SLHC upgrade of the ATLAS inner detector, over 10 000 short strip modules will have to be produced in a relatively short production time of 2 years. From the outset, it is important that yield and reliability issues are addressed to ensure that both electrical and mechanical operation are not compromised. Consideration should also be made for the physics requirements of minimising the material used in the module construction.
The design of the hybrid is implemented using multi-layer Cu-polyimide flex-circuit technology. A staged design approach has been adopted for the hybrid; firstly, a non-aggressive design was implemented to allow evaluation of the readout chip and sensor in an optimal electrical environment. The second design stage follows a more aggressive route of reducing hybrid mass by the removal of surface mounts, power planes, etc. It is also aimed to be more focused on a non-rigidised layout for mass production that is compatible with stave structures.
The flex hybrid architecture has been designed to be able to exploit the features of the new ABCN-25 readout chip without compromising performance. The circuit design rules have had to be chosen to take into account trace characteristic impedance, the number of drops on a loaded electrical bus, etc. Such considerations are necessary to ensure the reliable propagation of digital signals operating at 80Mb/s (though future designs may also operate at the higher speed of 160Mb/s). Compatibility has been maintained for either serial power distribution or DC-DC powering schemes.
Discussion of the design choices made, their features and characterization will be presented. We will also present the electrical characterization and performance of a fully populated single flex hybrid (comprised of 20 x ABCN-25 chips). Furthermore, results from the first full short strip module demonstrator utilizing 2 hybrid circuits coupled up to a 10cm x 10cm sensor produced by Hamamatsu will also be presented.
For the current ATLAS upgrade, the modules consist of two non-rigidised flex hybrids directly glued to a sensor, the design and studies necessary will be discussed. From initial studies, results on the affects of directly gluing onto the segmented sensor faces using Fuller Epolite 5313 epoxy will be shown. Depending upon the success of the program, first results with a non-rigidised hybrid/module will be shown.

POSTERS SESSION / 63

ATLAS Silicon Microstrip Tracker Operation

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The ATLAS experiment at the CERN Large Hadron Collider (LHC) has started taking data last autumn with the inauguration of the LHC. The SemiConductor Tracker (SCT) is the key precision tracking device in ATLAS, made up from silicon micro-strip detectors.
The completed SCT has been installed inside ATLAS. Since then the detector was operated for many months under realistic conditions. Calibration data has been taken and analysed to determine the noise performance of the system. In addition, extensive commissioning with cosmic ray events has been performed both with and without magnetic field.
The current status of the SCT will be reviewed, including results from the latest data-taking, and from the detector alignment. The SCT commissioning and running experience will then be used to extract valuable lessons for future silicon detector projects.

Summary:

The ATLAS experiment at the CERN Large Hadron Collider (LHC) has started taking data last autumn with the inauguration of the LHC. The SemiConductor Tracker (SCT) is the key precision tracking device in ATLAS, made up from silicon micro-strip detectors processed in the planar p-in-n technology.

The completed SCT has been installed inside the ATLAS experimental hall. Since then the detector was operated for many months under realistic conditions. Calibration data has been taken and analysed to determine the noise performance of the system. In addition, extensive commissioning with cosmic ray events has been performed both with and without magnetic
field. The cosmic muon data has been used to align the detector, to check the timing of the front-end electronics as well as to measure the hit efficiency of modules. Sensor behaviour in magnetic field Lorentz angle has been also studied from the data taken. For the initial running with unfocussed LHC beam operation with undepleted sensors is foreseen. Efficiency and noise determination for various bias voltages was also performed. One recent cosmic ray event with hits in the entire Inner Detector (Pixels, SCT and TRT) is shown in Figure 1.
The current status of the SCT will be reviewed, including results from the latest data-taking periods and from the detector alignment. We will report on the commissioning of the detector, including overviews on services, connectivity and observed problems. The SCT commissioning and running experience will then be used to extract valuable lessons for future silicon strip detector projects.

POSTERS SESSION / 64

The GBT-SCA, a radiation tolerant ASIC for detector control applications in SLHC experiments

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Co-authors: Alessandro Marchioro [2]; Antonio Ranieri [3]; Giuseppe De Robertis [3]; Kostas Kloukinas [2]; Paulo Moreira [2]; Sandro Bonacini [2]

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This work describes the architecture of the GigaBit Transceiver – Slow Control Adapter (GBT–SCA) ASIC suitable for the control and monitoring applications of the embedded front-end electronics in the future SLHC experiments. The GBT–SCA is part the GBT chipset currently under development for the SLHC detector upgrades. It is designed for radiation tolerance and it will be fabricated in a commercial 130 nm CMOS technology. The paper discusses the GBT-SCA architecture, the data transfer protocol, the ASIC interfaces, and its integration with the GBT optical link.

Summary:

The GBT–SCA is one the components of the GBT system chipset. It is proposed for the future SLHC experiments and is designed to be configurable matching different frontend system requirements. The GBT-SCA is intended for the slow control and monitoring of the embedded frontend electronics and implements a point-to-multi point connection between one GBT optical link ASIC and several frontend ASICs. The GBT-SCA connects to a dedicated electrical port on the GBT ASIC that provides 80 Mbps of bidirectional data traffic. If needed, more than one GBT-SCA ASIC can be connected to a GBT ASIC thus increasing the control and monitoring capabilities in the system. The GBT-SCA ASIC features several I/O ports to interface with the embedded front-end ASICs. There are 16 I2C buses, 1 JTAG controller port, 4 8-bit wide parallel-ports, a memory bus controller and an ADC to monitor up to 8 external analog signals. All these ports are accessible from the counting room electronics, via the GBT optical link system. Special design techniques are being employed to protect the operation of the GBT-SCA against radiation induced Single-Event-Upsets to a level that is compatible for the SLHC experiments.
The paper will present the overall architecture of the GBT-SCA ASIC describing in detail the design of the peripheral controllers for the individual I/O ports, the network controller that implements the connectivity with the GBT ASIC and will discuss the operation modes and the flow of information between the control electronics and the embedded front end ASICs.

Parallel session A2 - ASICs / 65

Design of High Dynamic Range Digital to Analog Converters for Calibration of the CALICE readout electronics

Author: Laurent Gallin-Martel[1]

Co-authors: Daniel Dzahini [1]; Fatah Rarbi [1]; Jean Yves Hostachy [1]; Olivier Rossetto [1]

[1] *LPSC/IN2P3 Grenoble*

The ILC ECAL front-end chip will integrate many functions of the readout electronics including a DAC dedicated to calibration. We present two versions of DAC with respectively 12 and 14 bits, designed in a CMOS 0.35µm process. Both are based on segmented arrays of switched capacitors controlled by a Dynamic Element Matching (DEM) algorithm. A full differential architecture is used, and the amplifiers can be put into a standby mode reducing the power dissipation. The 12 bit DAC features an INL lower than 0.4 LSB at 5MHz, and dissipates less than 7mW. The 14 bit DAC is an improved version of the 12 bit design.

Summary:

The ILC ECAL front-end chip will integrate many functions of the readout electronics. Due to mechanical constraints, no package will be used and the dies have to be located in cavities dogged in the printed circuit board. Consequently the electronics has to be fully integrated and no discrete components can be used. This multi-channel chip also requires a high dynamic DAC dedicated to calibration. Since calibration process can be carried out at intermediate frequencies, the key issues for such a DAC are the INL and the power consumption. Switched capacitor DAC are well suited to meet these requirements. The linearity of a design implemented in standard CMOS process is limited by the matching errors of its analogue components. For more than 10 bit the required capacitor matching is difficult to obtain and linearization techniques have to be used. High resolution over-sampled delta sigma converters commonly use a DEM algorithm to cancel the matching errors. The DEM allows such DAC to turn the harmonic distortion into noise which is then reduced by a low pass filter. When used in a calibration process the DAC has to provide a sequence of DC values, each value corresponding to a calibration point. In this case the DEM can be effective if several samples are accumulated for each calibration point. The mean value of the resulting distribution will provide with accuracy the output value of the circuit under calibration.
The aim of the first design was to reach a 12 bit resolution. This dynamic range is below the ILC ECAL requirements but will allow the design methodology to be validated. This full differential DAC comprises two 6 bit capacitor arrays connected together through a segmentation capacitor. The network stores a charge proportional to the DAC input code. This charge is then shared with a feedback capacitor using Direct Charge Transfer (DCT). The DCT architecture exhibits two important advantages. At first, the OTA does not have to charge the feedback capacitor and its power consumption can be maintained low even for large capacitor values. Moreover, the charge sharing also acts as a first order low pass filter that reduces the noise induced by the DEM. The test result shows that the DEM allows the chip to reach a 12 bit resolution. The DAC features an INL lower than 0.4 LSB up to a 5MHz frequency. The power consumption is lower than 7mW.
The 14 bit design is also based on segmented arrays of switched capacitors performing DCT with a feedback capacitor. The 14 bits are divided into three sub-arrays: 5 MSB, 5 ISB (Intermediate Significant Bits) and 4 LSB. The DAC integrates two OTA, the first one processes the ISB and LSB arrays and the other one is dedicated to the MSB array. Compared to the first design, this topology dramatically reduces the sensitivity to parasitic capacitors. The test of this 14 bit design will be carried out in the forthcoming weeks and the results will be presented.

Parallel Session A5 - ASICS / 66

A 5 Gb/s Radiation Tolerant Laser Driver in 0.13 um CMOS technology

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A laser driver for data transmission at 5 Gb/s has been developed as a part of the GigaBit Transceiver (GBT) project. The GigaBit Laser Driver (GBLD) targets High Energy Physics (HEP) applications for which radiation tolerance is mandatory.
The GBLD ASIC can drive both VCSELs and some types of edge emitting lasers. It is essentially composed of two drivers capable of sinking up to 12 mA each from the load at a maximum data rate of 5 Gb/s, and of a current sink for the laser bias current. The laser driver also include pre-emphasis and duty cycle control capabilities.

Summary:

The GBT project aims to design a radiation tolerant optical transceiver at 4.8 Gb/s for the future upgrades of the LHC experiments. The GBT will be able to transmit and receive data, trigger signals and control information, thus acting as an interface between the front-end electronics and the data acquisition, trigger and detector control systems.
The GBT chip set will include a laser driver, named GBLD, targeted at driving both VCSELs and some types of edge emitting lasers. The circuit is designed for both single ended and differential connection.
A GBLD prototype has been designed and is currently under test. The prototype is designed for a maximum output data rate of 5 Gb/s and is composed of two drivers and a current sink for the laser bias current. Each driver can sink between 2 and 12 mA from the load with a 50 Ω output impedance. The current sink is controlled by a 6 bits DAC. The two drivers can be connected in parallel, thus doubling the maximum output current and halving the output resistance. The latter configuration is better suited for edge emitting lasers. The laser bias current can be adjusted between 2 and 43 mA via an 8 bit DAC.
Pre and de-emphasis can be independently set on the rising and falling edges of the signal, in order to compensate for the bandwidth limitations of the optoelectronic components and transmission media employed. The emphasis can be adjusted both in height (between 0 and 12 mA) and in width (between 60 and 90 ps) by 4 and 2 bits DACs, respectively. The laser response can also be compensated by a duty cycle control circuit, controlled by a 3 bits DAC. The duty cycle control range is around 20% at 5 Gbps.
The driver architecture is based on a sequence of differential stages with resistive load. For the predriver the inductance peaking technique has been used in order to improve the bandwidth. Two 1 nH spiral inductors have been integrated.
The control DACs can be programmed via a I2C digital interface. Seven 8-bits control registers are used to store the configuration parameters. The control logic has been designed in order to be resistant to Single Event Upsets (SEUs) via Triple Modular Redundancy (TMR). An asynchronous correction logic has been adopted in order to provide error correction when the I2C clock is not present.
The chip has been designed in a CMOS 0.13 μm technology. The chip size is 2×2 mm2 and is packaged in a 5×5 mm2 QFN28 package. Double bonding has been used on the supply and high speed signals in order to decrease the bonding wire inductance.
This work describes in detail the operation principles of the GBLD circuits and the experimental results.

Parallel Session B5 - Optoelectronics and Links / 67

The GBT project

Author: Paulo Moreira[1]

[1] *CERN*

The GigaBit Transceiver (GBT) architecture and transmission protocol has been proposed for data transmission in the physics experiments of the future upgrade of the LHC accelerator, the SLHC. Due to the high beam luminosity planed for the SLHC the experiments will require high data rate links and electronic components capable of sustaining high radiation doses. The GBT ASICs addresses this issue implementing a radiation-hard bi-directional 4.8 Gb/s optical fibre link between the counting room and the experiments. The paper describes in detail the GBT architecture and will present an overview of the various components that constitute the GBT chipset.

Summary:

The GBT collaboration is working on the development of a full-custom radiation-hard chipset (the GBT chipset) to implement high-speed (4.8 Gb/s) optical links between the counting room and the experiments' sub-detectors. The GBT will implement point-to-point duplex links allowing bidirectional data transmission between the counting room and the detectors. It is designed so that the large bandwidth of a single optical fibre link can be shared among several frontend devices by providing up to 40 electrical links (E-Links) between the GBT chipset and the frontend ASICs. These E-Links are bit rate programmable and will thus accommodate different requirements in terms of bandwidth and number of interconnects between the frontend ASICs and the GBT chipset. The flexibility provided by the possible E-Link configurations will easily allow the GBT chipset to serve a variety of detector topologies and bandwidth requirements.
The GBT architecture is tailored to support simultaneous transmission of physics, trigger and experiment control data over the same link. The GBT will act thus simultaneously as a data-link and as a TTC transceiver incorporating many of the functions that traditionally have been separated physically and functionally in data-acquisition, timing, trigger and experiment control links.
Due to the high beam luminosity of the SLHC the radiation doses are expected to reach the 100 Mrad level for some of the inner detectors. These high levels of radiation will pose long term reliability problems to the electronics due to total dose effects which can be minimized by using advanced CMOS commercial technologies and by following special layout techniques previously developed for the LHC ASICs. The GBT ASICs will be thus fabricated in a commercial 130 nm technology which will ensure the required radiation tolerance. The high luminosity will also be linked to a high rate of the Single Event Upsets (SEU). These are a major impairment to error free data transmission at high data rates. To deal with this situation the GBT adopts a robust error correction scheme that will allow the correction of bursts of errors caused by SEUs on photodiodes and on the electronic circuits. The data communications protocol was chosen so that it is possible to develop compatible firmware in most standard FPGAs existing today in the market thus enabling the implementation of GBT compatible transceivers within FPGAs mounted in the counting rooms where radiation tolerance is not required.
The development of this architecture has gained acceptance among the High Energy Physics (HEP) community working for SLHC and the project has been approved as DG white paper project in 2008. During 2008 to date several ASIC and FPGA developments have taken place that will be introduced in the paper. The proposed architecture, the communications protocol will be described in detail and the project organization and schedule will be presented.

POSTERS SESSION / 68

Upgrade of the Cold Electronics of the ATLAS HEC Calorimeter for sLHC: Generic Studies on Radiation Hardness and Temperature Dependence.

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The signal amplification and summation electronics of the ATLAS Hadronic End-cap Calorimeter (HEC) is operated at the circumference of the HEC calorimeters inside the cryostats in liquid argon. The present electronics is designed to operate at irradiation levels expected for the LHC. For operation at the sLHC the irradiation levels are expected to be a factor 10 higher, therefore a new electronic system might be needed. The technological possibilities are investigated.

From irradiation tests of the present HEC electronics it is known that it will operate up to a dose of 55 kGy of ionizing radiation and up to a neutron fluence of 3 * 10**14 n/cm**2, where it shows some degradation of performance. This matches well the requirements of up to 1.5 * 10**13 n/cm**2 for 10 years of LHC operation, including safety factors. For a subsequent sLHC running phase with 10 times higher expected irradiation levels, a more radiation hard HEC electronics will be needed.

Therefore generic studies of different technologies have been carried out at the transistor level to understand the radiation hardness up to integrated neutron fluxes of ~2*1016 n/cm**2 and the behaviour during operation at cryogenic temperatures. The S-parameter technique has been used

to
monitor the performance e.g. of gain and linearity during irradiation at room temperature. In addition, DC measurements before and after irradiation have been compared. Results of these tests and of accompanying noise tests are reported. In addition, results of S-parameter measurements will be reported operating the transistors in liquid nitrogen. Conclusions are drawn and the potential is assessed on the viability of using the tested technologies for carrying out the design of new HEC cold electronics for the sLHC.

Summary:

The signal amplification and summation electronics of the ATLAS Hadronic End-cap Calorimeter (HEC) is operated in liquid argon at the circumference of the HEC calorimeters inside the cryostats. The present electronics is designed to operate at irradiation levels expected for the LHC. For operation at the sLHC the irradiation levels are expected to be a factor 10 higher, therefore a new electronic system will be needed. The technological possibilities are investigated.

The basic element of the cold HEC electronics is an integrated chip consisting of eight preamplifiers and two summing amplifiers. The concept of 'active pads' is employed, i.e. each preamplifier is connected to one pad of the calorimeter cells, the individual signals being amplified. The read-out channels are formed by summing signals from 2/4/8 or 16 pads to the required output granularity with subsequent amplification. This concept results in an optimal signal to noise ratio.

The HEC electronics has to fulfil two stringent requirements: It has to operate in liquid argon (~87 K) and it has to operate reliably in the radiation levels of the end-cap calorimeter region.

There are more detailed requirements, among those:
• The power consumption of the chip should not exceed the present level of < 0.2 W in order to avoid boiling of LAr;
• the gain difference between individual preamplifier channels of one IC has to stay below 1% since the electronic calibration is done at the level of the summed read-out channel;
• the gain difference of a read-out channel between operation in warm and cold should not be more than a factor of 2 since most QC tests have to be done in warm;
• the noise level should not exceed the present low level;
• the dynamic range of the preamplifier has to be 12-bit, that of the summing amplifier 13-bit;
• the IC has to be safe with respect to potential HV discharges in the gaps of the HEC. April 2-3,

From irradiation tests of the present HEC electronics it is known that it will operate up to a dose of 55 kGy of ionizing radiation and up to a neutron fluence of 3 * 10**14 n/cm**2, where it shows some degradation of performance. This is about a factor of 20 above the expected neutron fluence of 1.5 * 10**13 n/cm**2 for an operation of 10 years at LHC. It will take at least one year of LHC operation at a sizeable luminosity to determine the irradiation levels in situ. Therefore, presently a safety factor of 10 has been assumed to take all systematic uncertainties into account. Within this safety factor, the present electronics matches well the LHC requirements. For 10 years of sLHC operation at a luminosity of 10**35 /cm**2/s the chips have to survive ten times higher radiation levels: γ dose 50 kGy, 1.5·10**14 n/cm**2, 1.2·10**12 p/cm**2. A new radiation hard HEC electronics will be needed.

Therefore generic studies of different technologies have been carried out at the transistor level to understand the radiation hardness up to integrated neutron fluxes of *~21016 n/cm**2 and the behaviour during operation at cryogenic temperatures.

The following technologies have been studied: Bipolar SiGe (IHP 250 nm, IBM 130 nm, AMS 130 nm, Sirenza), CMOS Si (IHP 250 nm n and p), GaAs MESFET and HEMT (Triquint 250 nm, Sirenza 250 nm). The S-parameter technique has been used to monitor the performance e.g. of gain and linearity during irradiation at room temperature. In addition, DC measurements before and after irradiation have been compared. Results of these tests and of accompanying noise tests are reported. In addition, results of S-parameter measurements will be reported operating the transistors in liquid nitrogen. The dynamic range requirements pose a scrutinizing test on the technologies.

Conclusions are drawn and the potential is assessed on the viability of using the tested technologies for carrying out the design of new HEC cold electronics for the sLHC.

Parallel Session A5 - ASICS / **70**

A latchup topology to investigate novel particle detectors

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Here is described a novel approach to detect particles by means of a solid-state device susceptible to latchup-like effects. The stimulated ignition of latchup effects caused by external radiation has so far proven to be a hidden hazard. Here this is proposed as a powerful means of achieving the precise detection and positioning of a broad range of ionising particles. The cell can be constructed using state-of-the-art CMOS technologies. Thus, whenever this structure ignites upon charge detection, whatever its origin, a latchup condition is stated and this is a starting point for future pixel device designs.

Summary:

The paper describes an innovative idea for an ionizing particle detector. This is an alternative topology for a solid-state pixel detector. It is based on latchup effect, which is usually exploited as a dangerous hazard in solid-state electronic devices and is common in to-date CMOS technologies working in a radiation environment. Review of the latch up effect, description of the circuit topologies under investigation to assess the operating principle and initial experimental results will be presented. In principle the detector can operate at room temperature, does not require a high voltage power supply and is intrinsically more tolerant to radiation effects than the common solid-state detectors based upon reverse-biased junctions. In fact, a latchup-based detector can be easily constructed using state-of-the-art CMOS technologies. A prototype made up of discrete components is described and its rough sensitivity is exploited. Tests with daylight, electrons, via a current pulse generator and with a laser beam have proved that charge sensitivity of the order of 1 pC can be easily achieved. This seems to be very promising for future applications in particle detectors or signal readout systems, being the threshold already very precise (low noise) using commercial components. All in all, the whole power consumption of the cell is also very low, of the order of 1mW, when it is not ignited. This can be easily understood since the number of components inserted, basically two transistors, one reset switch and some resistors, is much smaller than that of the modern pixel circuits. Hence, it is reasonable to expect even better numbers and results for integrated versions of the latchup circuit. New ideas, circuit topologies and technologies will be presented. Possible applications range from heavy-ion discriminator to beam monitor provided they deposit an over-threshold charge in the cell. Applications in particle and radiation detection will be suggested. Other types of latchup detector studies oriented to low-power applications are ongoing by the authors.

Parallel Session A3 - Trigger / **71**

LHCb Level 0 Decision Unit

Authors: Hervé Chanal[1]; Régis Lefèvre[1]

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The Level 0 Decision Unit (L0DU) is one of the main components of the first trigger level of the LHCb experiment. This 16 layers custom board receives data from the calorimeter, muon and pile-up subtriggers and computes the level 0 decision, reducing the rate from 40MHz to 1MHz. The processing

is implemented in FPGA using a 40MHz synchronous pipelined architecture. The L0DU algorithm is fully configured via the Experiment Control System without any firmware reprogramming. An overall L0DU latency of less than 450ns has been achieved. The board was installed in the experimental area in April 2007. It has played a major role in the commissioning of the experiment.

Summary:

The trigger of the LHCb experiment is based on two levels. The first one, called level 0, makes use of custom electronics and should reduce the rate from 40MHz to 1MHz. The second trigger level, called High Level Trigger (HLT), is implemented on a farm of CPU.
The Level-0 Decision Unit (L0DU) is the central part of the first trigger level. The L0DU receives information from the calorimeter, muon and pile-up sub-triggers at 40MHz. The sub-triggers send their data via 17 high speed optical links transmitting at 1.6Gb/s. Each contains 16bits@80MHz of data with its particular clock. The L0DU is designed to cope with up to 24 such input links.
The L0DU computes the level 0 decision and sends it to the Readout Supervisor using a dedicated 40MHz LVDS link. The Readout Supervisor can veto the decision depending on the electronic workload. When an event is accepted, the L0DU sends an explanation block to the HLT. This block contains the kind of triggers fired by the event and is the starting point of the HLT processing.
The L0DU is plugged on a TELL1 board which is the standard Data Acquisition interface module used in LHCb. The TELL1 board interfaces the Timing and Trigger Control and the Experiment Control System (ECS) via a small embedded PC.
The L0DU is a full custom 16 layers board. The processing is implemented in 3 FPGA in BGA package using a 40MHz synchronous pipelined architecture. A smaller FPGA is dedicated to the synchronization and the ECS. The processing is done in two larger FPGA. It is split in two: a pre-processing block and a trigger definition block. The pre-processing block acquires and time-aligns the input data. It also handles specific counters to monitor the status of the links and check the time-alignments.
The trigger definition block implements up to 128 configurable comparisons. These elementary conditions are then combined using up to 32 fully configurable 'and' networks. This defines the trigger channels. The decision is finally built as the result of an 'or' network on the 32 trigger channels. This 'or' network is also configurable to enable or not any trigger channel. Between the 'and' and the 'or' networks, each trigger channel can be downscaled with a downscaling factor configurable in steps of 0.1%. The trigger definition block also implements its own counters to monitor the various trigger rates.
The overall L0DU latency is lower than 450ns. The trigger definition block is very flexible. It is fully set up via ECS. The L0DU can then cope with very different running conditions or physical priorities without any firmware reprogramming.
The L0DU board has been installed in the experiment in April 2007. It has played a major role in the commissioning of the experiment in general and of the level 0 trigger in particular. The first cosmic events were recorded in late 2007 triggering on calorimeter data. A cosmic trigger based on tracks reconstructed in the muon system was setup in spring 2008. Dedicated configurations of the L0DU also allowed triggering and recording beam dump events associated to the commissioning of the LHC itself in summer 2008.

Parallel Session B3 - Packaging and Interconnects / **72**

3D electronics for hybrid pixel detectors

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Facing the future challenges of hybrid pixel vertex detectors is foreseen to be done by microelectronic technology shrinking. However, this straightforward approach has some disadvantages in term of performances and cost. Based on a previous prototype of the future ATLAS pixel read-out chip FE-I4,

this paper presents design and test of a hybrid pixel read-out chip using 3 dimensional electronics technologies which enable to split pixel functionalities into two separate levels.

Summary:

Hybrid silicon pixels detectors featuring high spatial resolution, very good signal to noise ratio and true two-dimensional information are currently used as vertex detectors in High Energy Physic experiments and especially in ATLAS and CMS detectors at the Large Hadron Collider (LHC).
Future requirements of post-LHC accelerators are, as usual, one step beyond the actual ones. Facing these new challenges could be addressed by 3D technologies which offer an alternative way of 2D shrinking with the advantages of technology mixing and cost effectiveness.
Starting from the FE_I4 prototype design (14×61 pixel matrix) in IBM 130 nm, which is a test pixel read-out chip for ATLAS upgrades, we developed 3D variants in Tezzaron-Chartered 130nm technology called FE_TC4.
In these variants, pixel functionalities are split into 2 levels (so-called tiers), the first one housing the analog pixel and sensor connections and the second one sheltering all digital related blocks. These two tiers are then connected face to face by copper bonds and the resulting pixel dimension before any real optimization was scaled down from 50×250µm to about 50×160µm.
One of these 3D circuits contains "special" digital blocks dedicated to the detailed study of the parasitic coupling between tiers, the other one has a more realistic digital design including the "4-pixel region" architecture which is foreseen for ATLAS pixel Front-End IC upgrades.
Silicon sensor has been also designed in order to address bump-bonding issues in this new type of chip stacks.
Design issues and complete tests results will be presented.

POSTERS SESSION / 73

Buffer Control Chip (BCC) for the ATLAS Tracker Upgrade

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The ATLAS Tracker Upgrade project is developing large modules of up to two hybrids each. Each hybrid comprises two columns of ABCN-25 readout ASICs, each with a data rate twice the bunch-clock. A hybrid readout link thus handles two streams at quadruple the bunch-clock rate. To allow hybrids to operate at different potentials (as required by serial-powering), control signals make use of a novel AC coupled DC LVDS scheme. The BCC ASIC, designed to provide signal buffering, clock multiplication and data multiplexing, is described. Functionality, operation and results of testing and integration onto a tracker module will be presented.

Summary:

The ATLAS Tracker Upgrade project has progressed to building large objects nearing the scale and complexity of that is needed for the final system. These comprise 12 modules grouped into a super-module, each module having two hybrids. Each hybrid has 2 columns of ABCN-25 ASICs for reading out the strips. This design introduces a module-controller-chip (MCC) as a means to manage the module. As this component is complex with a long development cycle, an alternative for early testing was developed. The buffer-control-chip (BCC) multiplies the bunch clock and aggrigates data from each column. It also impliments a special AC/DC LVDS buffer.

As there are options for individual hybrids to operate at different potentials (as would be the case with serial powering) it is essential that control signals are AC coupled. To reduce complexity, power and noise generated by always-on balanced coding, a novel DC LVDS over AC method is used. An extra LVDS driver in the receiver feeds-back the signal to hold the input at the state it last transitioned to. These are are being tested for both multi-drop 40MHz
control signals and point-to-point 160MHz readout signalling.

The BCC provides an interface between the off- and on-hybrid signals. As such it receives a 40MHz beam crossing clock (BCO), a command line (COM) and a combined level-1 trigger and reset line (L1R). The ASICs are driven via two clocks - the BCO and a data-clock that is derived from the BCO. The BCC can optionally invert/disable either of these clocks, as well as double the frequency of the data-clock.

The command line is decoded on the BCC, providing multiple functions:
1) Write to the BCC configuration register
2) Readback the BCC configuration register
3) Readback the BCC ID
4) Carry a payload that is forwarded onto the ASICs on either their COM, RESETB or L1 lines

In the readout path, the BCC provides a means of switching to the redundant data output of a column of ASICs. The column data lines are then multiplexed onto the readout data line. An optionally invertable clock is used to sample the data and the phase of the multiplexing clock and various debug modes are provided - accessed via configuration register bits.

The BCC will return from fabrication mid-June 2009. Each die will be bonded to a PCB for testing. When confirmed functional, the PCB will then be bonded to a hybrid for use as part of a module. These results will be presented.

Parallel Session A5 - ASICS / 74

The 8 bits 100 MS/s pipe line ADC for the INNOTEP project

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This paper describes the Analog to Digital Converter developed for the front end electronic of the IN2P3 INNOTEP project by the “pole microelectronique Rhone-Auvergne”. (Collaboration LPC Clermont-Ferrand and IPNL Lyon).

This ADC is a 4 stages, 2.5 bits per stage pipe line, with open loops track and holds and amplifiers. It runs at 100MSamples/s and has 8 bits of resolution. The stages used two lines, the gain line, and the comparison line which runs in current. The main idea of this current line is to make a first step toward current structure and 130nm technology.

Currently, this ADC is designed with a 0,35µm SiGe technology.

Summary:

This paper concerns the 100 MSamples/s ADC developed for the IN2P3 INNOTEP project.
The architecture chosen is a 4 stages pipeline. Each stage is designed with 2.5bits to get an overall resolution of 8 bits.
This architecture needs 6 comparators per stage (for the 2.5bits system), two track and holds, a 3 bits DAC and an amplifier with a good accuracy and a gain of 4.
Each design is fully differential and open loop to minimize the kick back noise and the stability problems.
Two versions are described, the first release which uses one track and hold per stage and has a conversion time of 20ns, and the last release with two track and holds per stage and conversion time of 40ns. The conversion time has increased, but it is not a critical point because the aperture size latency

is the same, 10ns in each version. The second release offers better results than the first in conversion precision.
In each version, a part of the stages uses current structure, to limit the kick back noise
and the charge injections in the 3 bits DAC, and to offer more precision in the open loop gain amplification and reference subtraction.
The choice of handling the signal in current mode instead of in voltage for the comparison and subtraction stage as well as in the DAC is discussed, and simulation results are given. The choice to use two track and holds instead of one is discussed too, with comparisons using simulation results.
Simulations to verify the robustness to the process/matching variations were made.
The Layout is realized for each version, the first version was sent on June 2008 and the second on March 2009. Parasitic simulations were made and are discussed, and the two chips will be tested for the workshop. The test's results will be described, such as measurements of static performances, yield results. Comparisons between test's results and parasitic simulations will be made.

Parallel session A4 - Trigger / **75**

Feasibility studies of a Level-1 Tracking Trigger for ATLAS

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The existing ATLAS Level-1 trigger system is seriously challenged at the SLHC's higher luminosity. A hardware tracking trigger might be needed, but requires a detailed understanding of the detector. Simulation of high pile-up events, with various data-reduction techniques applied, will be described. Two scenarios are envisaged: (a) regional readout - calorimeter and muon triggers are used to identify portions of the tracker; and (b) track-stub finding using special trigger layers. A proposed hardware system, including data reduction on the front-end ASICs, readout within a super-module and integrating regional triggering into all levels of the readout system will be discussed.

Plenary Session 6 - Programmable Logic, Boards, Crates and Systems / **78**

Implementing the GBT data transmission protocol in FPGAs

Authors: Csaba SOOS[1]; Frederic MARIN[2]; Jean-Pierre CACHEMICHE[2]; Paulo MOREIRA[1]; Sophie BARON[1]

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The GBT chip is a radiation tolerant ASIC that can be used to implement bidirectional multipurpose 4.8 Gb/s optical links for high-energy physics experiments. It will be proposed to the LHC experiments for combined transmission of physics data, trigger, timing, fast and slow control and monitoring. Although radiation hardness is required on detectors, it is not necessary for the electronics located in the counting rooms. Therefore, a study is being made to implement these GBT links on FPGAs. This paper will describe the GBT protocol implementation, the configuration of the transceivers on Altera Stratix II GX and Xilinx Virtex 4, the optimization of resource for multi-transceivers, the first data transmission tests and the source code availability.

Summary:

The GBT chip is a radiation tolerant ASIC that can be used to implement bidirectional multipurpose 4.8 Gb/s optical links for high-energy physics experiments. It will be proposed to the LHC experiments for combined transmission of physics data, trigger, timing, fast and slow control and monitoring. Although radiation hardness is required on detectors, it is not necessary for the electronics located in the counting rooms, where the GBT functionality can be realized using commercial off-the-shelf (COTS) components.
A physical implementation of the protocol has been achieved for FPGA devices in the most versatile way: on Altera and Xilinx devices, in Verilog and in VHDL. It is currently based on Altera Stratix II GX and Xilinx Virtex 4. Stratix IV GX and Virtex 5-6 versions are under study.
This paper will first describe the GBT protocol implementation: scrambling, Reed-Solomon encoding, interleaving for the transmission and de-interleaving, decoding and descrambling for the reception. It will then focus on practical solutions to make Stratix and Virtex transceivers match the custom encoding scheme chosen for the GBT (in particular, the word alignment in the receiver will be treated). Results will be presented on latency, single channel occupancy, resource optimization when using several channels in a chip and bit error rate measurements. Finally, information will be given on how to use the available source code and how to integrate GBT functionality into custom FPGA applications.

POSTERS SESSION / 79

DEPFET Mini-matrix Readout System

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The Mini-matrix readout system is being developing for measuring characteristics of a small (3.5 x 3.5 mm) prototype of a DEPleted Field Effect Transistor (DEPFET) sensor for particle detection. The small sensor will have 8 x 6 active pixels allowing studies of the DEPFET structure behaving and processes during sensor operation. The Mini-matrix readout setup should allow us to make a precision collected charge measurement in each pixel with low noise, charge shearing among multiple pixels, clustering, charge-loss measurement, find optimal voltage values and timing of driving signals and should allow us to make a computer post-analysis as a correlated sampling, averaging, etc.
The system is made of a commercial and custom-made blocks as a PC with an 8-channel 14-bit 125 Msps PCI data acquisition card, FPGA control card, current readout and switching circuit and differential to single-ended converter. The custom-made current readout circuit is made of 8 low noise trans-impedance readout amplifiers and the switching circuit contains 12 individual analog switches that are necessary to control the Gate and Clear electrodes of the DEPFET Mini-matrix sensor.
The measuring system will be controlled and configured by PC. Total input noise should be below 20 e- (electrons). All 8 channels will be digitalized by 14-bit ADCs with 125 Msps for each channel in parallel with frame readout time 20 ⊠s. The switching circuit will have possibility of gate voltages timing with resolution of 10 ns and allows gate signals overlapping. Subtracting voltage for the pedestal current subtraction will be digitally reconfigurable.
The system concept is simple, based on the previous single pixel measuring setups and should provide fast realization and precise results.

POSTERS SESSION / 80

An FPGA-based Emulation of the G-Link Chip-Set for the ATLAS Level-1 Barrel Muon Trigger

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The ATLAS Level-1 barrel muon trigger is built as a synchronous pipeline and includes some high-speed serial links in order to transfer data from the detector to the counting room. The links are based on the GLink chip-set, which transfers data
with a fixed and deterministic latency. Despite its unique timing features, the production discontinued and no compatible off-the-shelf chip-sets are available. The transmission side of the links is buried on-detector and will not be upgraded, however a replacement for the receivers in the counting room in case of failures is needed. We developed a replacement solution for GLink transmitters and receivers, based on the gigabit serial transceivers (GTP) embedded in a Xilinx Virtex5-LXT Field Programmable Gate Array (FPGA). In the LHC experiments, and in general wherever an experiment-wide clock is distributed, our link is able to transmit data with a fixed latency, even after a loss of lock or a power cycle.
We present our architecture, showing the GTP internal configuration and the logic in the FPGA fabric needed for the protocol emulation. We compare the GLink and the GTP transmitter eye-diagrams and we discuss the results of Bit Error Rate (BER) and jitter measurements on hybrid (Glink vs. GTP) and homogeneous (GTP vs. GTP) links.

Parallel Session A3 - Trigger / 81

Integrated Trigger and Data Acquisition system for the NA62 experiment at CERN

Author: Marco Sozzi[1]

Co-authors: Bruno Angelucci [1]; Carlo Avanzini [1]; Gianluca Lamanna [2]; Gianmaria Collazuol [2]; Giuseppe Ruggiero [2]; Guido Magazzu' [3]; Stefano Galeotti [3]; Stefano Venditti [1]

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The TDC based integrated trigger and data acquisition system of the NA62 experiment at CERN will be presented. The system architecture, the trigger algorithm and its implementation in commercial high performance FPGAs will be described. The results of test and characterization of the custom components as well as those of extensive field tests performed on a system prototype handling up to 512 input channels will be discussed.

Summary:

The NA62 experiment at CERN (SPS) will measure the ultra rare Kaon decay to one Pion and two Neutrinos using detectors with sub-nanosecond resolution. Relevant events will be triggered when a minimum amount of hits in time coincidence is detected in the active detectors (e.g.: the RICH) with no hits in others ("vetoes").

The Trigger and DAQ system is based on components designed for the LHC experiments. The building blocks are the High Performance Time to Digital Converter (HPTDC), designed at CERN, which can measure the timing of rising and falling edges ("hits") on 32 input signals with a resolution of 100ps and the TELL1, a general-purpose data acquisition board developed for the LHC-b experiment.

We developed a custom mezzanine board (TDCB) housing 4 HPTDCs; 4 such boards can be plugged on one TELL1 resulting in 512 input channels handled in one VME-9U board.

Each TELL1 is equipped with 4 FPGAs (PP) that handle the readout of the TDCB and the storage of raw data in memory buffers while waiting for the global trigger and implement the trigger algorithm counting hits in time slots of a few nanoseconds. A fifth FPGA (SYNCLINK) combines the outputs of the PP FPGAs and handles the formatting and transmission of trigger and raw data through 4x1Gb Ethernet ports.

TELL1 boards can be daisy-chained and in each SYNCLINK FPGA the local trigger data is combined with that evaluated by the previous element of the chain and transmitted to the next. 2 Ethernet ports are used for this purpose and the other two handle the raw data transfer to PCs.

An embedded processor controls all the devices in the TELL1 and in the TDCBs through JTAG and I2C links. The clock is handled by a TTC-RX device and the clock jitter is reduced by QPLL devices to less than 50ps not to affect the HPTDC time measurements.

The TDCB is equipped with an Altera Stratix II device that handles the configuration of the HPTDCs through a dedicated JTAG port and controls the QPLL. The HPTDC readout can be directly controlled by the PP FPGAs if no data pre-processing is performed in the TDCB FPGA or it can be handled by TDC controllers embedded in the TDCB FPGA if raw data are locally pre-processed (e.g.: timing re-ordering is performed), stored in a local memory buffer and directly accessed by the PP FPGAs. Monitor functions as embedded TDC emulators, hit and error counters, detection of QPLL unlock condition and TDC calibration with external pulses are also handled by the TDCB FPGA.

The TDCB has been fully tested and characterized and results will be shown in this paper. The architecture of the board and the features embedded in the TDCB FPGA will be described in detail as well as the general architecture of the Trigger and DAQ system. Results of the test performed on a prototype of the entire system including a 440 channel detector, Front-End electronics and one fully equipped TELL1 will be also presented.

Parallel session B2a - Production, testing and reliability / **82**

Integrated test environment for a part of the LHCb calorimeter

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Co-authors: Albert Comerma Montells [1]; David Gascón Fora [1]; Eduardo Picatoste Olloqui [1]; Jordi Riera Baburés [1]; Maria del Mar Roselló i Canal [1]; Xavier Vilasís Cardona [1]; Álvaro Gaspar de Valenzuela Cueto [1]

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An integrated test environment for the data acquisition electronics of the Scintillator Pad Detector (SPD) from the calorimeter of the LHCb experiment is presented. It allows to test separately every single board or to perform global system tests, while being able to emulate every part of the system and debug it. This environment is foreseen to test the production of spare electronics boards and help to the maintenance of the SPD electronics along the life of the detector. The heart of the system is an Altera Stratix II FPGA while the main board can be controlled over USB, Ethernet or WiFi.

Summary:

The maintenance of the detector electronics shall become an issue along the LHC life. In effect, it is expected that potentially malfunctioning boards, repaired ones or even productions of new spares will have to be tested. Original test benches may have been dismantled or the original experts designing the board may not be available anymore. For this reasons, automated standalone test benches may be of use: they should allow an operator to diagnose or test a board along the detector lifetime. In this paper, we present such a test bench, for the Scintillator Pad Detector (SPD) of the LHCb calorimeter.
The SPD is the front layer of scintillator tiles of the LHCb calorimeter. The data acquisition electronics is basically divided in three boards: a Very Front End (VFE) board, a Regulator Board, providing the VFE power supply and a Control Board, linking the two to the experiment control system and performing some trigger calculations.
The integrated test system is capable of checking and diagnosing separately each type of board, namely the VFE boards, the Regulator boards and the SPD Control Boards, as well as their connectivity, including tests on a photomultiplier test bench and of the optical links. It can also perform global system tests using the various types of boards interconnected.
The system consists of a main printed circuit board which has connectors for all the boards. The system can be mounted in many different ways, from a completely simulated environment for a single board to a system fully connected to the real detector excepting one link connected to the test board. This is what gives the system its flexibility.
The board uses an Altera Stratix II EP2S60F484C5N mounted on a development board. It also contains 8 LVDS transmitters and 4 receivers at a total of about 8.6Gbps, an optical receiver at about 1.2Gbps and means to test the control cables which include I2C, a clock and a serial high speed link. It has a clock

generator at the exact frequency of the experiment, in order to increase its autonomy.
It all works attached to a computer by USB but it is also prepared to work connected to a network by Ethernet or WiFi. It is possible to adapt the software to use the network connection to control the system. This could be useful to allow users to perform remote tests, but it also opens the possibility of running the control software directly on the board. Running software from the board allows any PC with no specific program or drivers to use the system.
We expect the strong points of the system, such as the capacity to test all types of boards in the SPD, together as well as standalone, the automation of the process and the remote control capacity to prove useful in the years to come for the maintenance of our electronics.

Parallel Session B4 - Power, Grounding and Shielding / 84

KM3NeT Power and Submarine Cable Systems for the kilometre cube Neutrino Telescope

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The KM3NeT EU-funded consortium, pursuing a cubic kilometre scale neutrino telescope in the Mediterranean sea, is developing technical solutions for the construction of this challenging project, to be realized several kilometres below the sea level.
In this framework a proposed DC/DC power system has been designed, maximizing reliability and minimizing difficulties and expensive underwater activities.
The power conversion, delivery, transmission and distribution network will be presented with particular attention to: main electro-optical cable, on shore and deep sea power conversion, subsea distribution network, connection systems, installation and maintenance issue.

Summary:

The KM3NeT consortium, including members of the ANTARES, NEMO and NESTOR collaborations, is developing a kilometre cube-scale neutrino telescope for the Mediterranean sea.
The construction of such a detector will require the solution of technological problems common to many deep submarine installations.
Several hundred vertical detection units containing photomultipliers will be deployed on a seafloor site up to 100 km far from the shore below several kilometres the sea level.
The power system is composed of an AC/DC shore power feeding station, a management and control system, a standard, single conductor 10 kV DC rated electro-optical telecommunications cable with seawater current return and a distribution network to deliver power to the neutrino telescope. On the seabed specially-developed DC/DC converters will reduce the transmission voltage to 400 V for distribution to the detection units.
The sea-floor network will consist of several junction boxes linked by electro-optical cables to the telescope detection units and satellite ocean sciences nodes. The final design of the network is still under development and will incorporate extensive redundancy to mitigate single point failures.
The design requirements for an ocean observatory site-to-shore cable are compatible with the standard capabilities of telecommunications cables, for which a wide range of industry-approved standard, connection boxes, couplings and penetrators exist, which can be adapted to interface with scientific equipment.
Underwater connection systems technologies, available from telecommunication and oil and gas market, including deep-sea wet-mateable optical, electro-optical and hybrid electro-optic connectors, have been adapted and developed to fulfil the project requirements.
The installation and maintenance operations of such detector are difficult and expensive. In the design of the system special attention is being paid to techniques for maximizing reliability and minimizing underwater operations. All components must survive both the mechanical rigours of installation (torsion, tension due to self-weight and ship movement) and must have high reliability and long lifetime under the extreme seabed conditions (high ambient pressure of around 300 bar, aggressive and corrosive environment, lateral and torsional forces due to deep sea currents etc.).

The various technical aspects of this unusual power supply system are discussed.

Parallel session A1 - ASICs / 85

Advanced Pixel Architectures for Scientific Image Sensors

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We will present recent developments from two projects targeting advanced pixel architectures for scientific applications. Results will be reported from test structures demonstrating variants on a 4T pixel architecture. The variants include differences in pixel and diode size, the in-pixel source follower transistor size and the capacitance of the readout node to optimise for low noise and high dynamic range. Results will also be reported from TPAC, a complex pixel architecture, which has been manufactured with a special deep P-well process and on a high resistivity substrate for enhanced charge collection performance.

Summary:

The scientific community often requires advanced sensors which are able to detect small amounts of charge. The requirements can include high sensitivity, low noise, high charge collection efficiency and a tolerance to radiation. To achieve these requirements, we are developing advanced pixel architectures, two of which are presented in this paper: 4 transistor (4T) pixels and complex pixels with full in-pixel CMOS circuitry. In both cases, we are also exploring high resistivity substrates to improve the charge collection efficiency.
In a standard substrate material, charge arising from an incident photon/particle moves by diffusion, and is collected only when it reaches the depletion region around the collecting diode (typically 1-2μm). High resistivity substrates can provide full depletion of the sensing layer, and the extended electric field improves charge collection time and efficiency. Alongside this, a deep P-well implant, developed by us in conjunction with a leading CMOS image sensor foundry, allows advanced circuitry to be implemented inside pixels without a detrimental effect to the charge collection.
The FORTIS (4T Test Image Sensor) project is dedicated to developing test sensors containing a 4T pixel fabricated in a specialised 0.18μm CMOS image sensor technology. The sensors contain thirteen different pixel variants on a 15μm pitch, including differences in the capacitance of the readout node to increase the conversion gain, variations in pixel pitch up to 45μm together with increased diode sizes to improve the charge collection efficiency, and variations in in-pixel source follower transistor size to decrease the noise distribution. The project also investigates the architecture further with the addition of a high resistivity substrate and the deep P-well layer to improve the charge collection efficiency. Two prototypes have been fabricated and results from the first one demonstrate a low noise value of 5.8e- and a conversion gain of 60μV/e- as measured at the sensor output. The second prototype which aims to improve these values further is currently undergoing testing, and the results will be available for the Workshop.
FORTIS sensors are currently undergoing testing for radiation hardness by irradiating with x-rays. The results will give us an insight into how tolerant the 4T pixel architecture is to ionising radiation, and may suggest where the radiation damage occurs to improve future designs.
The TPAC (Tera-Pixel-Active-Calorimeter) sensor was designed to demonstrate digital calorimetry for a silicon tungsten ECAL at the ILC. This device has now been manufactured with a uniform pixel array on standard and high resistivity substrates. The charge collection performance of pixel test structures is evaluated using a pulsed IR laser to demonstrate the improvement achieved by the deep P-well implant and high resistivity substrates. The status of the TPAC project, including latest results on the sensor performance, will be reported.
The results from both sensors are an exciting addition to the field of scientific image sensor development. The architectures and processing variations explored are applicable to a wide range of other applications where low noise readout and high sensitivity to small amounts of charge is required.

Parallel session A1 - ASICs / 86

Performance of the ABCN-25 readout chip for ATLAS Inner Detector Upgrade

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We present the test results of the ABCN-25 front end chip implemented in CMOS 0.25um technology and optimized for the short, 2.5cm, silicon strips intended to be used in the upgrade of the ATLAS Inner Detector. We obtain the full functionality of the readout part, the expected performance of the analogue front-end and the operation of the power control circuits. The performance is evaluated in view of the minimization of the power consumption, as the upgrade detector may contain up to 70 millions channels. System tests with different power distribution schemes proposed for the future tracker detectors are possible with this chip. The ABCN-25 ASIC is now serving as the prototype readout chip in the developments of the modules and staves for the upgrade of the ATLAS Inner Detector.

Summary:

An important component of the development program of silicon strips tracking system for the upgrade of the ATLAS experiment at the S-LHC is the ABCN-25 front-end readout chip. The ABCN-25 chip is designed for binary readout of silicon strip detectors. The design follows the architecture of the ABCD3T design implemented in BiCMOS DMILL technology and used in present ATLAS SCT detector. The primary goal of the ABCN-25 chip is to provide a test vehicle for the detector module development program and at the same time optimization of the front-end power consumption, for short strips of 2.5cm, with an ENC noise below 800 electrons. The other target is the development of a full digital readout chain, with 6.2us trigger latency, zero suppression, and a serial readout protocol compatible with the actual readout systems but able to run at higher speed (80Mb/s). The chip incorporates two current shunt devices, to evaluate the serial power distribution, and a voltage regulator for the analogue frontend, compatible with both the serial power and the DC-DC power systems.

The ABCN-25 chips have been fabricated with the IBM CMOS6 technology and full functionality has been demonstrated. The performance of the chip has been measured both for the analogue and digital functions by using a dedicated “one-chip” test board. The performance of the front-end circuit optimized for short strips are measured for different bias conditions and load capacitances. Noise measurements on preliminary hybrid boards with 20 ABCN-25 connected to a silicon strip detector will be shown for comparison. For the nominal power consumption of 0.7mW in the front-end, the measured ENC for 2.5pF detector capacitance is below 800e-. Time walk and linearity are also measured to compare the performance with numbers expected from simulation.
The functionality of the digital part of ABCN-25 has been fully verified. The daisy-chain readout of up to 10 chips at the speed of 80Mb/s has been proven. As the power consumption of the digital part is becoming dominant, the power consumptions of the different functional blocks of the chips (namely the pipeline, the readout system and the command decoder) are measured and discussed. The average digital current of 130mA at 2.5V is around 30% higher than the initial estimation. The excess current is partially due to the final optimization of the digital block design, as the final design tool optimizers are efficient in favoring the timing performance, but at the cost of additional clock buffers. The estimation of the power consumption with the ABCN-25 architecture but with a 130nm technology, and the possibilities of power reduction by design, will be discussed.
One of the two on-chip shunt circuits is made of a large current shunt device. The control with feedback of this device is through a filtered input to its gate. The second on-chip shunt circuit is stand-alone on chip and contains a novel control circuit, which ensures uniform distribution of the shunt current in many shunt regulators (up to 20) connected in parallel on the module as required for the serial powering system. A dedicated “4-chips” test board for the evaluation of these circuits has been made and test results with the two shunt circuits will be shown. The potential limitations of these devices in the foreseen implementation of 20 ABCN-25 chips powered in parallel on one hybrid board will be discussed.

POSTERS SESSION / 87

A new paradigm using GPUs for fast triggering and pattern matching at the CERN experiment NA62

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We describe a pilot project for the use of GPUs in an online triggering application at the CERN NA62 experiment, and the results of the first field tests together with a prototype data acquisition system.

Summary:

Two major trends can be identified in the development of trigger and DAQ systems for particle-physics experiments: the massive use of general-purpose commodity systems such as commercial PC farms for data acquisition, and the reduction of trigger levels implemented in hardware, towards a pure software selection system (”triggerless”).

The NA62 experiment at the CERN SPS aims at measuring an ultra-rare decay of the charged kaon; the signal has to be extracted from a huge background which is ten orders of magnitude more frequent.
With an input particle rate of 10 MHz, some tens of thousands detector channels and the requirement of avoiding zero suppression as much as possible, triggerless readout into PCs is not affordable.

An innovative approach aims at exploiting the parallel computing power of commercial GPUs to perform fast computations in software in the early trigger stages.
General-purpose computing on GPUs is emerging as a new paradigm in several fields of science, although so far applications have been tailored to the specific strengths of such devices, exploiting parallelization and avoiding real-time applications.
With the steady reduction of GPU latencies, and the increase in link and memory throughputs, the use of such devices for real-time applications in high-energy physics data acquisition and trigger systems is becoming ripe.

A pilot project within NA62 aims at integrating GPUs into the central L0 trigger processor, and also to use them as a fast online processors for computing trigger primitives.
Several TDC-equipped sub-detectors with sub-nanosecond time resolution will participate to the first-level NA62 trigger (L0), fully integrated with the data-acquisition system, to reduce the readout rate of all sub-detectors to 1 MHz, using multiplicity information asynchronously computed over time windows of a few ns, both for positive sub-detectors and for vetos.
The online use of GPUs would allow the computation of more complex trigger primitives already at this first trigger level.
Cheap commercial links can be used to collect trigger primitives, and the task of the dedicated central processor is to perform time matching of those, generate the trigger signal and re-align it in time for synchronous distribution.

We describe the architecture of the proposed system and present the performances achieved in tests on a real detector data acquisition system, to perform online recognition of rings from a RICH detector with sub-nanosecond time resolution.
The challenges and the prospects of this promising approach are discussed.

Parallel session B1 - Systems, Installation and Commissioning / 89

Deep-sea data transfer at the KM3NeT neutrino telescope

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KM3NeT is a future cubic kilometre-scale neutrino telescope for the deep Mediterranean. Several hundred vertical detection lines, each containing up to 100 optical modules with photomultipliers will be anchored to a sea floor power and data transport network. Data acquisition will minimize offshore electronics, reducing difficult and expensive maintenance operations. No off-shore triggering or filtering combining signals from multiple optical modules is foreseen; all signals passing internal criteria (e.g. charge threshold) will be uploaded via a fibreoptic telecommunications cable at an overall data rate of~ 100Gb/s. Various options for front-end digitization and data transport, including colour multiplexing, are discussed

Summary:

Summary: for presentation in the Optoelectronics and Links session

The KM3NeT data acquisition and transit system will collect analogue signals from photomultipliers (PMTs) contained in optical modules (OMs - based on pressure resistant glass spheres) arranged on several hundred tethered detection lines rising hundreds of metres from the seabed (2500 - 4000m depth) and tensioned by submerged buoys. The PMTs are sensitive not only to Cherenkov light from muon tracks generated in neutrino interactions, but also to high levels of optical background from bioluminescence and decays of radioactive potassium 40 present in sea salt.

While local coincidence triggering between nearby photomultipliers could be used to reduce these backgrounds, the central strategic approach is to maximize reliability in the difficult-to-maintain deep-sea hardware by keeping the electronics to a minimum. No off-shore triggering or filtering combining signals from multiple OMs is foreseen; all signals passing certain OM-internal criteria (e.g. charge threshold) will be uploaded to shore. An total effective photocathode area of around 50m2 will generate an overall data rate (signal + background) of~ 100Gb/s, based on 8 bytes (including timestamp) per recorded photon. This data rate to shore can be accommodated on a small number of optical fibres within a single, standard fibreoptic deep-sea telecommunications cable using either coarse or dense wavelength division multiplexing (CWDM or DWDM) transfer protocols.

The long distance from the deep-sea site to shore (30-100 km) forces the use of single-mode optical fibres. The conversion of the electrical signals to optical signals can be implemented at different locations along the detection lines, or at other points in the local seabed network. One possible solution is to convert the electrical signals close to the PMTs, making each OM an end-node in the fibreoptic network. In this scheme, wavelength multiplexing would be used to limit the number of descending fibres in each detection line: an all optical star network would be constructed based on passive optical multiplexers. An alternative solution could be based on a network in which the star consists of an active switch array with connections to the OMs or groups of OMs implemented as a copper links running part-way or all the way down the detection line to the sea bed.

The copper-to-fibre transition point is determined not only from considerations of length/bandwidth capabilities for the two media but also from the relative reliability of the deep-sea mateable connectors that are required for remotely-operated submarine interconnection of the bases of the detection lines to the junction boxes that will relay data onto the main site-to-shore fibreoptic telecommunications cable. Such deep-sea connectors have been developed for the oil industry and military applications and can be

mated in seawater at ambient pressures of more than 400 bar. They exist in electrical, optical or hybrid (electro-optic) configurations. Experience from the ANTARES neutrino telescope has shown hybrid electro-optic deep-sea mateable connectors to have an unfavourable reliability/cost quotient among sea-bed infrastructure components. While the technology of deep-sea mateable connectors continues to evolve rapidly, their relative cost and reliability in electrical, optical or hybrid configurations may determine whether the copper-to-fibre backbone transition occurs near the OMs, at the bases of the detection lines or within the junction boxes attached to the site-to-shore cable.

The sea-bed data network which connects the detection lines to the site-to-shore cable should allow for a progressive enlargement of the apparatus through successive deployments of detection lines (implying the passive acceptance of extra added colours), while maintaining data path redundancy at all stages of the telescope evolution. It is probable the detection lines will connect to a series of satellite junction boxes in a radial (star) configuration, while these junction boxes will themselves be circumferentially interconnected in a ring allowing for redundant data flow and powering pathways. The use of standard deep sea telecommunications cable branching and junction box node technology is under investigation. Straightforward deployment from cable ships carrying standard cable repair and handling plant will also be a major cost motivator in the configuration of the sea floor layout of the future KM3NeT neutrino telescope.

Parallel Session A5 - ASICS / 90

PARISROC, a photomultiplier array integrated readout chip

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PARISROC is a complete read out chip, in AMS SiGe 0.35µm technology [1],for photomultipliers array. It allows triggerless acquisition for next generation neutrino experiments and it belongs to an R&D program funded by French national agency for research (ANR) and called PMm2:“Innovative electronics for photodetectors array used in High Energy Physics and Astroparticles” [2] (ref.ANR-06-BLAN-0186).
The ASIC integrates 16 independent channels with variable gain and provides charge and time measurement by a 12-bit ADC and a 24-bits Counter.

Summary:

PARISROC is a front-end electronics ASIC designed for the next generation of neutrino experiments. These detectors will take place in megaton size water tanks and will require very large surface of photo-detection [3].
PMm2 project proposes to segment the very large surface of photo-detection in macro pixels made of 16 photomultiplier tubes connected to an autonomous front-end electronics. The ASIC must only send out the relevant data by network to the central data storage. This data management reduces considerably the cost of these detectors.
The PARISROC chip integrates 16 channels totally independents.
Each analogue channel is made of a low noise preamplifier with variable and adjustable gain. The variable gain is common for all channels. The gain is also tuneable channel by channel to adjust the input detector’s gain (on 8 bit).
The preamplifier is followed by a slow channel for the charge measurement in parallel with a fast channel for the trigger output.
The slow channel is made by a variable (50-200ns) slow shaper followed by an analogue memory with depth of 2 to provide a linear charge measurement up to 50pC; this charge is converted by a 12 bit Wilkinson ADC.
The fast channel is composed of a fast shaper (15ns) followed by 2 low offset discriminators to auto-trig

down to 10fC. The thresholds are loaded by 2 internal 10-bit DACs common for the 16 channels. The 2 discriminator outputs are multiplexed to provide only 16 trigger outputs. Each output trigger is latched to hold the state of the response until the end of clock cycle. It is also delayed to open the hold switch on the maximum of the slow shaper.
On each channel, a fine time measurement is made by an analogue memory with depth of 2 which sample a 12 bit ramp, common for all channels, as the same time of the charge. This time is then converted by a 12 bit Wilkinson ADC.
The two ADCs discriminators have a common ramp, of 8, 10 or 12 bits, as threshold to convert the charge and the fine time.
A bandgap bloc provides all voltage references.
A digital part [4] manages all the acquisition, the conversion and the readout and provides by a 24-bit counter the coarse time measurement or timestamp.
Design, simulation results and measurements of the first prototype will be presented.

References:
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[3] B. Genolini et Al., PMm2: large photomultipliers and innovative electronics for next generation neutrino experiments, NDIP'08 conference.
[4] F. Dulucq et Al., Digital part of PARISROC: a photomultiplier array readout chip, TWEPP08 conference.

POSTERS SESSION / 91

A self triggered amplifier/digitizer chip for CBM

Authors: Ivan Peric[1]; Peter Fischer[1]; Tim Armbruster[1]

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The development of front-end electronics for the planned CBM experiment at FAIR/GSI is in full progress. For the charge readout of the various subdetectors a new self triggered amplification and digitalization chip is being designed and tested. The chip will have 32-64 channels each containing a low power/low noise preamplifier/shaper front-end, an 8-9 Bit ADC and a digital post-processing based on a simple FIR-filter. The ADC uses a pipeline architecture based on novel current-mode storage cells. An overview of the architecture and the targeted applications is given and the status of the project is presented.

Parallel Session B5 - Optoelectronics and Links / 92

STUDY OF RADIATION HARDNESS OF PIN AND VCSEL ARRAYS

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We study the radiation hardness of 850 nm PIN/VCSEL arrays for possible deployment in the detector optical readouts for the LHC luminosity upgrades. In 2008, we irradiated two devices from several vendors to the radiation doses expected for the ATLAS silicon trackers. This leads to the identification of the best arrays from two vendors for possible deployment in a new ATLAS pixel-detector for the first phase of the luminosity upgrade. In 2009, we will irradiate a large sample of these arrays, together with some new devices available, to verify the radiation hardness. We will present the results from the irradiations.

Summary:

Optical links deploying VCSELs and PINs are used for the data transmission in the major detectors at the Large Hadron Collider (LHC) at CERN (Geneva). The LHC will be upgraded in two phases, resulting in ten times higher luminosity. The detectors are expected to be exposed to a similar increase in radiation. In the past years, we have studied the radiation hardness of VCSEL and PIN from several vendors using 24 GeV/c protons at CERN up to a fluence of 2.6 x 10^15 p/cm^2. The GaAs VCSEL arrays were fabricated by four vendors, Optowell, Advanced Optical Components (two varieties, 5.0 and 10 Gb/s), and ULM Photonics (two varieties, 5 and 10 Gb/s). The GaAs PIN arrays were also fabricated by the same vendors but there was only one variety from each vendor. In addition, we also irradiated the GaAs (one variety) and silicon (two varieties) PIN devices from Hamamatsu. For the VCSEL arrays, we monitored the optical power as a function of dosage and observed significant decrease in the optical power with radiation. We periodically moved the devices out of the proton beam and passed high currents through the arrays for annealing. However, the time available for the annealing was limited during the irradiation period and the devices were returned to the laboratory for an extended annealing. Overall, we found that the AOC arrays were the most radiation hard. For the PIN diodes, we monitored the responsivity as a function of dosage and observed that the responsivity decreased with radiation. In general, the silicon devices had lower data bandwidth but were more radiation hard than the GaAs devices as expected. The degradation in the responsivities was smallest in the Hamamatsu devices, followed by the Optowell arrays. The above study was based on a small sample (typically two devices for each variety). We plan to repeat the irradiation this August with a much larger sample (20 devices for each variety) for possible application in the new pixel detector for the first phase of the LHC upgrades. The candidate devices are AOC (10 Gb/s) VCSEL array and Optowell PIN array. We will not study the Hamamatsu devices because we cannot acquire bare arrays for custom packaging. In addition, we will irradiate new devices available. The results from the studies will be presented.

Parallel session A2 - ASICs / 93

DIRAC v2: a DIgital Readout Asic for hadronic Calorimeter

Author: Renaud Gaglione[1]

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This mixed-signal circuit is a 64 channels readout R&D ASIC for Micro-Pattern Gaseous Detectors (Micromegas, Gas Electron Multiplier) or Resistive Plate Chambers. These detectors are foreseen as the active part of a digital hadronic calorimeter for a high energy physics experiment at the International Linear Collider. Physics requirements lead to a highly granular hadronic calorimeter with up to fifty millions channels with probably only hit information (digital calorimeter).
The first version of this chip has been tested in beam last year on a detector, thus proving the feasibility of Micromegas with embedded digital readout.

Summary:

This mixed-signal circuit is a 64 channels readout R&D ASIC for Micro-Pattern Gaseous Detectors (Micromegas, Gas Electron Multiplier) or Resistive Plate Chambers. These detectors are foreseen as the active part of a digital hadronic calorimeter for a high energy physics experiment at the International Linear Collider. Physics requirements lead to a highly granular hadronic calorimeter with up to fifty millions channels with probably only hit information (digital calorimeter).
Each channel of the chip is made of a 4 gains charge preamplifier, a DC-servo loop, 3 switched comparators and a digital memory, thus providing additional energy information for a hit. For detector characterization, a multiplexed analog readout has been implemented.
Configuration and readout are fully digital, indeed six 8-bit DACs are embedded to set comparators thresholds. Power-down circuitry has been included, decreasing the power consumption to 10 µW per channel. To achieve a low cost electronics, a cheap full CMOS 0.35 µm foundry process has been chosen and the floorplan has been designed to reduce Printed Circuit Board costs.
The SPS beam tests of the DIRAC first version embedded in a bulk Micromegas will be presented. The second version has just been received and preliminary results will be detailed. Large area detectors equipped with these chips are planned to be put in the PS beam this year.

Parallel session A4 - Trigger / 94

Design Considerations for an Upgraded Track-Finding Processor in the Level-1 Endcap Muon Trigger of CMS for SLHC Operations

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The conceptual design for a Level-1 muon track-finder trigger for the CMS endcap muon system is proposed that can accommodate the increased particle occupancy and system constraints of the proposed SLHC accelerator upgrade and the CMS detector upgrades. A brief review of the architecture of the current track-finder for LHC trigger operation is given, with potential bottlenecks indicated for SLHC operation. The upgraded track-finding processors described here would receive as many as two track segments detected from every cathode strip chamber comprising the endcap muon system, up to a total of 18 per 60° azimuthal sector. This would dramatically improve the efficiency of the track reconstruction in a high occupancy environment over the current design, since some of the track segments are filtered out in order to reduce transmission bandwidth and track processing logic. However, such an improvement would require significantly higher bandwidth and logic resources over the current design. We propose to use fastest available serial links, running asynchronously to the machine clock. Another enhancement critical for the overall Level-1 trigger capability for physics studies in phase 2 of the SLHC is to include the inner silicon tracking systems into the design of the Level-1 trigger. This requires matching muons identified in the endcap muon system and matching them to hits in the inner tracking system and refining the momentum measurement to improved precision for better rate reduction capabilities. Some preliminary ideas on the precision of information available from the endcap track-finder trigger will be presented along with possible algorithms for the matching.

Parallel Session A3 - Trigger / 95

Framework for Testing and Operation of the ATLAS Level-1 MUCTPI and CTP

Author: Ralf Spiwoks[1]

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The ATLAS Level-1 Muon to Central Trigger Processor Interface (MUCTPI) receives information on muon candidates from the muon trigger sectors and sends multiplicity values to the Central Trigger Processor (CTP). The CTP receives the multiplicity values from the MUCTPI and combines them with information from the calorimeter trigger and other triggers of the experiment and makes the final Level-1 decision. The MUCTPI and CTP are housed in two 9U VME64x crates and are made of eight different types of custom designed modules.
This paper will present the framework which is used for debugging, commissioning and operation of all modules of the MUCTPI and CTP. Testing of the modules has been considered right from design. Most types of modules contain diagnostic memories at the input of the module which can be used to capture incoming data or to inject data into the module. Testing of the modules can be achieved by

capturing data at input of a down-stream module, by reading out data from a monitoring buffer at output, or by reading out monitoring counters.
A layered software framework using C++ has been developed for configuring and controlling all modules and for testing them independently or grouped into complete sub-systems. The lowest level uses the ATLAS VME library and driver. At the next highest level, a compiler translates a description of the VME registers from XML to C++ code. This code together with existing code for some components, e.g. HPTDC, DELAY25, and JTAG, is combined to the low-level library of the module. A menu program provides access to all methods of the module low-level library. Generators create data for the test memories. Simulators calculate the expected results. Generators, simulators and the low-level library are combined to a suite of test programs which cover the full functionality of the MUCTPI and CTP. The low-level library is also used by the run control and monitoring programs which integrates the sub-systems into the ATLAS experiment control and monitoring framework.

Parallel session B1 - Systems, Installation and Commissioning / 96

Commissioning of the DT electronics under magnetic field.

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After several months of completing the installation and commissioning of the CMS (Compact Muon Solenoid) DT (Drift Tube) electronics, the system has finally been operated under magnetic field during the so-called CRAFT (Cosmic Run at Four Tesla) exercise. Over 4 weeks, the full detector has been running continuosly under magnetic field and achieved to acquire up to 300 million cosmic muons. The performance of the trigger and data acquisition systems during this period has been very satisfactory and the main results concerning stability and reliability of the detector are presented and discussed.

Summary:

A key point of CMS (Compact Muon Solenoid) is its ability to trigger on and reconstruct muon tracks at high luminosities. This task is performed by various CMS subdetectors, among them, the DT (Drift Tube) chambers.
The 250 DT chambers are hosted in the five wheels of the CMS barrel, with a total of 172,200 drift cells. A DT chamber is made of three (or two in the outer layer) superlayers, each made by four layers of rectangular drift cells staggered by half a cell, which provide track measurement in the magnetic bending plane (r,⊠) and in the Z position along the beam line.
DT read-out electronics is designed to perform time digitization of the signals generated by charged particle tracks and further data merging to achieve a read-out of the full detector at a Level-1 trigger rate of 100 kHz.
The purpose of the DT trigger system is to provide muon identification and precise momentum measurement, as well as bunch crossing identification. It provides an independent Level-1 muon trigger to the experiment, selecting the four best muon candidates on each event.
From May 2008 DT has participated in several long periods of data-taking with the 100% of the detector operational, such as CRUZET (Cosmics Run at Zero Tesla) and CRAFT (Cosmic Run At Four Tesla). Participation in these Global Runs has proven the DT system to be well integrated inside the CMS framework, with good reliability and stability. Operation during more than one year showed that failure rates are very low.
About 320 and 370 million events of cosmic muons were collected at CRUZET and CRAFT respectively and no significant effect on the performance of the electronics was observed due to the magnetic field.
Continuos operation over more than 3 weeks showed good stability of the power distribution systems, low voltage and high voltage, as well as of the reliability of the trigger and read-out links. Some issues with the cooling system are now being solved.
Furthermore, running periods at simulated high rate have shown no problems on the performance on

the system when operated at full speed.
The efficiency to reconstruct high quality local track segments has been measured to be of the order of 99% in all chambers. Also, very good stability in the calibration constants has been found.
Moreover, fine tunning of the trigger system timing, which was optimized for cosmic tagging, shows a very good synchronization with the rest of the subsytems.
Noise levels were monitored and the number of death and noisy cells is very low and it is stable in time. Sensitivity to some sporadic noise, usually related with activities in the cavern, is being studied at present.
Experience during these exercises has allowed improving significantly control and monitoring systems, which at present allow configuring all parts in an easy and flexible way and obtaining comprehensible synthetic information of the complete status of the detector.
Summarizing, the behaviour of the system is very satisfactory, being ready for operation at LHC running.

Parallel Session B4 - Power, Grounding and Shielding / 97

ASIC buck converter prototypes for LHC upgrades

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In the context of a new power distribution scheme for SHLC tracker based on switching DC/DC converter, we are developing a custom converter able to work in the high radiation and high magnetic field environment of the experiments. Two new ASIC prototypes, in two different technologies, have been designed and manufactured. Design techniques, functional and radiation tests of the prototypes will be discussed.

Summary:

In view of an increase of the current required by the front-end (FE) circuits for SLHC trackers, a new power distribution scheme based on DC/DC converters has been proposed at TWEPP 2008. A first converter ASIC developed in the 0.35µm AMIS high voltage technology (HVT) has been presented as well. We have since completed the design of two more mature converters, one in the same AMIS process and the other in the 0.25µm IHP HVT.
The AMIS prototype is a fully integrated buck converter with embedded voltage mode control loop (also with passive components). It includes two lateral high voltage NMOS with Rdson=20mΩ and 40mΩ (low and high side respectively), an oscillator with programmable frequency up to 3MHz, a voltage reference and a soft-start procedure to avoid large inrush currents at the start-up of the converter. The delay time between the gate signals is by default 50ns and it can be changed with external resistors. The ASIC is mounted in a 7x7mm QFN package, allowing the design of a compact PCB.
After the delivery of this chip, expected for mid-May 2009, tests will be carried out and results will be presented at TWEPP.
While the ASICs engineered in the AMIS process were developed for understanding the design issues of a fully integrated DC/DC converter, a market survey for other available commercial HVTs was held to find one that can be tolerant to radiation, both for total ionizing dose and displacement damage. The 0.25µm IHP technology showed the best radiation tolerance and also electrical performance, therefore we decided to move the design of the converter in this HVT.
In view of the integration of the converter in the system, small converter size (chip and PCB dimensions and number of external components) and high efficiency (above 80%) are specifically addressed in this design. For this purpose a study of different converter topologies and working modes was carried out, showing that the best compromise is a buck converter that works at a frequency of few MHz and in a conduction mode called quasi square wave (QSW). As it will be explained in details in the final paper,

this mode ensures a reduction of the switching losses. For the same reason, the internal control loop has been equipped with an adaptive logic circuit, developed on purpose to make the delay between the power MOS gate signals no longer fixed (but always shorter than a pre-selected value).
The ASIC developed in the IHP technology has been included in a shuttle MPW run in May 2009. It embeds two power transistors (a lateral PMOS for the high side with Rdson=25mΩ and a lateral NMOS with Rdson=10mΩ for the low side), the voltage control loop and an oscillator with nominal frequency of 2 MHz that can be changed with external resistors. This chip will also be bonded in a 7x7mm QFN package.
The delivery date of this ASIC is foreseen for July 2009 and test results will be presented at TWEPP together with a detailed description of the chip design.

Parallel Session A3 - Trigger / **98**

Precise Timing Adjustment for the ATLAS Level1 Endcap Muon Trigger System

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The ATLAS level1 endcap muon trigger system consists of about 4000 Thin Gap Chambers (TGC) with 320,000 input electronics channels in order to find level1 trigger candidates for muons in both endcap regions. We had already adjusted channel-to-channel timing difference in overall TGC system with 1.2ns level, and found its consistency with the observation of beam halo events in the first proton circulation of LHC in September 2008. After that we have found some more correction factors to be incorporated with and eventually achieved timing adjustment in 0.9ns precision. In this presentation we also discuss an effective strategy for a parameter that can be adjusted using colliding beams.

Summary:

For supplying the level1 endcap muon signals, we have installed about 4000 Thin Gap Chambers (TGC) to cover full region of both endcaps of the ATLAS detctor (1.05 < |eta| < 2.4). TGC signal processing system is divided into five stages as follows;
1. TGC and Amplifier, Discriminator and Shaper (ASD) block,
2. Patch Panel (PP) (Bunch Crossing Identification, sub-nano sec. fine delay),
3. Slave Board (Level1 buffer, derandomizer, Low pT coincidence matrix, and readout logic),
4. High pT (HpT) coincidence block, and
5. Sector Logic (wire (r) and strip (phi) coincidence logic).

The stages No.2 and No.3 are installed in the same board (PSB). The HpT board is installed in the vicinity of PSB (10 or 15m cables are used between PSB and HpT). These are all mounted just behind TGC while the stage No.5 (SL) is installed in the counting hut (USA15). The on-detector (PSB-HpT) and off-detector (SL) parts are connected with optical fibers of length 90m in average.
Since the most careful and precise timing adjustment must be made at the input of the PP stage, we have installed several facilities for this purpose in PP. We have sub-nano second delay circuit in PP to adjust timing difference of hit signals caused by differences of time of flight (TOF) of particles from the interaction point to a particular region of TGC and length of cables between ASD and PP. Another delay circuit with the same precision has been implemented to adjust BCID gate timing to absorb inherent timing fluctuation of signals generated in chamber. PP has further facility to produce test pulses (TP), which are triggered by TTCrx externally. Generation timing of TP after the trigger is adjustable with also the same precision as the delay circuits mentioned above. Since TP can be transported with the same cable connected between ASD and PP reversely into ASD, we can use this TP to simulate a hit signal made by a muon if we adjust the same timing as TOF expected for region covered by a particular ASD.
At this stage we had needed three parameters to estimate the delay timing for particular input channel, which are TOF, the cable length between ASD and PP and pulse mobile velocity in the cable. We had adjusted timing using these parameters and got reasonable results with beam halo events in the first beam circulation done in September 2008. Since then we carefully looked for other correction factors hidden in the system. We have then found the signal attenuation effect as the fourth factor for the signal delay, and also the existence of cables whose cable lengths are different from the nominal value supplied by

the company. We have found this fact by measuring the delay-timing scan for all signal cables of about 10,000 using TP. By implementing these effect and correction, eventually we could achieve the timing adjustment of channel-to-channel within 0.9ns level in RMS.
We have one timing adjustment parameter left unadjusted. That is the phase difference between bunch crossing signal supplied by LHC and the clock pulse used actually in TGC system. This phase difference can be adjusted only with colliding beams. We have fixed a strategy to how to adjust this difference in 10 min. if overall TGC level1 trigger rate is 500Hz. We would like to discuss also this strategy in the presentation.

Parallel Session A3 - Trigger / **100**

PERFORMANCE OF THE CMS REGIONAL CALORIMETER TRIGGER

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The CMS Regional Calorimeter Trigger (RCT) receives 8 bit energies and a data quality bit from the HCAL and ECAL Trigger Primitive Generators (TPGs) and sends it to the Global Calorimeter Trigger (GCT) after processing. The RCT hardware consists of 1 clock distribution crate and 18 double-sided crates containing custom boards, ASICs, and backplanes. The electronics for the RCT have been fully installed since 2007.

The RCT has been fully integrated into the CMS Level-1 Trigger chain. Regular runs, triggering on cosmic rays, prepare the CMS detector for the restart of the LHC. During this running, the RCT control is handled centrally by CMS Run Control and Monitor System communicating with the Trigger Supervisor. Online Data Quality Monitoring (DQM) evaluates the performance of the RCT during these runs. Offline DQM allows more detailed studies, including trigger efficiencies. These and other results from cosmic-ray data taking with the RCT will be presented.

Summary:

The Regional Calorimeter Trigger (RCT) has been installed in the Compact Muon Solenoid (CMS) cavern since 2007. The custom hardware of the RCT consists of one 6U clock distribution crate and eighteen 9U double-sided crates containing a backplane and boards with custom ASICs. Including spares, almost 1800 boards of 9 different types have been produced. Included are a Clock Input Card, two Clock Fan-out Cards, backplane, Clock and Control Card, Receiver Mezzanine Card, Receiver Card, Electron Identification Card, and Jet/Summary Card. This system receives 8000 calorimeter trigger tower transverse energies (ETs) and characterization bits from the Electromagnetic and Hadronic Calorimeter Trigger Primitive Generators (TPGs) via 4 GBaud copper links. These individual tower ETs and characterization bits are used to find electron candidates and tower ETs are summed over 4x4 regions. They are forwarded to the Global Calorimeter Trigger (GCT) via their source cards for jet finding, missing ET, total ET, and further sorting. The RCT has been fully integrated into the CMS Level-1 Trigger chain using patterns generated in the hardware and by joining in data taking triggering on cosmic-ray muons.

Generating patterns in the RCT and then capturing them in the GCT source cards test the RCT to GCT connection. Both TPG subsystems are also able to generate patterns. These test the TPG serial links to the RCT as well as connections downstream. TPG Patterns are also captured at the GCT. The Global Trigger is included for control and synchronization of all the subsystems involved. These tests are used to verify the connections are sound, especially after a hardware intervention.

The focus of the past year has been on running the CMS detector, triggering on cosmic rays, to prepare for the restart of the LHC. The RCT, as part of the fully integrated calorimeter trigger has actively participated. During this running, the RCT control is handled centrally by CMS Run Control and Mon-

itor System communicating with the Trigger Supervisor. This includes configuration of the RCT and monitoring of these configuration parameters and hardware status bits, including errors.

Online Data Quality Monitoring (DQM) evaluates the performance of the RCT hardware during these runs. In real time, data from the run is collected and compared to reference plots, using the software Trigger Emulator to compare algorithms implemented in the hardware with expected performance. Shift crews and experts monitor the histograms and can rapidly find problems that may be affecting the current run. Then, as soon as runs are completed, Offline DQM is run and the results analyzed. Offline DQM allows for the full event sample to be studied for detailed studies, including as channel-by-channel comparisons and efficiency curves.

In addition, further performance studies are under way to determine overall trigger efficiencies for the various calorimeter trigger types (jet and e/gamma, for example) during the cosmic-ray data taking – details of how these are measured and the overall performance of the RCT during cosmic-ray data taking will be presented.

POSTERS SESSION / 102

A 40 MHz trigger-free readout architecture for the LHCb experiment

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LHCb is considering an upgrade towards a full 40 MHz readout. In this paper we investigate possibilities for a new Timing and Fast Control (TFC) system based on completely new technologies, and the consequences for the readout electronics. We define the requirements and propose an architecture allowing partitioning, complete readout control and event management. The backbone is based on bidirectional high-speed optical links using the latest FPGA transceivers. For the Front-End Electronics we advocate exploiting the bidirectional capability of the CERN GigaBit Transceiver to make the Readout Boards the TFC and the Control System interface to the Front-End.

Summary:

The LHCb experiment at CEN is considering an upgrade towards a trigger-free 40 MHz complete event readout to a farm performing the event selection with only a high-level software trigger with access to all detector information. This allows operating LHCb at ten times the current design luminosity and improving the trigger efficiencies in order to collect more than ten times the statistics foreseen in the first phase. In practice it requires replacing the entire readout system. Optical links based on the CERN GigaBit Transceiver (GBT) are considered for the readout between the front-end electronics (FE) and a set of 400 Readout Boards. The Readout Boards will act as interfaces to the event-building 16 Terabit/s readout network based on IP-Over-InfiniBand. Exploiting the bidirectional capability of the CERN GBT, the Readout Boards also act as the FE interface for timing and synchronous control information, as well as the bridge for configuration and monitoring information on a subset of the optical links. The event filter farm is to be based on COTS multicore computers.
In this paper we present the architecture in consideration. In particular, we investigate new technologies and protocols to build a system for the distribution of timing, and synchronous and fast asynchronous control commands. This so called Timing and Fast Control (TFC) system sequences resets and calibrations, produces auto-triggers and performs rate control and central destination control for the events. It also manages the load balancing of the readout network and the event filter farm. The TFC system will be centred on a single FPGA-based multimaster allowing parallel stand-alone operation of any subset of sub-detectors. The TFC distribution network between the TFC master and the Readout Boards under investigation consists of a bidirectional optical network based on the high-speed transceivers embedded in the latest generation of FPGAs (ALTERA Stratix IV) with special measures to have full control of the phase of the transmitted clock and the latency of the transmitted information. Since data zero-suppression is performed at the detector front-ends, the readout is effectively asynchronous and will require that the synchronous control information carry event identifiers to allow realignment and synchronization checks.

For the detector FE we advocate exploiting the bidirectional capability of the CERN GBT development to also make the Readout Boards the relay for timing and synchronous control information, as well as the bridge for configuration and monitoring information on a subset of the optical links.
Recognizing the expanse of the LHCb upgrade, the new TFC architecture allows hybrid operation with the old and new readout electronics.
At the end we demonstrate the usefulness of a complete simulation framework and discuss the necessary R&D studies we are undertaking. We also underline the importance to take lead with the development of the TFC system in order to facilitate tests and assure conformity of the sub-detector electronics with the common specifications.

POSTERS SESSION / 103

The Prompt Trigger of the Silicon Pixel Detector for the ALICE Experiment

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The ALICE Silicon Pixel Detector (SPD) constitutes the two innermost layers of the ALICE experiment. It consists of 1200 pixel chips with a total of ~107 channels with a pixel size of 50x425 μm2. Each pixel chip transmits a Fast-Or signal upon registration of at least one pixel hit. These signals are extracted every 100 ns and processed by the Pixel Trigger (PIT) system. A signal is then sent within a latency of 800 ns to the Central Trigger Processor for the Level 0 trigger decision.
This paper describes the commissioning of the PIT, the tuning procedure of the SPD modules to obtain a good efficiency of the Fast-Or signal, and results of operations in cosmic and beam runs.

Summary:

The ALICE Silicon Pixel Detector (SPD) constitutes the two innermost layers of the ALICE experiment. It consists of 1200 pixel chips with a total of ~107 channels with a pixel size of 50x425 μm2.
Its output data stream includes 1200 Fast-Or signals provided by the pixel chips and generated by the on-chip Fast-Or circuitry. The Fast-Or signals are transmitted every 100 ns on 120 optical links and indicate the presence of at least one pixel hit in the matrix of each readout chip. The Pixel Trigger (PIT) system extracts these signals and processes them with up to 10 trigger algorithms in parallel. Algorithms based on event topology or hit multiplicity can be implemented as boolean logic functions inside FPGAs.
The PIT sends the processed signals to the Central Trigger Processor (CTP) where they contribute to the first level trigger decision (Level 0). The PIT trigger information will help to improve event selection in proton and heavy ions collisions as well as the background rejection.
According to the design requirements, the maximum latency of the PIT output signal from the particle collision to the transmission to the CTP has been proven to be within 800 ns.
This contribution describes the commissioning of the Pixel Trigger and the tuning of the 120 SPD modules (half-staves) in order to maximize the efficiency and minimize the readout noise of the Fast-Or trigger signal.
A procedure to find the optimum settings of the 4 Fast-Or internal 8-bits DACs of each pixel chip has been developed and tested in laboratory, and implemented into the experiment when the Pixel Trigger was installed in the cavern in April 2008. After an initial manual tuning, an automatic calibration procedure has been developed, with the goal to reduce by two orders of magnitude the time needed for the tuning of the 1200 pixel chips. To implement this automatic procedure, the SPD and Pixel Trigger Front End Device (FED) servers communicate to each other and exchange data through a Distributed Information Management (DIM) System. A DAC scan algorithm has been implemented inside the SPD FED Server and offline tools have been prepared to analyse the results.
The Pixel Trigger signal was successfully used by the ALICE experiment as a L0 trigger. A sizeable amount of cosmic data for alignment has been collected with several ALICE detectors being triggered by the SPD. In 6 months of operation nearly 100k events with 3 or 4 muon tracks in the pixel detector were collected.
In June 2008, during the beam injection tests, the SPD recorded in self-triggering mode the first events related to the beam activity in LHC. In September 2008, during the first circulating beams, the ALICE Inner Tracking System observed the first beam induced interactions: the trigger was provided by the

PIT and based on a multiplicity algorithm.

Parallel session A2 - ASICs / 104

HARDROC, Readout chip of the Digital Hadronic Calorimeter of ILC

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HARDROC (HAdronic Rpc Detector ReadOut Chip) is the very front end chip designed for the readout of the RPC or Micromegas foreseen for the Digital HAdronic CALorimeter (DHCAL) of the future International Linear Collider.
The very fine granularity of the ILC hadronic calorimeters (1cm2 pads) implies a huge number of electronics channels (400 000 /m3) which is a new feature of "imaging" calorimetry.
Moreover, for compactness, the chips must be embedded inside the detector making crucial the reduction of the power consumption to 10 µWatt per channel. This is achieved using power pulsing, made possible by the ILC bunch pattern (1 ms of acquisition data for 199 ms of dead time).
HARDROC readout is a semi-digital readout with two or three thresholds (2 or 3 bits readout respectively in hardroc1 and hardroc2) which allows both good tracking and coarse energy measurement, and also integrates on chip data storage.
The 64 channels of the 2nd prototype, HARDROC2, are made of:
• Fast low impedance preamplifier with a variable gain over 8 bits per channel
• A variable slow shaper (50-150ns) and Track and Hold to provide a multiplexed analog charge output up to 15pC.
• 3 variable gain fast shapers followed by 3 low offset discriminators to autotrig down to 10 fC up to 10pC. The thresholds are loaded by 3 internal 10 bit- DACs and the 3 discri outputs are sent to a 3 inputs to 2 outputs encoder
• A 128 deep digital memory to store the 2*64 encoded outputs of the 3 discriminators and bunch crossing identification coded over 24 bits counter.
• Power pulsing and integration of a POD (Power On Digital) module for the 5MHz and 40 Mhz clocks management during the readout, to reach 10µW/channel
The overall performance of HARDROC will be described with detailed measurements of all the characteristics. Hundreds of chips have indeed been produced and tested before being mounted on printed boards developed for the readout of large scale (1m2) RPC and Micromegas prototypes. These prototypes have been tested with cosmics and also in testbeam at CERN in 2008 and 2009 to evaluate the performance of different kinds of GRPCs and to validate the semi-digital electronics readout system in beam conditions.

Parallel Session B4 - Power, Grounding and Shielding / 105

Progress on DC-DC converters for SiTracker for SLHC

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Previous tests have shown that Enpirion EN5360, a 6 amp device is capable of taking sLHC radiation dosage but the input voltage is limited to a maximum of 5.5V. But from a systems point of view it is essential to have a factor of 10 in input/out voltage ratio in single stage i.e. maximum input voltage be >12 Volts.
The silicon foundry that made this device can now make 12 V FETS on the same 0.25 μm process with good irradiation results that are reported. Plug in power cards with x10 voltage ratio are being developed for testing the hybrids with ABCN chips, these have air coils but using commercial chips that may not be radiation hard but help in system noise and performance testing.

Summary:

Our goal has been to have DC-DC converters capable of delivering an output of 1.2 volts with load currents of several amperes. To our knowledge there was no IC process that was capable of running at 12 volts to give us a 10:1 voltage ratio with the SiTracker radiation hardness. In 2008, IHP Microelectronics successfully added 12 V FET transistor switches to their existing process, by the addition of 2 more mask layers.
We emphasize that the radiation damage limits the maximum input voltage because of the processing and oxide thickness. IHP has worked on this Silicon LDMOS process for 5 years or more. To the best of our knowledge there is no other foundry making 12 V devices with 0.25 μm process. At the moment there is no commercial device available with this process.

Plug in power cards with commercial converters devices are being developed by our group to test the Hybrids being developed by the ATLAS Si tracker upgrade group. These cards will use commercial devices that are not likely to be radiation hard. The current requirements for the 20 chip hybrids are now 4 amps and we are developing boards for the
1. Converter chips Maxim 8864 and IR3841
2. Spiral and spring/ solenoid coils

The above will be 4 separate pcbs. We need to fully power the new hybrids from this power cards to study both conduction and radiated noise.

We are continuing to irradiate new commercial device that in our view may tolerate high radiation levels.

Parallel Session A5 - ASICS / **106**

SuperNemo Absolute Time Stamper, a high resolution and large dynamic range TDC for SuperNemo experiment

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The SNATS chip is designed to provide both a high resolution of 70ps RMS and a large dynamic range of 53 bits.

The architecture is based on the association of 32 cell delay locked loops and of a 48-bit digital counter which are synchronized to a 160 MHz external clock.

A 16 channel prototype has been designed in AMS 0.35 μm CMOS technology and its main performances are a Differential Non Linearity of about 0.2 LSB and an Integral Non Linearity about 1.3 LSB.

The circuit uses 12.7 mm2 of silicon area and is packaged in a 100-pin ceramic CQFP.

Summary:

The aim of the NEMO collaboration is to investigate neutrinoless double-beta decay. This research is one of the principal topics in neutrino physics, which is a subfield of particle physics with cosmological and astrophysical implications.
Double-beta decay experiments can play a particularly interesting role in providing the answers to questions on the nature of the neutrino. Of paramount importance is the identification of the neutrino as a Dirac particle or Majorana particle.
For double-beta run of the SuperNEMO experiment, it has been decided to work without trigger module, with absolute time measurements.
To assume this requirement, a time stamp system is needed for the calorimeter front-end electronics.

So, the SNATS chip, described in this paper, has been designing to provide both a high resolution of 70ps RMS and a large dynamic range of 53 bits.
The architecture is based on the association of delay locked loop and digital counter which are synchronized by a 160 MHz external clock.
A prototype chip of 16 channels TDC was designed in AMS 0.35 µm CMOS technology.

The chip contains 8 DLL ‘s single ended (1 DLL for 2 channels) and a common counter. Each Delay Locked Loop has 32 delay elements giving a binning of 200 ps. To guarantee this binning independent of process and temperature variation, specific voltage controlled delay cell has been optimized. This cell is made of a current-starved inverter followed by a standard inverter.
Separate buffering of the outputs driving the channel buffers and the phase detector are required to maintain correct path delay matching and to minimize the effects of parasitic components.
The characteristic of the delay cells offers a low slope of 0.15ps/mV at typical frequency of 160 MHz which minimizes the jitter at the end of the DLL.
The memorization of the state of DLL’s is obtained by 2 cascaded D latch in order to reduce metastability.
Voltage controlled external tuning is optionally available to reduce individually the phase error of each DLL and to optimize the Differential Non Linearity.
A 48 bits GRAY counter filling a 780um x 100um area, is employed for coarse conversion and used to measure a time range of about 20 days. It permits limiting the digital noise by decreasing the power consumption of the counter and its respective output buffers. The counter is composed of 12 parts modulo 4 bits to reduce the complexity and to insure the gear until a frequency of 200MHz.
In order to avoid error junction due to the phase difference between the DLL and the counter, a synchronizer was implemented to reduce the area used by limiting the use of two counters synchronous to opposite phases of the reference clock. The principle of this synchroniser consists in generating a hit coarse delayed in function of the relative position of the hit arrival within the clock period. It always permits latching the state of the counter when its outputs are in relation with the DLL.

When a channel is hiting, data are available with 4 words of 16 bits and 100ns are necessary to read its. After the read out, each channel must be reset to accept new event.

Concerning the performances, it has been measuring a Differential Non Linearity of about 0.2 L

The static power dissipation is measured as about 380mW. The circuit uses 12.7 mm2 of silicon area and was packaged in a 100-pin ceramic CQFP.

Parallel Session B5 - Optoelectronics and Links / 108

Passive Optical Networks in Particle Physics Experiments

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In this paper we propose a generic Passive Optical Network (PON) platform for the distribution of synchronous, fast rate signals within particle physics experiments. Our aim is to demonstrate a versatile network architecture that will be able to serve one or more applications in future high energy physics (HEP) experiments. In order for the current PON systems to be adapted to future HEP optical link requirements, a number of challenges regarding the physical layer and medium access layer implementations have to be overcome. A prototype PON is in the process of being built and its properties in accordance to HEP tentative requirements will be measured and reported.

Summary:

Passive optical networks have attracted considerable attention from the telecommunications community over the past decade as they are considered to be the most cost efficient solution for fiber-to-the-home applications, [1-2]. In its simplest form a PON consists of a central node which is called the Optical Line Terminal (OLT), connected to a number of customer terminals called Optical Network Units (ONUs) through a passive optical tree. Communication between OLT and ONUs is bidirectional and occurs through the same fiber by employing different wavelengths for the OLT to ONU (downstream) communication and the ONU to OLT (upstream) communication. A simple optical filter installed at the OLT and at each of the ONUs is responsible for separating the upstream from the downstream signals on both sides of the network. PONs use Time Division Multiplexing (TDM) to prevent collisions from multiple ONU transmissions and they utilize a centralized architecture where all processing and decisions as to how medium should be shared is concentrated at the OLT, while ONUs are kept very simple.
A number of applications in LHC are currently using similar point-to-multipoint passive architectures such as the global clock distribution [3], and the Timing,Trigger and Control (TTC) systems [4]. These applications will require higher bandwidths and enhanced functionalities in the S-LHC and other future HEP experiments and therefore, we believe that they can benefit from the PON concept. In addition, even some applications which are currently of point-to-point in nature, such as the Data Acquisition (DAQ) system [5], might also benefit from certain aspects of PONs. The main advantages that PON technologies can bring to HEP applications are:
a) They are inherently bidirectional networks.
b) A number of protocols have already been developed and standardized for channel access arbitration, synchronization and path protection.
c) If they are used instead of point-to-point applications they can reduce the number of components installed and thus maintained in the system, as well as the fiber optic cabling.
d) Keeping track of PON technology can provide us with information about a pool of high bandwidth, cheap optical transceiver components that might be used even in non-PON architectures.
Despite their benefits, implementation of PONs in particle physics experiment environments is not straightforward. PON components and protocols have been primarily designed to serve commercial applications, such as to deliver voice and video data, but different requirements will need to be met for them to be employed in HEP. More particularly PONs need to be modified in the following ways:
1) Protocols have to be adjusted to ensure that signals are transmitted with very low latency usually within a few tens of clock cycles. For comparison, today's most latency demanding PON application is voice transmission with latency requirement in the order of 1ms. In addition, signals must have a well defined and fixed latency which should not vary with time due to environmental or other changes, for example.
2) Signals must be delivered to their destinations with very low jitter, typically in the order of a few hundred ps, as jitter uncertainties accumulate and might eventually result to system loosing synchronization.
3) A generic architecture should be able to support multiple data rates to be able to support multiple applications.
4) Hardware must be radiation hard if PONs are to be deployed at the front-end.

This paper will present the results of prototype demonstrators based on commercially available PON transceivers and FPGAs that are being built and tested against jitter and latency requirements for HEP applications. In addition, modified PON protocols for the communication between the various terminal components in such networks will be discussed.

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POSTERS SESSION / 109

The Fast Tracker Architecture for the LHC baseline luminosity

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Hadron collider experiments search for extremely rare processes hidden in much larger background levels. Only a tiny fraction of the produced collisions can be stored on tape and an enormous real-time data reduction is needed. This requires massive computing power to minimize the online execution time of complex algorithms. A multi-level trigger is an effective solution for an otherwise impossible problem.
The Fast Tracker (FTK) [1], [2] has been proposed for high quality track finding at very high rates (Level-1 output rates) for LHC experiments. FTK will use FPGA and ASIC devices in order to complement CPUs. FTK beats the combinatorial challenge with special associative memories, where parallelism is exploited to the maximum level. They compare the track detector hits to all pre-calculated track patterns at once.
The system design is defined and proposed for high-luminosity studies including low-Pt B physics and high-Pt signatures for Level-2 selections: b-jets, tau-jets, and isolated stiff light leptons. We test FTK algorithms using Atlas full simulation with WH and Hqq events at 10^-34 cm^-2 s^-1. The reconstruction quality is evaluated comparing FTK results with the tracking capability of an offline tracking algorithm. We show that similar resolutions and efficiencies are reached by FTK. The online use of the whole silicon tracker is necessary to obtain the low fake rate typical of the offline. We study the event timing inside the pipelined, data-driven FTK architecture. We compare different architectures to optimize the latency and hardware system size.

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Nuclear Science, IEEE Transactions on
Volume 55, Issue 1, Part 1, Feb. 2008 Page(s):145 - 150

POSTERS SESSION / 110

Hardware studies for the upgrade of the ATLAS Central Trigger Processor

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The ATLAS Central Trigger Processor (CTP) is the final stage of the first level trigger system which reduces the collision rate of 40 MHz to a level-1 event rate of 75 kHz. The CTP makes the Level-1 trigger decision based on multiplicity values of various transverse-momentum thresholds received from the calorimeter and muon trigger sub-systems using programmable selection criteria. In order to improve the rejection rate for the first phase of the planned luminosity upgrade of the LHC to 3 x 1034 cm-2 s-1, one of the options being studied consists of adding a topological trigger processor, using Region-Of-Interest information from the calorimeter and potentially also the muon trigger. This will also require an upgrade of the CTP in order to accommodate the additional trigger inputs. The current CTP system consists of a 9U VME64x crate with 12 custom designed modules where the functionality is largely implemented in FPGAs. The constraint for the upgrade study was to reuse the existing hardware as much as possible while not exceeding the latency envelope of 100 ns by a significant amount. This is achieved by operating the backplane at twice the design frequency and required developing new FPGA firmware for several of the CTP modules. We present the design and performance of the firmware for the input, monitoring and core modules of the CTP as well as results from initial tests of the upgraded system.

Plenary Session 6 - Programmable Logic, Boards, Crates and Systems / **111**

FPGA-based Bit-Error-Ratio Tester for SEU-hardened Optical Links

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Reliable optical links for future High-Energy Physics experiments will require components qualified for use in radiation-hard environments. To cope with radiation induced single-event upsets, the physical layer protocol will include Forward Error Correction (FEC). Bit-Error-Ratio (BER) testing is a widely used method to characterize digital transmission systems. In order to measure the BER with and without the proposed FEC, simultaneously on several devices, a multi-channel BER tester has been developed. This paper describes the architecture of the tester, its implementation in Xilinx FPGA devices and discusses the experimental results.

Summary:

In the framework of the Versatile link project [1], optical transceiver components will be tested to verify their compliance with the requirements of future radiation hard optical links in High-Energy Physics experiments. A widely accepted method to test digital transmission systems and their components is the Bit-Error-Ratio (BER) test. In order to quantify the effects of radiation the components will be irradiated and the impact of the Single-Event Upsets (SEU) on the BER will be investigated.

Measuring the BER with high confidence level (> 0.95) is usually a lengthy process, thus testing components sequentially takes too much time. Therefore, a multi-channel BER Tester (BERT) supporting the measurement of several components simultaneously has been developed. The BERT operates at multiple data rates up to a maximum of 6.5 Gbit/s. Unlike standard equipment that uses pseudo-random bit patterns, the BERT described uses the custom physical layer protocol, which is proposed by the GigaBit Transceiver (GBT) project [2]. In order to cope with the radiation induced SEUs, the protocol will include Forward Error Correction (FEC). By measuring the BER both before and after the error correction, the tool can be used to evaluate the performance of the FEC in the radiation environment.

Detailed information about the architecture, the implementation in Xilinx Virtex-4 and Virtex-5 FPGA devices, as well as a procedure to improve the measurement time will be discussed in the paper. Results of laboratory BER tests of standard components will be shown for reference and finally results from the SEU tests will be presented.

POSTERS SESSION / 112

ASPIC: LSST camera readout chip Comparison between DSI and C&S

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The ASPIC chip has been designed to readout the 3.2Gpixels of the LSST camera focal plane. The dynamic range is more than 16 bit and the noise has to be less than 7µV rms with a crosstalk better than 0.05%.
The architecture is based on a double correlated sampling. 2 methods have been investigated: differential output Dual Slope Integrator which has been chosen to be the LSST baseline and Clamp and Sample. We plan to perform a deep comparison between these methods and therefore 2 ASICs have been designed in 5V compliant CMOS 0.35µm.

Summary:

The LSST camera will have more than 3000 video-processing channels
to readout its large and highly segmented focal plane, requiring a compact readout chain.
The standard technique for analog signal processing of CCDs is "Correlated Double Sampling," which can be implemented with "Dual Slope Integrator" or "Clamp and Sample" methods. We have designed and implemented an ASIC for LSST to directly compare the strengths and weaknesses of these methods on a working device: the Analog Signal Processing asIC (ASPIC). Four channels of each method have been implemented on the same ASIC to perform direct comparisons and fine crosstalk measurements.
Video channel to video channel crosstalk due to electronics (cables, boards, chips) has to be no more than 0.05% (1::2000) with a 0.01% goal (1::10000) at 500kHz readout frequency. The other requirements on this readout chain are:
- readout noise < 7µV rms for an integration time of 500ns
- crosstalk < 0.05%
- linearity < 1%
- dynamic range 16 bits
- maximum power consumption of 25mW/channel
- working temperature 173 K
- differential ouputs driving 1kΩ // 50pF load

The chosen technology is 5V compliant CMOS 0,35µ by AMS.

A second version, ASPIC 2, containing 8 DSI channels has been submitted by the end of 2008. This version is characterized by a 3 bit programmable gain (made by capacitive feedback) of the input amplifier, and a 3 bit programmable time constant integrator in order to match the CCD output conversion and the readout frequency. In order to reduce the power consumption, an idle mode has been implemented. First measurements show an important improvement in noise which has been reduced to less than 7µV for an integration time of 500ns at room temperature. Power consumption is now around 26mW/ch also at room temperature. A very preliminary crosstalk of 0.02% has been measured on a socket mounted chip.

A CLAmp and Sample aSIC (CLASSIC) chip containing 8 channels has been submitted in march in order to perform a comparison between the two methods. CLASSIC is also characterized by a programmable

input amplifiers gain and a programmable time constant output filter.
Both ASPIC and CLASSIC will be readout with a specific Back End board containing eight 18 bits ADC channels which are the LSST Back End Board ADC, 256 kwords memory and an USB interface. This board will permit CDD correlated noise measurement.

POSTERS SESSION / 113

Silicon Photomultiplier integrated readout chip (SPIROC) for the ILC: characterization and mesurements

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The SPIROC chip is a dedicated very front-end electronics for an ILC technical prototype hadronic calorimeter with Silicon Photomultiplier (or MPPC) readout. This ASIC is due to equip a 2,000-channel demonstrator in 2009. The SPIROC chip is the successor of the ILC_SiPM ASIC presently used for the ILC AHCAL physics prototype incorporating additional features like autotriggering, pipelines, digitization as well as power pulsing. Realized in 0.35um SiGe technology it is designed in order to fulfill ILC final detector requirements of large dynamic range, low noise, low power consumption, high precision and large channel numbers.

The SPIROC is a 36-channel chip. Each channel has bi-gain amplification, auto-triggering capability, a 16-bit depth analog memory array and a 12-bit Wilkinson ADC. It allows time and charge measurements at the same time with digitized data results. The digitization is controlled and read out by the digital part of the chip.

After the submission in June 2007, extensive measurements have been carried out to characterize the chip. Results on linearity, noise, triggering, timing capability and the A/D interface etc. will be presented. The chip has been proven to be successful in calorimeter calibration as well as real physics experiments.

POSTERS SESSION / 114

Presentation of the "ROC" chips readout

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The OMEGA group at LAL has designed 3 chips for ILC calorimeters: one analog (SPIROC) and one digital (HARDROC) for the hadronic one and also one for the electromagnetic one (SKIROC). The readout and the management of these different chips will be explained.
To minimize the lines between the ASICs and the DAQ, the readout is made thanks to 2 lines which are common for all the chips: Data and TransmitOn. As the chips are daisy chained, each chip is talking to the DAQ one after the other. When one chip has finished its readout, it starts the readout of the chip just after. Moreover, during this readout, only the chip which is talking to the DAQ is powered: this is made thanks to the POD (Power On Digital) module in the ASIC. In the ILC mode, readout sequence is active during inter bunch crossing (like ADC conversion).
Another chip designed for PMM2 R&D program (PARISROC) integrates a new selective readout: that's mean only hit channels are sent to the DAQ in a complete autonomous mode.

POSTERS SESSION / 115

Characterization of Semiconductor Lasers for Radiation Hard High Speed Transceivers

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Co-authors: Christophe Sigaud [1]; Csaba Soos [1]; François Vasey [1]; Henrique Salgado [2]; Ioannis Papakonstantinou [1]; Jan Troska [1]; Luís Amaral [1]; Paulo Moreira [1]; Pavel Stejskal [1]; Spyridon Papadopolos [1]; Stephane Detraz [1]

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In the context of the versatile link project, a set of semiconductor lasers were studied and modeled aiming at the optimization of the laser driver circuit. High frequency measurements of the laser diode devices in terms of reflected and transmission characteristics were made and used to support the development of a model that can be applied to study their input impedance characteristics and light modulation properties. Furthermore the interaction between the laser driver, interconnect network and the laser device itself can be studied using this model. Simulation results will be compared to measured data to validate the model and methodology.

Summary:

Keywords: Laser, VCSEL, model, Verilog-A, transceiver, radiation hard.

SUMMARY

The versatile transceiver under development for the Super Large Hadron Collider (SLHC) experiment will have to endure severe radiation conditions while providing multiple gigabit per second data transmission capability to cover the experiments requirements [1, 2]. For this, characterization and modeling of the electro-optic components (in particular the semiconductor laser), are of upmost importance as they will enable the correct design and optimization of the transceiver [3]. They will also enable to evaluate the link performance when the physical characteristics of the device change due to the environmental circumstances.

A measurement methodology will be presented whose results lead to the implementation of a model with broad validity. This model accommodates several different laser types (Fabry-Perot, Distributed Feedback, Vertical Emission) [4-7]. The laser model is implemented in Verilog-A for ease of use by integrated circuit designers, and it aims at easing the design of robust systems capable of complying with the demanding requirements of high energy physics experiments.

Since the impedance mismatch between the driver and the laser should be kept as low as possible to decrease inter-symbol interference, jitter and power loss, a very accurate model of the laser chip input and parasitic network was developed. It will be shown that the theoretical model is in good agreement with experimental data and that it enables correct design of the transmitter circuitry of the laser driver. The results of the study of an impedance matching network and signal pre-emphasis will be shown.

Current work is focusing on the use of the model to predict the performance degradation with environmental conditions and analyses of the system sensitivity to manufacturing parameter deviations [8].

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POSTERS SESSION / 116

Position Measurements with Micro-Channel Plates and Transmission Lines using Pico-second Timing and Waveform Analysis

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Micro-Channel Plates anodes are coupled to fast transmission lines in order to reduce the number of electronics readout channels, and provide two-dimensions position measurements using centroids and two-ends delay timing. Tests using a laser and waveformanalysis have shown that resolutions of a few hundreds of microns along thetransmission line can be reached. This technique is planned to be used in novel Micro-channel Plates devices integrating the transmission lines as anodes.

Summary:

10 and 25 micron pores Micro-Channel Plates devices (MCP) have been connected to 50 Ohms transmission lines printed circuit cards and tested using a 408nm laser focused on the window entrance of the MCP. The numbered of amplified photo-electrons is evaluateded using a single photo-electron sensitive photo-multiplier. Once the velocity along the 10cm-long transmission line is determined, the position along the line is derived from the difference in delays between the two ends of the card. Since the two signals originate from the same pulse at the output of the MCP, their shapes are strongly correlated. Waveform analysis using least square fits to a known template waveform allow extracting the time of arrival of the
pulse at the two ends of the line. The differences of these times show a spread of a few picoseconds, depending mainly on the signal to noise ratio, that depends in turn upon the number of incident photoelectrons and the gain of the MCP set by the high voltage applied to the MCP pores.
Results are presented for 18, 50, and 158 Photoelectrons and high voltages values corresponding to signals with amplitudes between 10 and 500 mV. These results are
in good agreement with both simulations, and timing measurements achieved with off-the-shelf Constant Fraction Discriminators and Time to Amplitude converters.
Results obtained from tests at the Advanced Photon Source at the Argonne National Laboratories where the transmission lines are sitting in the vacuum as close as possible to the MCP output, are also presented and compared to detailed simulations. From these results, it is possible to optimize a design where the transmission lines are integrated to the MCP device itself. This design is also briefly discus

Parallel session A1 - ASICs / 117

Reduction techniques of the back gate effect in the SOI Pixel Detector

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A pixel sensor in 0.2um Silicon-On-Insulator (SOI) CMOS technology, consisting of a thick sensor layer and a thin circuit layer with an insulating buried-oxide in a monolithic chip, has many advantages. However, it has been found that applied electric field in the sensor layer also affects transistors in the adjacent circuit layer. Thus, full depletion voltage cannot be applied. To overcome this, we performed TCAD simulation and added an additional p-well (buried p-well) in the SOI process. Simultaneously, we attempt vertical integration of two SOI chips by using a micro-bonding technique. Designs and preliminary results will be presented.

Summary:

We are developing Silicon-On-Insulator (SOI) pixel detector. While our fabricated SOI pixel detectors operate as we expected, at this moment a sufficient detector bias voltage can not be applied due to so called back gate effect. To overcome this, we have introduced two new techniques in the fabrication processes, based on TCAD simulations performed to understand the phenomenon in details.
SOI technology enables a monolithic pixel detector by bonding thick, high-resistivity semiconductor sensors and thin, low-resistivity readout electronics layer with insulating buried oxide layer (BOX). Contacts between the sensing nodes of the sensor layer and the readout circuitry are made through the BOX layer.
Compared to conventional bulk CMOS pixel sensors, SOI pixel sensor has following advantages:
* No mechanical bump bonding; minimizing multiple scattering in the detector and smaller pixel size is possible.
* Small parasitic capacitance (~10fF) of sensing nodes gives large conversion gain and lower noise.
* Small active volume in each transistor ensures latch-up immunity and high radiation tolerance.
* Both sensor and readout electronics can be fabricated with the industry standard SOI process; further progress and lower cost are expected.
While the SOI structure is ideal for realizing the monolithic pixel detector, applied electric field in the sensor layer also affects transistors in the adjacent LSI circuit layer (back gate effect). Due to this phenomenon, sufficient bias voltage to make the sensor full depletion can not be applied at this moment.
To overcome this, we made TCAD simulation to understand the phenomenon in detail. Based on these TCAD simulation study, we have tried two methods in the fabrication process.
First method is an introduction of a buried p-well (BPW) in the substrate. A p-type Dopant is implanted through the top Si layer and forms p-well just below the buried oxide (BOX) layer. This BPW region acts as a Faraday cage to shield the electric field from the Sensor layer and the transistors in the top LSI circuit layer may not be affected. The doping level of the BPW is about 3 orders lower than that of the p+ sensor node and drain/source region, so it does not affect the transistors in the top LSI circuit layer.
The other method is a 3D vertical integration technique. We will bond two SOI wafers face to face by using micro-bump technology of ZyCube Co. Ltd. Minimum pitch of the bump is 5um. This will not

only enables higher circuit integration density but also will separate the sensitive circuit regions from the sensor.
We have developed a 0.2 um fully-depleted (FD) SOI pixel process in collaboration with OKI Semiconductor Co. Ltd. Additional processing steps to create BPW and contacts between sensor nodes and readout circuitry were established.
To reduce development cost, we have been organizing MPW (Multi Project wafer) runs. Two MPW runs were completed and one runs is now being processed. In each run, we have about 16 designs from our collaborators.
In this presentation, the techniques and preliminary results will be shown.

Parallel Session B3 - Packaging and Interconnects / 118

Thin, Fully Depleted Monolithic Active Pixel Sensor with Binary Readout based on 3D Integration of Heterogeneous CMOS Layers

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On the way towards fast, radiation tolerant and ultra thin CMOS sensors, we propose new generation of devices based on commercial availability of vertical integration of several CMOS wafers (3D Electronics). The proposed prototype device is a 245x245 pixel array with a pitch of 20 μm, In the first silicon layer charge sensing diode and the input buffer amplifiers are integrated, using 0.6 μm CMOS on high resistivity epitaxial wafers. Following stage of processing electronics (charge integration, time invariant shaping and signal discrimination), are placed in the second silicon layer (0.13 micron CMOS). Third layer (same 0.13 CMOS) is used for implementation of fast, digital (binary) readout.

Summary:

A On the way towards fast, radiation tolerant and ultra thin CMOS sensors, we propose new generation of devices based on commercial availability of vertical integration of several CMOS wafers (3D Electronics). In this process, each wafer is thinned down to less than 10 microns end equipped with through-silicon vias (TSV) allowing for electrical interconnection between wafers at very small pitch (few microns) and with minimum material budget. The proposed prototype device is a 245x245 pixel array with a pitch of 20 μm, providing active area of 5x5 mm2. In the first silicon layer charge sensing diode and the input buffer amplifiers (source follower in this case) are integrated, using 0.6 μm CMOS process on high resistivity epitaxial wafers. Pioneering application of such substrate which is fully depleted at less than 5V for particle tracking sensors results in higher signal seen at the seed pixel, reduces strongly cluster multiplicity and in particular, due to fast charge collection (<5ns), improves radiation hardness with respect to non-depleted CMOS MAPS by at least order of magnitude. Outputs of first layer buffer amplifiers are vertically coupled (through poly-poly capacitor) to the following stage of processing electronics (charge integration, time invariant shaping and signal discrimination), placed in the second silicon layer (0.13 micron CMOS). For this stage we have chosen a “shaperless front-end” (SFE) structure already fabricated in similar 0.13 μm process, tested and evaluated. Expected equivalent noise charge (ENC) is less than 15 electrons, for a pulse peaking time of about 500 ns, voltage gain at the discriminator input of 150 μV/e (300 μV/e for the second versions) and for total (analog) power dissipation of ~5μW/pixel. In connection with fully depleted, 14 μm thick epitaxial substrate as a charge sensing layer, this brings very comfortable signal-to-noise ratio of more than 40 for detection of minimum ionizing particles. Third silicon layer (also 0.13 micron CMOS) is used for implementation of digital (binary) readout, with a fast, data driven, self-triggering data flow. The idea is to read in less than 2 μs the X and Y projection of a hit pattern, following a trigger signal set by the first hit pixel. In addition to the presented sensor, other pixel structures have been submitted for production at the same

time, aiming testing of different, more power efficient solutions for analog processing (rolling-shutter architecture and novel, very high gain (1-2 mV/el) and low power (<1μW/pixel) time invariant amplifier-discriminator). Integrated three silicon layer stack described above can be in principle thinned down to less than 50 μm, still keeping full sensor functionality and quality. This may pave a way for the construction of new generation of high precision vertex detectors.
Details of the proposed design (recently submitted for fabrication) and preliminary test results will be presented. Possible extensions and applications will be discussed.

Parallel Session B5 - Optoelectronics and Links / 119

The Versatile Transceiver Proof of Concept

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Co-authors: Christophe Sigaud [1]; Csaba Soos [1]; Francois Vasey [1]; Ioannis Papakonstantinou [1]; Pavel Stejskal [1]; Sergio Ruì Silva [1]; Spyros Papadopoulos [1]; Stephane Detraz [1]

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SLHC experiment upgrades will make substantial use of optical readout to enable high-speed data readout and control. The Versatile Link project will develop and assess optical link architectures and components suitable for deployment at SLHC. The on-detector element will be bidirectional opto-electronic module: the Versatile Transceiver that will be based on a commercially available module type minimally customized to meet the constraints of the SLHC on-detector environment in terms of mass, volume, power consumption, operational temperature and radiation environment. We report on the first proof of concept phase of the development, showing the steps towards customization and first results of the radiation resistance of candidate optoelectronic components.

Summary:

The Versatile Link project aims to provide a multi-gigabit per second optical physical data transmission layer for the readout and control of Super LHC (SLHC) experiments. Point-to-point bidirectional (P2P) as well as point-to-multipoint (PON) architectures are foreseen to be supported by the systems and components currently being assessed and developed. The front-end component that will enable the configuration of any of the Versatile Link's supported architectures is a bi-directional module composed of both optical transmitter and receiver: the Versatile Transceiver (VTRx).
The components situated on the detectors at the front-end must meet strict requirements imposed by the operational environment for radiation- and magnetic-field tolerance, low temperature operation (between -40 and -10℃), low mass and volume, and low power consumption. The radiation environment is particularly challenging, as any device placed at the front-end must survive the Si-equivalent of 1.5×1015 n (1MeV)/cm2 fluence and 500kGy ionizing dose.
Experience with optical links deployed in LHC experiments has indicated that even the opto-electronic modules situated on the detectors should be sufficiently rugged to allow handling by integration teams relatively unfamiliar with their use. For this reason the VTRx development aims to minimally customize a commercial form factor bidirectional transceiver module that features a direct optical connector interface. The most promising commercial form factor is the SFP+, which measures approx. 50mm long by 10mm wide by 14mm high. Such a commercial module contains a laser diode driver and laser in the transmit path, a photodiode plus transimpedance and limiting amplifiers in the receive path, along with a microcontroller for module control. The VTRx will omit the microcontroller, replace the ASICs with custom-designed radiation resistant versions, and add radiation-resistant commercially available laser- and photo-diodes.
The proof of concept is the first phase of the three-phase Versatile Link project, which for the VTRx means the demonstration that a standard commercial transceiver type can be modified so as: (a) to reduce the material of the commercial package to make it suitable for deployment within SLHC detector volumes; and (b) to include optoelectronic devices of our choosing that we believe will lead to sufficient radiation tolerance and low power consumption. In this paper we will present how be have achieved these goals by providing details of the internals of the module that we have built and showing results of the optoelectronic characterization that has been carried out.
Additionally, a critical requirement for the choice of laser- and photo-diodes to be included in the VTRx is that of radiation resistance. A first survey of devices has been carried out to gauge their resistance to

displacement damage (the most challenging type of radiation damage for active opto-electronic devices). This test irradiated a number of commercially-available devices at the neutron irradiation beamline of the Cyclotron facility of the Université Catholique de Louvain. Results will be shown for both irradiation and annealing, leading to preliminary conclusions as the suitability of these commercial devices for use in the VTRx.

Parallel Session A5 - ASICS / 120

The GBTIA, a 5 Gbit/s radiation-hard optical receiver for the SLHC upgrades

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This paper presents a 4.8 Gbit/s optical receiver designed in a 0.13 μm CMOS process as part of the GBT project. The receiver consists of a transimpedance amplifier (TIA) and a limiting amplifier. A differential cascode structure with inductive peaking is adopted for the TIA to achieve high gain, high bandwidth and low input referred noise. Experimental results at room temperature show an open eye diagram at 4.8 Gbit/s with rise time < 40 ps, a bandwidth of 4 GHz, and a sensitivity of < -16 dBm for a BER of 10-12. The total chip power consumption is < 120 mW.

Summary:

The Gigabit Bi-directional Transceiver (GBT) is a high-speed optical transmission system with a data rate of 4.8 Gbit/s currently under development for HEP applications. This system is intended to be used as bi-directional optical links in radiation environments for the Super LHC upgrade.
At the front end of the GBT chip set is the optical receiver: the GigaBit Transimpedance Amplifier (GBTIA). This paper presents the 4.8 Gbit/s, fully differential, and highly sensitive GBTIA chip designed and implemented in 0.13 μm CMOS process. The chip consists of a low-noise, high-bandwidth transimpedance amplifier (TIA) and a high performances limiting amplifier (LA).
The TIA adopts a differential cascode structure with series inductive peaking to achieve high transimpedance gain, high bandwidth, and low input referred noise. The Photo Detector (PD) current is AC coupled to the TIA using on-chip capacitances. The capacitive coupling rejects the DC current of the PD and allows for a fully differential structure with high power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR). To cope with a potentially high leakage current in the PD induced by radiation, a novel PD biasing circuit is designed in the TIA to ensure the proper biasing of the PD for a leakage current ranging from 1 pA to 1 mA.
The LA is designed with four limiting amplifier stages followed by a 50 ohm output stage to achieve high gain and high bandwidth. Each limiting stage employs a modified Cherry-Hooper structure with resistive loading and active inductive peaking to enhance the bandwidth. The four limiting stages are sized with increasing current and transistor dimensions capable of delivering 8 mA to the output stage while maintaining a high bandwidth.
The GBTIA chip has been tested with a high-frequency PD in the lab at room temperature. The experimental results show an open eye diagram at 4.8 Gbit/s with 40 ps rise time. At 4.8 Gbit/s, the measured sensitivity with 27-1 PRBS is lower than -16 dBm for a BER of 10-12. The chip achieves an overall transimpedance gain of 70 Kohm with a measured bandwidth of 4 GHz. The total power consumption of the chip is less than 120 mW and the chip die size is 0.75 mm x 1.25 mm. Irradiation testing of the chip is currently under way; both pre- and post-irradiation test results will be presented at the conference.

Parallel session A2 - ASICs / 121

A SiGe ASIC Prototype for the ATLAS LAr Calorimeter Front-End Upgrade

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We have designed and fabricated a very low noise preamplifier and shaper to replace the existing ATLAS Liquid Argon readout for use at Large Hadron Collider upgrade (SLHC). IBM's 8WL 130nm SiGe process was chosen for its radiation tolerance, low noise bipolar NPN devices, wide voltage range and potential for use in other LHC detector subsystems. The required dynamic range of 15 bits is accomplished with a single stage, low noise, wide dynamic range preamp followed by a dual range shaper. The low noise of the preamp is made possible by the low base spreading resistance of Silicon Germanium NPN bipolar transistors. The relatively high voltage rating of the NPN transistors is exploited to allow a gain of 650V/A in the preamplifier, which eases the input voltage noise requirement of the shaper. Each shaper stage is designed as a cascaded differential op amp doublet with a common mode operating point regulated by an internal feedback loop. Preliminary measurement of the fabricated circuits indicates their performance is consistent with the design specifications.

Summary:

Although some components of the present LAr electronics design may be adequate for use in SLHC the lack of spares and elimination of the processes in which the custom ASICs were designed means that the complete ATLAS LAr electronics chain will need to be redesigned for operation at SLHC.

Our work characterizing IBM's 8WL process has qualified this process for use at much higher levels than required for the LAr electronics (300krad ionizing radiation dose and 1013 neutrons/cm**2 fluence) and makes this process an obvious candidate. The ideal behavior of the SiGe bipolar NPN's and their very low base resistance makes them compelling components to be considered in this low noise wide dynamic range application.

Preamplifier Design- The preamplifier is based on the "super common base" architecture as the one presently installed in the LAr front-end boards described in previous publications. Thanks to the SiGe low spreading base resistance it employs an input transistor of manageable size (emitter length 4 x 20μm, 2 emitter stripe geometry) biased at 8mA collector current. Simulations predict that the preamplifier achieves good integral non-linearity (INL< 1%) and an overall equivalent series noise of ~0.3nV/√Hz while dissipating 42mW.

Shaper Design – It was decided at the outset to use a differential design to help eliminate common mode pickup on and off chip. A series simple translinear configuration was examined and rejected due to its excessive noise. Instead, a differential operational transimpedance amplifier (OTA) gain block followed by a unity gain buffer was implemented using 2.4V PMOS and NPN with 20μm active circuit elements. Since the preamplifier output is at 5V relative to ground , an AC coupling is necessary. One advantage of this approach is that it allowed us to implement a relatively low gain common mode amplifier to maintain a stable DC operating point. The shaper realizes a CR-(RC)2 transfer function, and achieves an input equivalent voltage noise of about 2.2nV/√Hz.

Fabrication - The prototype ASIC fabricated through MOSIS consists of four independently powered preamplifiers and two dual gain shaper stages on a 1.6 X 2.1mm die housed in a 9X9mm open cavity QFN64 package. Packaged ASICS were received in March.

Measurements - All preamp and shaper circuits are functional with gain, shape and dynamic range close to that predicted by SPICE simulation of the extracted layout. Preliminary measurements show good linearity. Work is underway to design a PCB for a complete characterization over the summer.

We intend to discuss the design implementation and measurements of power, linearity, noise and radiation effects.

POSTERS SESSION / 122

Radiation hardness studies of a 130 nm Silicon Germanium BiCMOS technology with a dedicated ASIC

Author: Sergio Díez[1]

Co-authors: Abraham Seiden [2]; Akil K. Sutton [3]; Alexander A. Grillo [2]; Edwin Spencer [2]; Forest Martinez-McKinney [2]; Godwin Mayers [4]; Hartmut F.-W. Sadrozinski [2]; Helmut Spieler [5]; Igor Mandic [6]; John D. Cressler [3]; M. Newcomer [4]; Max Wilder [2]; Miguel Ullán [1]; Nandor Dressnandt [4]; S. Phillips [3]; Sergio Rescia [7]; V. Emerson [7]; Walter Kononenko [4]; Yu Tazawa [4]

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We present in this paper radiation hardness studies on devices of the 130 nm 8WL Silicon Germanium (SiGe) BiCMOS technology from IBM. This technology has been proposed as one of the candidates for the Front-End (FE) readout chip of the upgraded Inner Detector (ID) and the Liquid Argon Calorimeter (LAr) of the ATLAS Upgrade experiment. Gamma, neutron and proton radiation experiments have been scheduled using a purposely designed ASIC in order to take into account all radiation damage mechanisms of the devices. A study of the influence of thermal neutrons on the radiation hardness of devices of this technology has also been scheduled.

Summary:

Large Hadron Collider (LHC) upgrade, the Super-LHC, will imply a luminosity increase in the experiment of an order of magnitude. This will mean a significant increase in the radiation levels inside the ATLAS detector. The current Semiconductor Tracker (SCT) and the readout electronics for the Liquid Argon Calorimeter (LAr) will have to be replaced completely in order to deal with the increased luminosity and the enhanced degradation created by the radiation environment. The 8WL SiGe BiCMOS technology from IBM has been selected by the SiGe group as one of the candidate technologies for these new readout chips. For this application, one of the main features of this technology to be validated is its radiation hardness to the high radiation levels expected in the experiment. In this work we present the experiments scheduled for the full study of the radiation resistance of the IBM 8WL technology.

A purposely designed test chip has been fabricated on the IBM 8WL process for these experiments. The SiGBiT ASIC includes 36 bipolar transistors, in the form of 18 bipolar differential pairs, of different performances and emitter geometries, along with a CMOS test structure, similar to the 8RF IBM test structure previously used by the CERN microelectronics group. A low mass Printed Circuit (PCB) test board has also been fabricated to facilitate irradiation and testing with low activation of the test chip. ASICs will be mounted on these test boards and devices will be wire-bonded to external pads on the test boards.

We have scheduled gamma, neutron and proton irradiations in order to take into account all radiation damage mechanisms on the devices under study, i.e., ionization, atomic displacement damage, and the combination of both, respectively.

Gamma irradiations will be performed at Brookhaven National Laboratory (BNL) facilities, in USA, and at CIEMAT facilities, in Spain. Devices will be exposed to a total dose of 0.65, 5, 10, 30 ad 50 Mrad(Si). A detailed irradiation program for the study of Enhanced Low Dose Rate Sensitivity (ELDRS) effects on the technology has also been developed.

Devices will be exposed to 800 MeV protons during fall of 2009 at the Los Alamos LANSCE facility. We expect to reach fluences up to 1e15 p/cm2.

Neutron irradiations will be performed at the TRIGA Nuclear Research Reactor of Josef Stefan Institute (JSI) in Ljubljana, Slovenia. Samples will be exposed to 1e14, 2e14, 6e14 and 1e15 neq /cm2 fluences. Devices will remain with all their terminals shorted together during irradiation. Samples will be irradiated inside a cadmium (Cd) shielding box, so as to limit radiation damage created by thermal neutrons. In

order to observe the effect of slow neutrons on the radiation damage of devices, some devices will be irradiated without Cd shielding. Activation of three board materials (standard FR-4, halogen-free and alternate halogen-free) were measured after exposure to 1e14 neq /cm2 inside the Cd shielding to determine which would result in reasonable deactivation times – the time required before post-radiation tests can be performed. Samples from standard FR-4 material showed no measurable activity four weeks after irradiation. Test boards were fabricated with this material.

At the time of TWEPP conference, we expect to have finished the gamma and neutron irradiation program. These tests will give us reliable results about the radiation hardness of the IBM 8WL technology and a final result about the suitability of this technology for its application on the S-LHC experiment.

POSTERS SESSION / 123

OMEGAPIX : 3D electronics chip for pixel readout

Author: Damien Thienpont[1]

[1] *IN2P3/LAL*

The OMEGAPIX circuit is the first front end prototype ASIC designed at LAL (Orsay) using 3D technology for the ATLAS upgrade SLHC pixel project. This work has been done inside a new international consortium for development of Vertical Integrated Technologies for Electronics and Silicon SEnsors (VITESSE), which has gathered, not only 3 IN2P3 (France) institutes, but also Fermilab (USA) and INFN (Italy) HEP laboratories . One goal of the consortium is to explore the range of design options available that could fit the physics requirement of future high energy colliders.
LAL focused its efforts on the specific approach of sub-micron readout circuit dedicated for innovative high granular planar pixel sensors for Atlas upgrade pixel detector.
This circuit has been submitted on May 2009. It is build in a two tier IC stacks: one analogue layer and one digital layer. For the manufacturing of the 2D part, it has been realized in 0.13um Chartered technology. For the 3D part the Tezzaron process has been used. The process is wafer to wafer technology, face to face, via first and uses Copper-Copper bonds. The circuit embeds 64x24 readout channels that have been developed to match the following requirements : low noise (100 e-), low threshold (1000 e-), very low power consumption (3 uW/ch) and a high granularity (50x50 um). This electronics chip will also allow us to study various flavours of transistors types (normal, low VT, 3p3) and their behaviour when exposed at high radiation levels compatible with SLHC doses.
One other expected improvement of the 3D technology that will be checked is the reduction of substrate coupling between analogue and digital parts and thus should allow us to lower efficiently the pixel signal threshold.
To reach these requirements, a simplified common source configuration has been designed to perform the charge preamplifier and the shaper. A special care has been taken for the minimization of the global capacitance, and, for the shaper, a variable gain and a DC level adjustment have been designed. Design considerations, simulation and hopefully first tests results will be presented.

Authors : Lounis Abdenour, Christophe de La Taille, Gisèle Martin-Chassard, Yixian Guo, Damien Thienpont

Parallel session B2b - Radiation tolerant components and systems / 124

Measurement of radiation damage of 130nm hybrid pixel detector readout chips

Author: Richard Plackett[1]

Co-author: Xavier Llopart [1]

[1] *CERN*

We present the first measurements of the performance of the Medipix3 hybrid pixel readout chip after exposure to significant x-ray flux. Specifically the changes in performance of the mixed mode pixel architecture, the digital periphery, digital to analogue converters and the e-fuse technology were characterised. A high intensity, calibrated x-ray source was used to incrementally irradiate the separate regions of the detector whilst it was powered. This is the first total ionizing dose study of a large area pixel detector fabricated using the 130nm CMOS technology.

Summary:

The Medipix3 hybrid pixel detector readout chip is the first 130nm CMOS large area pixel detector to be fabricated. It is expected that the SLHC generation of pixel detectors will use 130nm or 90nm technology, both of which are expected to be significantly more radiation tolerant than the current generation of sensors using 250nm CMOS. This expectation is based largely upon the use of a significantly thinner oxide layer in the 130nm devices and some preliminary evaluation of individual components [1]. It is hoped that these measurements will confirm this intrinsic improvement in a complete large area device, rather than small test structures.
The study will include measurements of the evolution of the performance of the pixel architecture, the digital to analogue converters (DACs) in the chip's periphery, the custom LVDS drivers used to read out the chip and the e-fuse logic that sets the chip's identification number. The tests on the pixel region will concentrate on threshold scans of an injected test pulse and of the noise level. This will yield information on the gain variation of the pixels after irradiation and the position and extent of the noise within the chip. The linearity of the DACs within the chip's periphery will be measured to check for any drift with irradiation. The operability of the chip's digital periphery including its IO logic and LVDS drivers will be checked continuously throughout the studies to give an indication of the point of failure. In addition the e-fuses that set the chips identity code will be read continuously to confirm their survivability. Changes in power consumption of the chip as it is irradiated will also be monitored.
As there are only a very limited number of Medipix3 chips currently available these initial tests will be performed on a single chip, incrementally irradiating a region of the pixel matrix and then the periphery. As Medipix3 has been designed primarily for x-ray imaging in medical applications, it uses mainly the standard 'open' gate transistors and has no features to combat single event upsets (SEUs). For this reason the study will concentrate on the total ionizing dose rather than the SEU cross section. A demonstration of the intrinsic radiation hardness of this technology has some significant implications for the design of future chips for use in HEP, synchrotrons and beyond.

[1] F. Faccio, "Radiation issues in the new generation of high energy physics experiments," Int. J. High Speed Electron. Syst., vol. 14, pp. 379-399, 2004.Power consumption

POSTERS SESSION / 125

Design and measurements of 10 bit pipeline ADC for the Luminosity Detector at ILC

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The design and preliminary measurement results of a prototype 10 bit pipline ADC for the Luminosity Detector (LumiCal) at the International Linear Collider (ILC) are presented. The motivation for the chosen architecture is presented and followed by the description of the core blocks. The prototype was fabricated in 0.35 um CMOS technology. The preliminary measurements of static (INL, DNL) and dynamic (SHNR, THD) parameters were performed to understand and quantify the circuit performance. The ADC was found to be fully functional for sampling frequencies up to about 40 MHz. The measurements performed at 30 MHz sampling showed the INL below 1 LSB and the DNL below 0.5 LSB.

Summary:

Two analog to digital conversion schemes are presently under study for the Luminosity Detector readout. One with relatively slow ADC per each front-end channel and one with faster ADC per group of (about) 8 channels. First option would be the simplest solution from the design point of view while the second one would save the area. The ILC bunch crossing rate is about 3 millions event per second so the first option (ADC per channel) would require an ADC with sampling rate of about 3 Msample/s while the second would require a sampling rate of about 24 Msample/s.
The aim of this work was to design an ADC working up to about 30 MHz sampling frequency. One of the most efficient architectures assuring a good compromise between the speed, the area and the power consumption is a pipeline ADC. This architecture was chosen for the LumiCal data conversion. Since in the ILC experiment each 1 ms active beam time will be followed by 200 ms pause the requirements on readout electronics power dissipation may be strongly relaxed if the powering is switched off in the pause.
The present ADC design consist of sample-and-hold circuit, 9 1.5-bit pipeline stages and digital correction logic. The whole ADC is fully differential. Each pipeline stage contains two pairs of sampling and feedback capacitors, telescopic gain boosted amplifier, two dynamic latch comparators, several switches and small logic block. To save the area and the power scaling of capacitors and currents is implemented in the following stages. In addition the power and the clock switching off is implemented.
The prototype ADC was fabricated in 2-poly, 4-metal, 3.3 V, 0.35 um technology. A dedicated test setup based on Xilinx FPGA, allowing ADC tests up to about 100 MHz sampling frequency, was build. The preliminary tests showed full functionality of the prototype. The static measurements were performed for 30 MHz nominal sampling frequency and input voltage range between 1 – 2 V, corresponding (after single-ended to differential conversion) to 2 V full differential input range. The results were analyzed using standard histograming method. The measured DNL was found to be less than ±0.5 LSB (the worst case was 0.4 LSB) while the INL was less than ±0.9 LSB.
The effective number of bits calculated from static INL reached about 9.6. No missing codes were found. The preliminary dynamic measurements were performed with a sin-wave input. The Signal to Non Harmonic Ratio (SNHR) of about 57 dB was measured. The Total Harmonic Distortion (THD) of about -56 dB was measured. These first results of dynamic measurements require further studies since the measured values may be affected by the test setup. In particular by the sin-wave distortion of the signal generator and by the single-to-differential conversion (on PCB) before the ADC. The measured ADC current consumption was about 10 mA for analog blocks and 6 mA for digital part at smapling frequency 30 MHz.

Parallel session B2b - Radiation tolerant components and systems / 126

Radiation tests on the complete system of the instrumentation of the LHC Cryogenics at the CERN Neutrinos to Gran Sasso (CNGS) test facility

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Co-authors: GONZALO PENACOBA FERNANDEZ [1]; JOSE DE LA GAMA SERRANO [1]; JUAN CASAS CUBILLOS [1]

[1] *CERN*

There are more than 6000 electronic cards for the instrumentation of the LHC cryogenics, housed in crates and distributed around the 27km tunnel. Cards and crates will be exposed to a complex radiation field during the 10y of LHC operation. COTS and rad-tol ASIC have been selected and individually qualified during the design phase of the cards. The test setup and the acquired data presented in this paper target the qualitative assessment of the compliance with the LHC radiation environment of an assembled system. It is carried out at the CNGS test facility which provides exposure to LHC-like radiation field.

POSTERS SESSION / 127

A 10-bit 40MS/s pipelined ADC in a 0.13µm CMOS process

Author: Hugo Franca Santos[1]

[1] *CERN*

This paper presents a 10-bit analogue to digital converter (ADC) that will be integrated in a general purpose charge readout ASIC that is the new generation of mixed-mode integrated circuits for Time Projection Chamber (TPC) readout. It is based on a pipelined structure with double sampling and was implemented with switched capacitor circuits in eight 1.5-bit stages followed by a 2-bit stage. The power consumption is adjustable with the conversion rate and varies between 15 and 34mW for a 15 to 40MS/s conversion speed. The ADC occupies a silicon area of 0.7mm2 in a 0.13µm CMOS process and operates from a single 1.5V supply.

Summary:

In the framework of the research activities at CERN for the EUDET collaboration, a general purpose charge readout chip is being developed. It consists of a programmable charge amplifier and shaper, an analogue-to-digital converter, digital blocks with numerous flexible functions and memory. This paper is focused on the ADC which was entirely developed at CERN and prototyped in a multi project wafer (MPW).
The pipelined ADC architecture was elected since it offers the best compromise in terms of power and area for the speed and resolution required. It was implemented with switched capacitor circuits in eight 1.5-bit stages followed by a 2-bit stage. The half-bit of redundancy in each one of the 1.5-bit stages allows a relaxed accuracy of the comparator's thresholds; therefore low power dynamic comparators were used.
The sampling switches were implemented with complementary low-threshold FETs and guarantee a maximum signal distortion below -72dB over a 20MHz bandwidth. Since low on-resistance is required these switches are relatively large, however a charge injection cancellation scheme with dummy transistors minimizes the amount of change injected. In addition, the bottom sampling technique was employed making the sampling circuit nearly immune to voltage dependant charge injection.
The multiplying digital-to-analogue converter (MDAC) blocks are equipped with rail-to-rail differential output operational amplifiers with 104dB of DC-gain and 314MHz of unitary gain bandwidth. These amplifiers have continuous common mode feedback and a multipart frequency compensation scheme that provides a phase margin of 70º for the main amplifier and 57º for the common mode loop.
The double sampling technique was employed in this design. It consists on the duplication of the sampling circuit permitting a full exploitation of the amplifier's power; therefore the bandwidth is reduced to half of their counterparts in the standard pipelined configuration. A skew insensitive sampling circuit was used to eliminate disparities in sampling time between odd and even samples.
The biasing circuit is based in the beta-multiplier principle that provides constant Gm over a wide range of temperature and is process independent. This circuit allows the tuning of the biasing currents from outside the chip, so the analogue power consumption can match the required sampling speed. In this prototype the power consumption can be tuned from 15 to 34mW for a sampling speed between 15 and 40MS/s.
This design was done in a 0.13µm CMOS process from IBM with analogue options that allowed the use of metal-insulator-metal (MIM) capacitors which are the best available in terms of capacitance accuracy, matching and voltage dependence. This is the same process in which the programmable amplifier shaper amplifier (PASA) was prototyped in a 16-channel chip called PCA16, however with different back end of line (BEOL) options.
For the completeness and enhancement of this ADC a few updates are possible: the inclusion of the redundant sign digit code (RSD) block that combines the data from the stages into a single digital word; the scaling of the MDACs which would lead to a significant reduction of area and power consumption; the integration of a standby mode and the widening of the power efficient operating frequency range.

Parallel session B1 - Systems, Installation and Commissioning / 128

In-situ performance of the CMS Preshower Detector

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[1] *CERN*

The CMS Preshower detector, based on silicon strip sensors, was installed on the two endcaps of CMS in March/April 2009. First commissioning showed that of the 137000 electronics channels virtually all were fully operational. This report summarizes the electronics integration (on-detector) and in-situ performance in terms of noise (including common-mode pickup), channel-to-channel variations, gain uniformities etc. Comparisons are made between these measurements and those made during assembly and system-tests. First observations of in-situ cosmic-rays are expected during the Summer.

Summary:

This article describes the electronics performance of the CMS Preshower detector. The Preshower forms part of the CMS Endcap Electromagnetic Calorimeter system and is based upon layers of silicon strip sensors with their associated front-end electronics. Both endcaps were installed and commissioned in CMS during March/April 2009.
We start by giving an overview of the complete system, both on-detector and off-detector, with special focus on those parts that contribute to the electronics performance, such as the engineering design, silicon detectors, front-end electronics, power supplies (and associated distribution systems), cables and optical fibres. Indeed the integration of the on-detector components was a major challenge, given the extremely limited space available; Novel solutions were found to route all of the on-detector cables and fibres.
The off-detector control and readout electronics also contribute to the overall performance, so these too are described, including the algorithms implemented to perform data sparsification. These off-detector components also have the task of configuring the thousands of front-end chips, an operation that needs to be both fast and reliable. Finally in this section we give an overview of the slow control and safety systems (both hardware and software) that influence the performance - such as temperature and humidity control.
The second section presents the performance of the electronics, in terms of such quantities as intrinsic noise, linearity, dynamic range and susceptibility to influence from external (and internal) noise sources. We show these performances in absolute values and also in terms of uniformity across the detector. In our “calibration” mode we can obtain a signal to noise ratio (for single incident minimum ionizing particles - MIPs) of better than 9 with a linear dynamic range up to about 70 MIPs. In “normal” mode of operation the S/N for single MIPs is lower, at around 2.5, but the dynamic range is extended up to more than 400 MIPs. External influences (e.g. from neighbouring detectors) are shown to be small in relation to the intrinsic noise.
During the Summer the CMS detector will be configured to trigger on cosmic muons, both with and without the 4T magnetic field. We expect to detect the first in-situ signals inside the Preshower. A discussion on the results of these observations is foreseen.

Parallel session B2a - Production, testing and reliability / **129**

Picosecond time measurement using ultra fast analog memories.

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The currently existing electronics dedicated to precise time measurement is mainly based on the use of constant fraction discriminators (CFD) associated with Time to Digital Converters (TDC). The time resolution measured on the most advanced ASICs based on CFDs is of the order of 30 ps rms. TDC architectures are usually based either on a voltage ramp started or stopped by the digital pulse, which offers an excellent precision (5 ps rms) but is limited by the large dead time, or on a coarse measurement performed by a digital counter associated with a fine measurement (interpolation) using Delay Line Loop, which exhibits a timing resolution of 25 ps, but only after a careful calibration. In the meantime, alternative methods based on digital treatment of the analogue sampled then digitized detector signal have been developed. Such methods permit achieving a timing resolution far

better than the sampling frequency. Digitization systems have followed the progress of commercial ADCs, but the latter have prohibitory drawbacks as their huge output data rate and power consumption. Conversely, high speed analog memories now offer sampling rates far above 1GHz at low cost and with low power consumption.
The new USB-WaveCatcher board has been designed to provide high performances over a short time window. It houses on a small surface two 12-bit 500-MHz-bandwidth digitizers sampling between 400 MS/s and 3.2 GS/s. It is based on the patented SAM chip, an analog circular memory of 256 cells per channel designed in a cheap pure CMOS 0.35µm technology and consuming only 300 mW. The board also offers a lot of functionalities. It houses a USB 12 Mbits/s interface permitting a dual-channel readout speed of 500 events/s. Power consumption is only 2.5 W which permits powering with the sole USB.
In an embodiment of the board optimized for time measurement, a reproducible time precision of a few ps has been demonstrated.

The USB-WaveCatcher can thus replace oscilloscopes for a much lower cost in most high-precision short-window applications. Moreover, it opens new doors into the domain of very high precision time measurements.

Summary:

The currently existing electronics dedicated to precise time measurement is mainly based on the use of constant fraction discriminators (CFD) associated with Time to Digital Converters (TDC). The constant fraction technique minimizes the time walk effect (dependency of timing on the pulse amplitude). Several attempts have been made to integrate CFD in multi-channel ASICs. But the time resolution measured on the most advanced one is of the order of 30 ps rms.
Two main techniques are used for the TDC architectures. The first one makes use of a voltage ramp started or stopped by the digital pulse. The obtained voltage is converted into digital data using an Analog to Digital Converter (ADC). The timing resolution of such a system is excellent (5 ps rms). But this technique is limited by its large dead time which can be unacceptable for the future high rate experiments. Another popular technique associates a coarse measurement performed by a digital counter with a fine measurement (interpolation) using Delay Line Loop. Such a system can integrate several (8-16) channels on an FPGA or an ASIC. The most advanced DLL-based TDC ASIC exhibits a timing resolution of 25 ps, but only after a careful calibration.
It should be noticed that the overall timing resolution is given by the quadratic sum of the discriminator and of the TDC.
In the meantime, alternative methods based on digital treatment of the analogue sampled then digitized detector signal have been developed. Such methods permit achieving a timing resolution far better than the sampling frequency. For example, 100ps rms resolution has been reported for a signal sampled at only 100MHz.
Digitization systems have followed the progress of commercial ADCs, which currently offer a rate of 500 MHz over 12 bits. Their main drawbacks are the huge output data rate and power consumption. Their packaging, cooling, and tricky clock requirements also makes them very hard to implement. Conversely, high speed analog memories now offer sampling rates far above 1GHz at low cost and with low power consumption.
The new USB-WaveCatcher board has been designed to provide high performances over a short time window. It houses on a small surface two 12-bit 500-MHz-bandwidth digitizers sampling between 400 MS/s and 3.2 GS/s. It is based on the patented SAM chip, an analog circular memory of 256 cells per channel. Its innovative matrix design permits reaching these performances, yet in a cheap pure CMOS 0.35µm technology, while consuming only 300 mW.
Raw sampling precision is as good as 15ps rms. In an embodiment where the clock is directly sent to the SAM chip, thus limiting the usable sampling frequency to 3.2GHz, and after a calibration of the fixed pattern time distribution, a reproducible time precision of a few ps has been demonstrated.
The board also offers various functionalities. Its input offset is tunable over a range of 2 V. It can be triggered either internally or externally and several boards can easily be synchronized. Trigger rates counters are implemented. Both channels can also be used for reflectometry thanks to their internal pulser. The precision obtained for cable length measurements is as good as 2mm. Charge measurement mode is also provided, through integrating on the fly over a programmable time window the signal coming for instance from photo-multipliers. Power consumption is only 2.5 W which permits powering with the sole USB. Signal connectors can be BNC, SMA or LEMO.
The board houses a USB 12 Mbits/s interface permitting a dual-channel readout speed of 500 events/s. Faster readout modes are also available. In charge measurement mode, the sustained trigger rate can reach a few tens kHz. A 480Mbits/s version will soon be available.
Various evolutions of the SAM chip are under study, targeting either higher precision time measurements or longer time window.
The USB-WaveCatcher can thus replace oscilloscopes for a much lower cost in most high-precision

short-window applications. Moreover, it opens new doors into the domain of very high precision time measurements.

POSTERS SESSION / 131

A Prototype Front-End Readout Chip for Silicon Microstrip Detectors Using an Advanced SiGe Technology

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The upgrade of the ATLAS detector for the high luminosity upgrade of the LHC will require a rebuild of the Inner Detector as well as replacement of the readout electronics of the Liquid Argon Calorimeter and other detector components. We proposed some time ago to study silicon germanium (SiGe) BiCMOS technologies as a possible choice for the required silicon microstrip and calorimeter front-end chips given that they showed promise to provide necessary low noise at low power. Evaluation of the radiation hardness of these technologies has been under study. To validate the expected performance of these technologies, we designed and fabricated an 8-channel front-end readout chip for a silicon microstrip detector using the IBM 8WL technology, a likely choice for the ATLAS upgrade. Preliminary electrical characteristics of this chip will be presented.

Summary:

The expected upgrade of the Large Hadron Collider (LHC) to increase luminosity by as much as an order of magnitude will require a major upgrade of the ATLAS detector. Included in the upgrade will be a rebuild of the entire inner detector, replacement of the readout electronics of the Liquid Argon Calorimeter (LAr) as well as many other detector components. The proposed new Inner Detector will include silicon microstrip detectors. The silicon microstrip detectors, especially those proposed to be 10 cm long, and the LAr will present relatively large capacitive loads to the front-end readout chip. These electrical characteristics along with the necessary shaping times less than 20 ns, are well suited to bipolar circuitry as proven in several past experiments including the present ATLAS SCT. The advanced germanium doped bipolar technologies are especially suited to this since they yield extremely small base resistances (of order tens of Ohms), which allow very low noise operation without excessive bias currents.

In order to validate these technologies for use in the upgraded ATLAS Detector, our group has performed radiation studies on several commercial technologies [1,2,3,4]. We have also built one prototype chip using the IHP SG25H1 25 μm technology. The IBM 8WL technology looks very promising for ATLAS upgrade work, given our radiation results and the fact that its CMOS component is compatible with the IBM 8RF technology now being used for several other prototype chips for the upgrade.

In order to confirm the electrical performance of this 8WL technology, we have designed and fabricated an 8-channel front-end readout chip. It consists of pre-amp, shaper and comparator circuits for each channel along with LVDS output drivers such that the comparator outputs can be fed into an FPGA for testing. Any final readout chip would likely contain additional digital circuitry such as pipeline, output buffer and command decoder, which can be implemented with CMOS structures available in the 8WL technology and compatible with 8RF designs already in development.

Along with a description of the circuit and simulation results, we will present preliminary electrical characterization results showing the performance that can be achieved with this technology.

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Parallel session B1 - Systems, Installation and Commissioning / 132

The Noise Performance of the CMS Detector

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The design of the CMS power distribution system plays a major role in the ultimate noise performance of detector, both from the perspective of internally generated noise and of noise coupling between subdetectors. Noise considerations in a detector power system depend strongly on the mechanical configuration of the detector and the cabling and grounding conventions used.

This talk will review the commissioning history of CMS from the point of view of noise performance and interactions between detector subsystems. Particular emphasis is placed on the influence of the global mechanical design of CMS, as well as that of its subdetectors.

Summary:

The design of the CMS power distribution system plays a major role in the ultimate noise performance of detector, both from the perspective of internally generated noise and of noise coupling between subdetectors. Noise considerations in a detector power system depend strongly on the mechanical configuration of the detector and the cabling and grounding conventions used.

The CMS detector is mechanically complex. It is segmented into 13 longitudinal sections, of which the central section is stationary, while the others can move up to 10m in the longitudinal direction. The cables in these sections pass through flexible cable chains in trenches beneath the detector. These cable paths are typically 100m-140m long.

The power system for the on-detector electronics of the CMS Experiment comprises approximately 12000 low voltage channels, requiring a total power of 1.1 MVA. Typical current requirements at the CMS detector front end range from 1A-30A per channel at voltages ranging between 1.25V and 8V. This requires in turn that the final stage of the low voltage power supply be located within ~10m of the front-end electronics, that is, on the detector periphery.

In addition, the detector periphery holds crates containing first-level data acquisition and trigger electronics, many of which are laterally interconnected by control and readout buses.

In the process of commissioning the CMS detector we have observed multiple instances of interactions between the electronics of different subsystems. We have studied the behavior of noise currents in the CMS power system in an effort to understand the noise susceptibilities of the subdetectors. We have observed
instabilities in detector electronics brought about by effects of the CMS magnetic field on cavern electrical infrastructure.

We have also observed significant high-frequency common-mode currents in the power cabling of a subset of the on-detector power supplies. These currents are present in the earthing conductors as well. Understanding the subsequent propagation of these currents through the mechanical structure of

the detector, and understanding their effect on detector electronics is essential to optimizing the noise performance of CMS.

This talk will review the commissioning history of CMS from the point of view of noise performance and interactions between detector subsystems. Particular emphasis is placed on the influence of the global mechanical design of CMS, as well as that of its subdetectors.

Parallel session B2b - Radiation tolerant components and systems / 133

Development of new readout electronics for the ATLAS LAr calorimeter at the sLHC

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The ATLAS Liquid Argon (LAr) calorimeter consists of 182,486 detector cells whose signals need to be read out, digitized and processed, in order to provide signal timing and the energy deposited in each detector element. The current readout electronics is not designed to sustain the ten times higher radiation levels expected at sLHC in the years ≥2017, and will be replaced by new electronics with a completely different readout scheme. The future on-detector electronics is planned to send out all data continuously at each bunch crossing, as opposed to the current system which only transfers data at a trigger-accept signal. Multiple high-speed and radiation-resistant optical links will transmit 100 Gbps per front-end board, each covering 128 readout channels. The off-detector processing units will not only process the data in real-time and provide digital data buffering, but will also implement trigger algorithms.
An overview about the various components necessary to develop such a complex system will be given. The current R&D activities and architectural studies of the LAr Calorimeter group will be presented, in particular the on-going design of the mixed-signal and radiation hard front-end ASICs, the Silicon-on-Saphire (SOS) based optical-link, the high-speed off-detector FPGA based processing units and the power supply distribution scheme.

Summary:

The ATLAS experiment is one of the two general purpose detectors designed to study the proton-proton collisions at the Large Hardron Collider (LHC) with a center-of-mass energy of 14 TeV and to explore the full physics potential of the LHC at CERN. A vital part of the ATLAS detector is the Liquid Argon (LAr) calorimeter which is used to measure the energy of electromagnetic and hadronic particles, and to trigger on interesting physics events. The LAr calorimeter consists of 182,486 detector cells in total. Their signals need to be read out, digitized and processed, in order to provide accurate signal timing and the energy deposited in each detector element. The current readout electronics is not designed to sustain the ten times higher radiation levels expected at sLHC in the years ≥2017, and will be replaced by new electronics with a completely different readout scheme. The different components and general architecture of the upgraded system will be presented.

The challenges for the on-detector electronics are two-fold: it must be radiation tolerant and able to transmit large amount of data at high rates. The future electronics is planned to send out all data continuously at each bunch crossing, as opposed to the current system which only transfers data at a trigger-accept signal.
For the front-end electronics, two R&D efforts are going on which are focused on the analog and mixed-signal ASIC design, respectively. For the analog part, a test structure chiplet based on 0.13 μm SiGe BiCMOS technology will be used to test radiation performance of different transistor configurations. A prototype with a low-noise pre-amplifier, CR–(RC)2 signal shaping and two gain settings is currently being designed and tested. For the mixed-signal part, a custom pipeline ADC in IBM 8RF CMOS technology is chosen and many critical techniques, such as S/H capacitor, amplifier and digital correction etc. have been studied. In summer 2009, a MOSIS test structure proposal is planned to be submitted. For the high speed digital components jitter control is being investigated. An issue is also to provide

power to the front-end modules, and radiation and magnetic field tolerant devices are developed, where experience from the current LAr system is used.

The digitized data is sent to the off-detector readout via multiple high-speed and radiation-resistant optical links. The transmission of presumably 16 bit signals from 128 channels per front-end board at 40 MHz requires a total data rate of ~100 Gbps per board. Currently, radiation tolerant multi-fibre ribbons are tested. The optical transceiver is planned to be in 0.25 μm UltraCMOS Silicon on Sapphire (SOS) technology due to its inherent resistance to radiation. Results from a test chip as well as from a Link-on-Chip prototype will be presented.

The off-detector processing units, the readout drivers (ROD), will not only process the data in real-time and provide digital data buffering, but will also implement trigger algorithms. The data will be received by high-speed commercial optical links and FPGA based SERDES components. Data processing and digital filtering will also be realized in modern FPGAs. A challenging task is the implementation of trigger algorithms which need an interconnect between the ROD boards. The ATCA technology is chosen to provide the framework for fast serial links between the RODs. First ROD prototypes equipped with a Xilinx Virtex-5 FPGA together with an optical signal injector board currently run successfully at about 40% of the target data rate. A second ROD prototype in ATCA format is expected to be available for further tests in summer 2009.

In the presentation, an overview about the various components necessary to develop this new and complex readout system will be given. The current R&D activities and architectural studies of the LAr Calorimeter group will be presented, in particular the on-going design of the mixed-signal front-end ASICs, the SOS based optical-link, the high-speed off-detector FPGA based processing units and the power supply distribution scheme.

POSTERS SESSION / 134

Interference coupling mechanisms in Silicon Strip Detector – FEE. -CMS tracker “wings”: A leaned lesson for SLHC-

Authors: Claudio Rivetta[1]; Fernando Arteche[2]

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The identification of the coupling mechanisms between noise sources and sensitive areas of the front-end electronics (FEE) in the previous CMS tracker sub-system is critical to optimize the design of integrated circuits and hybrids for the proposed SLHC Silicon Strip Tracker systems. This paper presents a validated model of the noise sensitivity of the Silicon Strip Detector-FEE of the CMS tracker to quantify the impact of the noise coupling mechanisms in the system immunity against electromagnetic interferences. This model has been validated based on simulations using finite element models and immunity tests conducted on prototypes of the Silicon Tracker End-Caps (TEC) and Outer Barrel (TOB) systems. The results of these studies show important recommendations and criteria to be applied in the design of future hybrids and modules to increase the immunity against electromagnetic noise.

Summary:

Electromagnetic interference (EMI) has been one of the major concerns during the integration of the last generation of the Silicon Strip Tracker. Grounding and shielding problems and electromagnetic compatibility (EMC) issues arisen during the integration of the tracker sub-system have required time and important series of tests and studies to solve them. Efforts to find both the root cause and the solution of these problems have allowed learning important lessons that have to be included in the design of the integrated circuits, hybrids and system integration of the up-dated silicon tracker systems.
In general, most of the EMC problems associated with the CMS Tracker sub-systems were associated with interference generated by the power supplies and auxiliary equipment and coupled to the silicon detector through the distribution boards within the tracker area. Interference and noise currents flowing through both the power and auxiliary equipment cables penetrates into the tracker detector and

propagates in that area following the distribution cables and boards. Within the detector area, these interference currents couple noise to the sensitive spots of the FEE, reducing its signal-to-noise ratio. This coupling mechanism is mainly via conduction and near field.
A new power distribution scheme based on DC-DC switching power converters is under study to overcome the problem of ultra-low voltage required by the new electronics and the conductor mass that is possible to allocate in the central part of the detector. It defines a noticeable and important noise source very close to the detector's FEE. Although a big effort is put to reduce the primary noise emission in the distributed DC-DC switching converters based powering scheme proposed for the CMS tracker upgrade, the emitted noise levels achieved have to be directly compatible with the noise immunity levels of the new silicon detectors and associated FEE. This immunity is basically defined by the intrinsic FEE topology, the silicon strip detector-FEE connection and the integration of the unit at system level. The experience gained with the previous tracker FEE has to be seriously considered to improve future designs. For that purpose, the evaluation of the electromagnetic immunity of previous generation of silicon tracker detector- FEEs is critical to optimize and improve the performance of the future generation of detectors.
This paper presents a validated model of the noise sensitivity of the Silicon Strip Detector-FEE of the CMS tracker to quantify the impact of the noise coupling mechanisms in the immunity against electromagnetic interference. Furthermore, based on that model, it defines both strategies to improve the EMI immunity and limitations to be applied in future designs. The coupling phenomena of electromagnetic interferences with the Silicon Strip Detector-FEE has been both evaluated via simulation using finite element models and measured on prototypes. Those measurements are based on several immunity tests conducted in final prototypes of the Silicon Tracker End-Caps (TEC) and Tracker Outer Barrel (TOB) systems, to estimate the sensitivity of each system to conducted noise.
The understanding of the coupling mechanism of electromagnetic interferences to the Silicon Strip Detector-FEE and the model of the noise sensitivity have been used to identify critical elements and inappropriate layouts in the prototypes that were responsible for the degradation of the signal-to-noise of the FEE during the commissioning. Today this understanding is critical to define design recommendations and specify the electronics and system topology to increase the FEE robustness to EMI in anticipation of the challenging power distribution schemes proposed for the SLHC tracker upgrades.

POSTERS SESSION / 135

Study Radiation Hardness Performance of PiN diodes for the ATLAS Pixel Detector at SLHC

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We study the radiation hardness of PiN diodes which are part of the optical link. These components were irradiated by 200 MeV protons up to 8.2 x 10exp(15) 1-MeV neq/cm2 (84 MRad). The responsivity of PiN diodes are measured as a function of the radiation dose to estimate life time reliability of diodes.

Summary:

We discuss the radiation tolerance of the silicon and GaAs PiN diodes that will be part of the readout system of the ATLAS upgraded pixel detector. The components were irradiated by 200 MeV protons up to 1.2 x 10exp(15)p/cm2for 2.6 x 10exp(15)p/cm2 for 24 GeVprotons. We study the radiation hardness of PiNs as a function of the optical sensitive area and of their cut off frequency. The dark current of PiN diode candidates is measured before and after irradiation, and the response of the PiN diodes was monitored online and some of them off-line as a function of the radiation dose.

POSTERS SESSION / 136

DC-DC switching converter based power distribution vs Serial power distribution: EMC strategies for SLHC tracker up-grade

Authors: Claudio Rivetta[1]; Fernando Arteche[2]

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This paper presents a detailed and comparative analysis from the electromagnetic compatibility point of view of the proposed power distributions for the SLHC tracker up-grade. The main idea is to identify and quantify the noise sources, noise distribution at the system level and the sensitive areas in the front-end electronics corresponding to both proposed topologies: The DC-DC converter based power distribution and the serial power distribution. These studies will be used to define critical points on both systems to be studied and prototyped to ensure the correct integration of the system taking critically into account the electromagnetic compatibility. This analysis at the system level is crucial to ensure the final performance of the detector using non conventional power distributions and to avoid interference problems and excessive losses that can lead to failures or expensive unpractical solutions.

Summary:

The up-grade for the tracker sub-system in both CMS and Atlas detectors are based in a front-end electronic (FEE) circuitry that requires ultra-low voltages to power-up the integrated circuits. This constraint forces to define new schemes of DC power distribution to bias efficiently the tracker front-end electronics, reducing the volume of the power conductors. The proposed power distribution schemes can be grouped into: Serial Power Distribution System and DC-DC switching converter based Power Distribution System. Both schemes are not conventional and have advantages and disadvantages.
The high magnetic field in the central detector forces to use DC-DC power converters without magnetic material as kernel for the DC-DC switching converter based Power Distribution System. A large R&D effort is planned to develop unique DC-DC switching converters to operate under high magnetic field and particle radiation with minimum radiated and conducted noise emissions. The constraint imposed by the no-magnetic material design sets the conductive and radiated noise levels to a minimum that is higher than that achieved in conventional switching converters. Additionally, in this power distribution scheme, DC-DC converters will be located near the FEE, within the tracker volume, increasing the coupling for interference between the power converter and the detector and its front-end electronics.
Serial power distribution system has been already used in other small subsystems and experiments. This topology is mainly characterized by floating the Detector-FEE. This requirement forces special design to keep balanced the high frequency connections to ground. For that purpose special effort should be focused on the integral design of the FEE, detector and distribution systems to minimize the effect of parasitic elements that have critical impact in the system performance. Additionally, in order to increase the efficiency, the serial power distribution plans to use as a primary power supply DC-DC converters that may increase the total interference of the system due to the conducted output noise emitted.
Those scenarios force to conduct electromagnetic compatibility studies on the proposed systems to be able to improve the noise immunity of the front-end electronics to assess compatibility with the noise generated by the power supply system. CMS tracker power task force has recommended that the baseline powering system for an upgraded CMS Tracking system should be based on distributed DC-DC power conversion, with Serial Powering as a back-up solution, whereas ATLAS upgrade has no decision yet. In any case, electromagnetic compatibility between components in both the DC-DC switching converters based Power Distribution and the Serial Power Distribution topologies can be only achieved minimizing both the radiated and conducted noise emitted by the main noise sources and increasing the immunity to noise of the FEE by a robust design.
This paper analyses the main elements that defines the electromagnetic compatibility of both power distribution systems and defines the impact of the system design and integration strategies in the compatibility of FEE. The main aspects (noise sources and FEE immunity) that define the electromagnetic compatibility of both topologies are presented. The integration aspects have strong impact in the system compatibility. However, if an EMC strategy is implemented at an early stage of the design, the compatibility between both FEE and proposed DC power distributions may be achieved.

POSTERS SESSION / 138

Upgrade of the BOC for the ATLAS Pixel Insert-able B-Layer

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The first upgrade for the ATLAS pixel detector will be an additional layer, which is called IBL (Insert-able B-Layer). To readout this new layer having new electronics assembled an update of the readout electronics is necessary. The aim is to develop a system which is capable to read out at a higher bandwidth and also compatible with the existing system to be integrated into it. The talk will describe the necessary development to reach a new readout system, concentrating on the requirements of a newly designed Back of Crate card as the optical interface in the counting room.

Summary:

The innermost layer of the ATLAS Pixel detector, the B-Layer, will suffer a lot of irradiation damage and therefore will not be operational for the full lifetime of 10 years of ATLAS. To provide a good tracking performance over the full lifetime a replacement or an addition of a pixel tracking layer is to be done. Since the shutdown time for such an operation is rather short, the only possible solution of this is to insert a new additional layer in the phase 1 upgrade pause, around 2013/2014. This additional layer, called IBL (Insert-able B-Layer), will include newly designed on-detector electronics to cover the higher radiation and occupancy. It needs to be read out using an adopted or renewed readout system, which is under development.
Since the distance to the interaction point is reduced the occupancy of the FE chips is higher and the readout bandwidth needs to be adapted to that. A change in the pixel size is reducing this effect so that an increase in readout bandwidth by a factor 2 is sufficient.
The adaption of the readout bandwidth must be done on off-detector side within the Back of Crate card (BOC). Therefore, the Back of Crate card needs a redesign of the data receiving part. It will be the off-detector end of the optical link, which transmits data in both directions. From the BOC card the command and control data is sent to the optoboard (the opto-electrical interface inside the detector volume) and from there electrically to the modules. Vice versa, the modules data is sent electrically to the optoboard and from there optically to the BOC card. While the transmission to the detector will be operated at 40 Mb/s, the readout from the detector will be done at 160 Mb/s bandwidth.
This higher readout speed has several implications, which need to be fulfilled like getting the correct clocks to the different parts of the detector. Also under investigation is a DC balanced signal to transmit the data from the detector. This would enable an automated phase adjustment of the detector data to the readout system clocks.
Under the baseline to be compatible with the remaining parts of the readout system an R&D project is started to study the opportunities of these new BOC card. The constrains and requirements for this card are discussed as well as first results of this investigation.

POSTERS SESSION / 139

Development and commissioning of the ALICE pixel detector control system

Author: Claudio Bortolin[1]

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The Silicon Pixel Detector (SPD) is the section of the ALICE Inner
Tracking System closest to the interaction point. In order to operate the detector in a safe way, a control system was developed in the framework of PVSS which allows monitoring a large number of parameters such as temperatures, currents, etc.
The control system of the SPD implements interlock features to protect the detector against overheating and prevents operating it in case of malfunctions. The nearly 50000 parameters required to fully configure the detector are stored in a database which implements an automatic version of the configuration file after a new calibration run has been carried out. Several user interface panels were developed to allow also non-expert shifters to operate the detector easily and safely.
This contribution provides a detailed description of the features and commissioning of the SPD control system.

Summary:

The ALICE Silicon Pixel Detector (SPD) corresponds to the two innermost layers of the ALICE central tracking system and it is the closest detector to the interaction point. The SPD is made of hybrid silicon pixels and contains 9.8 M read-out channels. It is composed of 120 half staves (HS) mounted on 10 carbon fibre supporting sectors. Each half stave is made of two ladders, a Multi Chip Module and an aluminium-polyimide multilayer bus. Each ladder consists of 5 front-end chips bump bonded to a 200 microns thick silicon sensor. The MCM constitutes the on-detector electronics and performs operations such as triggering, clock distributions, data multiplexing, etc. The multilayer bus provides the communication between the MCM and the front-end chips. The communication between the MCM and the off-detector electronics (Routers) is assured by three single-mode optical fiber links.
The SPD low voltage power supply system is based on 20 CAEN A3009 dc-dc converter modules housed in 4 CAEN Easy3000 crates located at about 40m from the detector. The sensor bias voltage is provided by CAEN A1519 modules housed in a CAEN SY1527 mainframe 100 m away from the detector. The SY1527 mainframe is the top level of the system that communicates via Ethernet (TCP/IP, OPC protocol) with the software layer of the Detector Control System (DCS)
The DCS plays a very important role in operating the SPD and fulfils very stringent requirements. In particular, it protects the detector against overheating that may occur in case of failures in the evaporative cooling system or malfunctioning in the system components. The ALICE Detector Control System, as well as all the LHC experiments, is supervised by a SCADA system (Supervisory Control and Data Acquisition) based on a software platform called PVSSII.
The aim of every control system is to supervise all the operations carried out in its structure and to react promptly in case of misbehaviours. The ALICE Control Coordination (ACC) team in collaboration with every detector foresaw a series of constrains to integrate the control system of each sub-detector into a unique ALICE detector control system. The detector control system (DCS) of the SPD was designed according to such requirements. Standard components were mainly used to reduce maintenance efforts and, in few cases, dedicated components were developed for specific and innovative tasks. The DCS of the SPD has been developed to fully operate the detector and its system components, including the configuration of the front-end electronics.
PVSSII provides the link between the hardware components and the control logic units which are supervised by the Finite State Machine (FSM). The latter connects the defined logical states of the detector components and sends macroinstructions (i.e.: Go Off, Go Ready, etc) via PVSS: a macroinstruction is a sequence of operations addressed to the hardware. The correct sequence of actions is checked and possible errors are detected. The FSM has also the task of providing the Alice DCS with information regarding the status of the SPD (i.e.: Ready for data-taking, calibrating, etc.).
PVSS is designed for slow control applications and it is not suitable for direct control of fast front-end electronics. More than 50000 parameters (DAC) are required to configure the SPD front-end electronics. For this reason a dedicated Front-End Device (FED) driver was build to interface the PVSS layer with the SPD electronics. The FED receives macroinstructions and autonomously operates the front-end/off-detector electronics. A direct connection reads and saves all the required parameters in the configuration Oracle database (CDB).
The DCS of SPD is a distributed system composed of 4 PVSSII sub-projects which run in 4 PCs (3 working nodes and 1 operator node). The working nodes, accessible only to expert users, are the computers used to control the detector. The User Interface (UI) is installed in the operator node where all users can login.
The UI is the graphic interface tool that allows users to monitor and manage the detector in a safe way. This contribution will provide an overview of the DCS of the SPD, with particular emphasis on the functionalities that improved the system automation level. The solution adopted to connect PVSSII to the configuration database will also be presented.
The SPD detector control system is installed and used for the detector commissioning and operation. The DCS performances will also be discussed.

Plenary Session 6 - Programmable Logic, Boards, Crates and Systems / 140

Recent Advances in Architectures and Tools for Complex FPGA-based Systems (Invited Talk)

Emerging FPGA architectures include large amounts of programmable logic and interconnect, dedicated memory, and digital signal processing slices, along with high-speed serial and parallel I/0, embedded microprocessors, integrated communication blocks, and advanced clocking capabilities. These emerging FPGA architectures and new FPGA development tools, which enable designs to be developed at a high level of abstraction, are enabling the design of very complex digital systems.

In this talk, I will provide an overview of emerging FPGA architectures and describe some recently developed tools that facilitate the rapid design, integration, and testing of complex FPGA-based systems. I will also discuss how some of these FPGA architectures and tools are being utilized to facilitate the design and testing of advanced FPGA-based systems for particle physics.

Summary:

Biography:
Michael Schulte is an Associate Professor of Computer Engineering at the University of Wisconsin-Madison, where he directs the Madison Embedded Systems and Architectures (MESA) Lab. He received a B.S. degree in Electrical Engineering from the University of Wisconsin-Madison, and M. S. and Ph.D. degrees in Electrical Engineering from the University of Texas at Austin. He has served as the Program Chair and General Chair for several internal conferences, and as an Associate Editor for the IEEE Transactions on Computers and the Journal of VLSI Signal Processing Systems.

Michael's research and teaching interests include FPGA-based embedded systems, domain-specific processors, computer architecture, computer arithmetic, and digital system design. He currently leads an NSF-supported project on "Design and Integration of Complex Digital Systems for High Energy Physics," which seeks to develop novel techniques and tools to enable geographically-distributed, multi-disciplinary teams of scientists and engineers to design, integrate, and test complex FPGA-based systems for upgrades to the Large Hadron Collider at CERN.

POSTERS SESSION / 141

The Online Error Control and Handling of the ALICE Pixel Detector

Author: Michele Caselle[1]

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The SPD forms the two innermost layers of the ALICE experiment. It is equipped with a total of 120 modules (half-staves) with a total number of 9.8 x 106 readout channels. Each half-stave is connected via three optical links to the off-detector electronics made of FPGA based VME readout cards (Routers). The Routers and their mezzanine cards provide the zero-suppression, data formatting and multiplexing and the link to the DAQ system. This paper presents the hardware and software tools developed to detect and process errors occurring at the level of the Router originating from either front-end electronics, DAQ or the off-detector electronics. The error handling system then automatically transmits this information to the detector control system and to dedicated MySQL database for further analysis.

Summary:

The ALICE SPD consists of two barrel layers at average radii of 3.9 and 7.6 cm, respectively. The SPD is made of 120 half-staves with a total of about 107 readout channels. Each half-stave is made of two sensors flip chip bonded to five front-end chips each, one Multi-Chip Module (MCM) and an Al/kapton multilayer bus to connect each front-end chip with the MCM. The MCM is connected with the off-detector electronics via three 800Mbit/s bidirectional optical links.
The off-detector electronics consists of 20 VME based readout cards (Routers), each holding three mezzanine cards (LRx) for zero-suppression and data formatting. Each LRx card connects to two half-staves in the detector. The Router card performs the data multiplexing and interfaces to the ALICE Central Trigger Processor (CTP) and Data Acquisition (DAQ) to transmit the data stream.
The hardware tools for error detection consist of two different units implemented in VERILOG modules that were added to the standard off-detector components in the Routers managing the data taking. All error information is processed at 40 MHz. The first unit identifies the error typologies coming from different parts of the SPD system, e.g.: optical connection status and data format errors, front-end and back-end errors/status, SEE (Single Event Effect), wrong trigger sequences or missing/spurious trigger signals, etc. The second unit is a set of VERILOG modules that manage and transmit the error information to the SPD Front-End-Device server (FED). The maximum number of potential error topologies in the full SPD amounts to 3200, which can be processed at 40 MHz. Usually one error condition generates a cascade of secondary errors that then will also be registered by the error detection hardware units. The hardware units are capable to distinguish between the original error and secondary effects and will flag the cause of the problem.
The Software components consist of one low and one high tier. The low tier is driver written in C++ included in the FED. It establishes the communication with the hardware units in the Routers and transmits the error information to the dedicated MySQL Database. In parallel the error information from the FED is sent to the Detector Control System (DCS) to make aware the operator.
A statistical errors analysis (histograms, cross-correlations, etc.) of the different error types can be done using the MySQL database to evaluate the main error sources in the SPD hardware. This will allow monitoring the SPD stability over the lifetime in the ALICE experiment.
The error detection system has been thoroughly tested in the integration lab using final system components and was then implemented in the SPD system in the ALICE experiment. This paper presents the hardware and software tools developed in order to recognize and process errors in the SPD front-end and off-detector electronics. The first operation experience in the experiment are also reported.

TUTORIAL - FPGA Tools and Techniques for High Performance Digital Systems (1) / 142

FPGA Tools and Techniques for High Performance Digital Systems (Tutorial)

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This two-part tutorial will introduce the audience to FPGA tools and techniques that provide the ability to efficiently design, integrate, and test high performance digital systems. The first half of the tutorial will cover hardware design techniques and tools currently available from industry such as Xilinx ISE Foundation, PlanAhead Design Analysis, and ChipScope. The second half of the tutorial will cover advanced techniques and tools for complex digital system design, testing, and integration such as the Dataflow Interchange Format (DIF), the DSPCAD Integrative Command Line Environment (DICE), and Subversion (SVN) repositories.
Tutorial participants will be introduced to tools and techniques for FPGA-based design, see examples of efficient HDL coding, testing, and integration practices, gain experience with using the tools, and. obtain an understanding of FPGA tool capabilities and challenges Although the focus of the tutorial will be on FPGA-based systems, many of the tools and techniques presented can also be used to design, test, and integrate ASICs, embedded software, and other types of digital system. No previous experience with FPGA design is required.

POSTERS SESSION / 144

Electronic development for the upgrade of the LHCb Vertex detector.

Author: Jan Buytaert[1]

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The LHCb experiment plans to upgrade the entire detector and increase its running luminosity by a factor 10, by 2015/2016. This will require a full scale replacement of the front end electronics, to enable all detector information to be read out at 40 MHz and combined in the first level trigger executed on a PC-farm. In addition, the parts of the detector which suffer from radiation damage or excessive occupancy at high luminosity will be upgraded appropriately. One very important component of the upgrade is the replacement of the silicon vertex detector, possibly to a pixelated device. R&D is underway to exploit the Timepix pixel detector recently developed by the Medipix2 collaboration. This chip, in combination with a pixelated silicon detector is very suitable for such a high energy physics application. The small pixel size of 55 x 55 micron together with the time over threshold charge measurement is expected to give very precise spatial resolution which is well matched to the requirements of LHCb. Some adaptions to the chip design are required to match the 40MHz readout rate and move from 250 nm technology to smaller feature sizes.

The deep submicron technology has good potential to survive the radiation environment of up to 400 MRad, and future developments in 130 or 90 nm technology will provide increased radiation resistance and reduced power, which will be advantageous for the detector design. The potential to hybridise the design with the use of through silicon vias further enhances the efficiency and material budget of the detector. This talk will report on the planned developments, and on a number of testbeams scheduled for summer 2009 to establish the proof of principle of the use of Timepix for the high energy physics environment. Further electronics developments for the LHCb upgrade, such as alternative electronics chips, the planned use of FPGAs and the further extension of the Timepix for possible use in the RICH photon detector readouts will also be touched on.

Summary:

The recently developed Timepix chip, from the family of Medipix chips, is a candidate for use as the front end chip for a silicon pixel vertex detector for the upgraded LHCb experiment. This talk will focus on the design modifications necessary for its use in the LHCb environment, as well as the proof of principle tests of the chip in combination with a pixelated silicon detector as a sensing device for minimum ionising particles in testbeams in summer 2009. The developments will be put in context with an overview of the general electronics developments for the LHCb upgrade.

Parallel session A1 - ASICs / 145

Low noise, low power front end electronics for pixelized TFA sensors

Author: Karolina Poltorak[1]

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In this paper we present the preliminary experimental results obtained with 10 μm thick hydrogenated amorphous silicon sensors, deposited directly on top of integrated circuit optimized for tracking applications at linear collider experiments. The signal charges delivered by such a-Si:H n-i-p diode are small; about 37 e-/μm for a minimum ionizing particle, therefore a low noise, high gain and very low power front-end circuitry is of primary importance. The developed demonstrator chip comprises an array of 64 by 64 pixels laid out in 40 μm by 40 μm pitch designed in 250 nm CMOS technology.

Summary:

Thin Film on ASIC (TFA) technology combines advantages of Monolithic Active Pixel and Hybrid Pixel technologies thanks to the direct deposition of a hydrogenated amorphous silicon (a-Si:H) sensor film on top of the readout circuit. The sensor film comprises 3 layers; a n doped thin layer of a-Si:H in electrical contact to the electrodes of the readout chip, a thick layer of an intrinsic a-Si:H, and a top p-doped a-Si:H thin layer. The intrinsic a-Si:H layer is depleted by applying an electric field of about 5 to 10 V/μm. Compared to the Monolithic Active Pixel imagers, the TFA technology allows using more sophisticated front-end circuitry to extract the signal. In addition, compared to the Hybrid Pixel imagers, the TFA technology does not require bump bonding, which imposes limitations on sensor segmentation, cost and material budget. This technology approach is especially attractive for high sensitivity imagers sensing very low levels of light, low energy electrons and 1-50 keV X-rays. In this paper we present the preliminary experimental results obtained with 10 μm thick hydrogenated amorphous silicon sensors, deposited directly on top of integrated circuit optimized for tracking applications at linear collider experiments. The signal charges delivered by a-Si sensors are small, about 400 e- for a minimum ionizing particle in 10 μm thick sensor layer. For that reason design of a low noise, high gain and very low power front-end circuitry is essential.
The circuit is based on a charge sensitive preamplifier built around an un-buffered cascode stage with 1.3fF feedback capacitor Cf, which provides sufficiently high gain in a single amplifier stage. The dimensions of the input PMOS transistor are 6μm/0.28μm, so that contribution of the gate capacitance (cg = 7fF) to the total input capacitance (cin = 40fF) is reasonably small. During the reset phase the feedback capacitance is discharged through a feedback transistor biased with a constant current instead of a voltage controlled reset transistor, which is a commonly used solution. Investigation of a new solution is stimulated by limitation of the schema with voltage controlled reset transistor due to intolerable parasitic injection from the reset signal to the very small feedback capacitor. From this point of view a small reset currents will be favorable. On the other hand one has to keep in mind that the preamplifier stage working in soft reset regime operates as a transimpedance amplifier with parallel noise sources originated from the feedback transistor.
The integrated signals are stored subsequently on sample and hold buffer and sent out during the readout frame via analogue multiplexer. The device contains an array of 64 by 64 pixels laid out with 40 μm by 40 μm pitch. Total power dissipation is around 10μW per pixel. The developed demonstrator chip was designed in 250 nm CMOS technology. In the paper we will present detailed analysis of noise in the reset and the readout phase, optimization of the design as well as test results for the prototype chip.

POSTERS SESSION / 146

Total dose effects on a deep-submicron SOI technology for Monolithic Pixel Sensor development

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A monolithic pixel detector in deep-submicron Silicon On Insulator (SOI) technology has been developed and characterized. This summary presents the first assessments of the effect of ionizing radiation as regards the total dose damage on single transistors in the technology used for the development of the first prototype chip. This work shows the decisive effect of the substrate bias condition during irradiation on the radiation induced damage on the electronics.

Summary:

SOI technology allows the fabrication of CMOS integrated circuits on a thin Silicon layer, electrically isolated from the rest of the silicon wafer by means of a thick oxide layer. The isolation of the electronics from a high-resistivity substrate, used as sensitive volume, allows the production of monolithic pixel sensors for particle tracking and imaging. Vias etched through the oxide contact the substrate from the electronics layer, so that pixel implants can be created and a reverse bias can be applied.
A prototype chip, named LDRD-SOI-1, has been obtained in 2007 in a 0.15μm Fully Depleted (FD) SOI technology. In the chip, some single transistor test structures are implemented, including both I/O and core transistors (n-type and p-type).
The thick buried oxide (200nm) is expected to be sensitive to ionizing doses, which lead to positive charge trapping and consequently to an increase of the top-gate leakage current. This effect is even larger for the kind of structures we are studying. In fact, when a depletion voltage is applied to the detector, a strong electrical field is present inside the BOX. When exposed to ionizing radiation, electron-hole pairs are created inside the thick oxide. Due to the presence of the electrical field, these charges are immediately separated and do not recombine. This greatly increases the amount positive charge which is trapped throughout the BOX. The total dose damage is hence expected to be strongly dependent on the substrate voltage.
The test structures were characterized as regards their tolerance to total dose effects, by measuring the Ids-Vgs curves of each transistor before and after irradiation with X-ray photons. The irradiations were performed with the transistors in the worst-case bias conditions. A first chip was irradiated with a dose of 15krad (SiO2), in one single step. The substrate bias was Vsub = 40V, to maximize the number of electron-hole pairs escaping recombination. A second chip was irradiated up to a dose of 54krad(SiO2) with the same transistors bias conditions, but applying a Vsub = 10V (a typical operative value for the substrate bias of the pixel detector).
On the same dose given to the transistor, the two bias voltages induce two different damages: while the irradiation with Vsub =10V increments the leakage current less than one order of magnitude, the same dose given with Vsub =40V during irradiation induces an increase of the leakage current of a factor 104. The positive charge trapped inside the buried oxide in the first irradiation (Vsub = 40V) is sufficient to invert the back-channel interface, which forms a conducting path between the source and the drain and leads to a huge increase of the leakage current (the transistor is “ON” state even without any voltage applied to the gate).
Further investigation on the substrate bias conditions are planned for a 0.20μm FD SOI technology of the same producer, which was used for the development of the second prototype chip (LDRD-SOI-2). Also the effects of different dose rates will be addressed to.

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AFTER, the Front-End ASIC of the T2K Time Projection Chambers

Author: Eric Delagnes[1]

Co-authors: Alain Le Coguie [1]; Denis Calvet [1]; Estelle Montmarthe [1]; Frederic Druillole [1]; Pascal Baron [1]; Xavier De la Broise [1]

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The T2K (Tokai-to-Kamioka) experiment is a long baseline neutrino oscillation experiment in Japan, for which a near detector complex (ND280), used to characterize the beam, will be built 280m from the target in the off-axis direction of the neutrino beam produced using the 50 GeV proton synchrotron of J-PARC (Japan Proton Accelerator Research Complex). The central part of the ND280 is a detector including 3 large Time Projection Chambers based on Micromegas gas amplification technology with anodes pixelated into about 125,000 pads and requiring therefore compact and low power readout electronics. A 72-channel front-end Application Specific Integrated Circuit has been developed to read these TPCs. Each channel includes a low noise charge preamplifier, a pole zero compensation stage, a second order Sallen-Key low pass filter and a 511-cell Switched Capacitor Array. This electronics offers a large flexibility in sampling frequency (50 MHz max.), shaping time (16 values from 100 ns to 2 μs), gain (4 ranges from 120 fC to 600 fC), while taking advantage of the low physics events rate of 0.3 Hz. 6000 AFTER ASICs, have been manufactured in 2008 using a low-cost 0.35 μm CMOS technology,. They are currently being integrated on the TPCs for a start of commissioning at the end of the year 2009 in Japan.

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Welcome 2

TOPICAL / 150

Two-Phase Cooling of Targets and Electronics for Particle Physics Experiments

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An overview of the author's decade of experience with two-phase cooling research for computer chips and power electronics will be described with its possible beneficial application to high energy physics experiments. Flow boiling in multi-microchannel cooling elements in silicon (or aluminium) have the potential to provide high cooling rates (up to as high as 350 W/cm2), stable and uniform temperatures of targets and electronics, and light-weight construction while also minimizing the fluid inventory. An overview of two-phase flow and boiling research in single microchannels and multi-microchannel test elements will be presented together with videos of these flows. The objective is to stimulate discussion on the use of two-phase cooling in these demanding applications, including the use of CO2.

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Low Power SoC Design

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The design of Systems-on-Chip (SoC) in very deep submicron technologies becomes a very complex task that has to bridge very high level system description to low level consideration due to technology defaults and variations. This talk will describe some of these low level main issues, such as dynamic and static power consumption, temperature, technology variations, interconnect, DFM, reliability and yield, and their impact on high-level design, such as the design of multi-Vdd, fault-tolerant, redundant or adaptive chip architectures. Low power SoC designed by CSEM will be presented for applications in three domains: wireless sensor networks, vision sensors and mobile TV.

Plenary Session 1 - Beam Condition Monitors and Machine-Experiment Interlocks / 152

Experiment protection at the LHC and damage limits in LHC(b) silicon detectors

Author: Massimiliano Ferro-Luzzi[1]

[1] *CERN*

A review is given of possible beam failure modes at the LHC and of the strategy adopted in the LHC experiments to protect the detectors against such events.
Damage limits for the detectors are discussed and, in particular, some recent experimental tests concerning the LHCb silicon microstrip vertex detector are presented.

OPENING 2 / 153

HEP experiments in Japan : The Next Generation

Author: Ryosuke Itoh[1]

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The HEP experiment in Japan is now stepping into the next phase. The J-PARC, which is a newly-built high intensity proton synchrotron facility, started the operation recently. A new long-baseline neutrino experiment T2K is now at the commisioning stage utilizing the beam. In parallel, the upgrade of the KEKB/Belle, the new-stage B-factory experiment at KEK, is about to start. The accelerator will be upgraded to SuperKEKB whose luminosity is expected to be more than 50 time higher. The detector is also upgraded to Belle II to keep up with the increased rate. In this talk, a detailed review is given for these new experiments with some coverage of the readout and DAQ technologies.

Plenary Session 5 - Key technologies for present and future optical networks / 154

Key technologies for present and future optical networks

Author: Jean-Christophe Antona[1]

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In less than forty years, optical fiber has become omnipresent to convey high volumes of information over long distances for any segment of transport network.
Short reach access networks are now boosted by the advent of 10Gigabit Ethernet standards, Fiber-To-The-Home and Passive Optical Networks technologies.
Longer reach (from a few hundreds up to a few thousands of kilometers), terrestrial metropolitan and backbone networks have become translucent, based on the ability of lightpaths to traverse some Wavelength-Selective-Switch-based nodes without optoelectronic processing while being redirected depending on their wavelength; besides, those wavelength-multiplexed networks are about to become dynamically reconfigurable and very soon to transport capacities as high as 10 Terabit/s on a single fiber, using up to 100Gigabit/s optoelectronic transponders most likely based on Coherent Detection assisted by Digital Signal Processing.
Eventually, submarine systems are expected to propose multi-terabit/s capacities over transoceanic distances.
Such evolutions all aim at coping with the ever-increasing demand while lowering the cost and consumption of a transported bit.
This paper draws an overview of the most recent evolutions and prospects for optical networks and the key associated technologies

OPENING 2 / 155

The future of the LHC programme and machine

Author: Sergio Bertolucci[1]

[1] *CERN*

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ILC-CLIC

Author: Alex Kluge[1]

[1] *CERN*

The planned linear colliders - international linear collider (ILC) and compact linear collider (CLIC)- will provide electron-positron collisions in the TeV range. Due to the high energy of the passing electrons and positrons at the interaction point a large number of background particles not related to the collision are produced. Thus the detectors must identify and reject these background particles providing small spatial segmentation and precise particle arrival time identification. In order not to influence the particle trajectory and to provide precision measurements the amount of detector material and services need to be reduced to a minimum. Especially for CLIC, the acceleration scheme results in a bunch crossing timing structure posing a challenge to the detector and read-out electronics implementation.
In the presentation the specifications and challenges of the detector and read-out electronics for linear colliders are discussed.

Plenary Session 3 - Buses and boards, making the right choice / 157

Buses and Boards

Author: Jerry Gipper[1]

[1] *Embedify LLC*

From motherboard to backplane to blade based computer systems, the choices are numerous. This session will cover the markets and trends within those markets that are impacting decisions made by board suppliers. Discussion will focus on the various form factors, the development and evolution of industry standards, and the consortia that support and develop these standards, including VITA, PICMG, and others. The presentation will conclude with suggestions for choosing the right form factor for your application

Plenary Session 2 - Low Power Analog Design Techniques / 158

Low Power Analog Design in Scaled CMOS Technologies

Author: Andrea Baschirotto[1]

Co-authors: G. Cocciolo [2]; M. De Matteis [2]; P. Delizia [2]; S. D'Amico [2]

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[2] *University of Salento - Italy*

The running CMOS technology scaling has a big impact in the design of analog circuits. Since scaled technologies offer big advantages to digital parts (reduce space, lower power consumption, etc...), complex mixed-signal systems are typically developed in the smallest minimum-gate-length technology. However these advantages for the digital part in a scaled technology correspond to a big penalty in the analog design. Typical problems are due to the lower output impedance, to the lower available output swing and to the lower distance from VDD to VTH (VDD scales faster than VTH). Analog designers have then to develop new solutions for achieving in scaled technologies the same performance previously achieved in "older" technologies. In this talk these problems will be addressed for the cases of basic building blocks. The discussion will then move to their effects on complex systems showing the possible solutions in 90nm/65nm.

Plenary Session 4 - Low Noise Design for Large Detectors / 159

Low Noise Design for Large Detectors

Author: Marvin Johnson[1]

[1] *Fermi National Accelerator Laboratory (FNAL)*

Low common mode noise design methods for small instruments such as oscilloscopes are well known. Extending these ideas to very large systems such as detectors at the Large Hadron Collider is often not very obvious. This talk will describes methods for developing large detector designs and provide some examples of successful designs using these ideas. It will also describe some common design mistakes and how to avoid them.

Power WG / 162

SPI test results

Power WG / 163

Irradiation results of technologies for a custom DCDC converter

Author: Federico Faccio[1]

[1] *CERN*

Power WG / 164

EMC issues for CMS Tracker Upgrade

Author: Fernando Arteche[1]

[1] *Instituto Tecnológico de Aragón*

Power WG / 165

Roadmap for serial powering

Author: Marc Weber[1]

[1] *Rutherford Appleton Laboratory*

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Discussion

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Roadmap for DC-DC

Author: Federico Faccio[1]

[1] *CERN*

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Access to ASIC Design Tools and Foundry Services at CERN for SLHC

Author: Kostas Kloukinas[1]

[1] *CERN*

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Versatile Link status report

Plenary Session 7 - Reports from WGs / 171

Report from Power WG

Plenary Session 7 - Reports from WGs / 172

Report from Opto WG

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Report from MUG

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Research activities at Pierre & Marie Curie University

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Status and Perspective of Research at IN2P3

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Micro-Electronics at In2P3

CLOSE OUT / 177

CLOSE OUT

Author: Francois Vasey[1]

[1] *CERN*

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Mixed-Signal Challenges and Solutions for advanced process nodes

Author: Bruno Dutrey[1]

[1] *Cadence Design Systems*

MUG / 179

Digital Block Implementation Methodology for a 130nm process

Author: Sandro Bonacini[1]

[1] *CERN*

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Discussion

Author: Kostas Kloukinas[1]

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Future operating mode of the group

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Executive Summary