Development of new readout electronics for the ATLAS LAr Calorimeter at the sLHC

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Abstract

The readout of the ATLAS Liquid Argon (LAr) calorimeter is a complex multi-channel system to amplify, shape, digitize and process signals of the detector cells. The current on-detector electronics is not designed to sustain the ten times higher radiation levels expected at sLHC in the years beyond 2019/2020, and will be replaced by new electronics with a completely different readout scheme.

The future on-detector electronics is planned to send out all data continuously at each bunch crossing, as opposed to the current system which only transfers data at a trigger-accept signal. Multiple high-speed and radiation-resistant optical links will transmit 100 Gb/s per front-end board. The off-detector processing units will not only process the data in real-time and provide digital data buffering, but will also implement trigger algorithms.

An overview about the various components necessary to develop such a complex system is given. The current R&D activities and architectural studies of the LAr Calorimeter group are presented, in particular the on-going design of the mixed-signal and radiation tolerant front-end ASICs, the Silicon-on-Saphire based optical-link, the high-speed off-detector FPGA based processing units, and the power distribution scheme.

I. Introduction

The Liquid Argon (LAr) calorimeters of the ATLAS experiment [1] at the Large Hadron Collider (LHC) [2] consist of 182486 detector cells whose signals need to be read out, digitized and processed. For each detector element, the signal timing and energy deposit are determined. A total of 1524 Front-End Boards (FEB) [3] are installed directly on the detector in radiation environment. In the current system, each of them performs the pre-amplification, shaping and gain-selection, analog buffering and digitization of up to 128 input channels. The analog sampling rate of the Switched Capacitance Array (SCA) of the FEB is 40 MHz, while digitization is performed at up to 100 kHz, after reception of a Level-1 trigger accept signal via the Trigger, Timing and Control (TTC) system. The FEBs also calculate analog sums of up to 32 channels as input to the Level-1 trigger system. The digitized output is transfered with optical links at 1.6 Gb/s per FEB to the 192 Readout Driver (ROD) boards of the back-end system [4]. The ROD implements digital FIR filters on Digital Signal Processors (DSP) to prepare the data for the higher-level trigger and data acquisition (DAQ) systems. The overall architecture of the current system is shown in Figure 1.

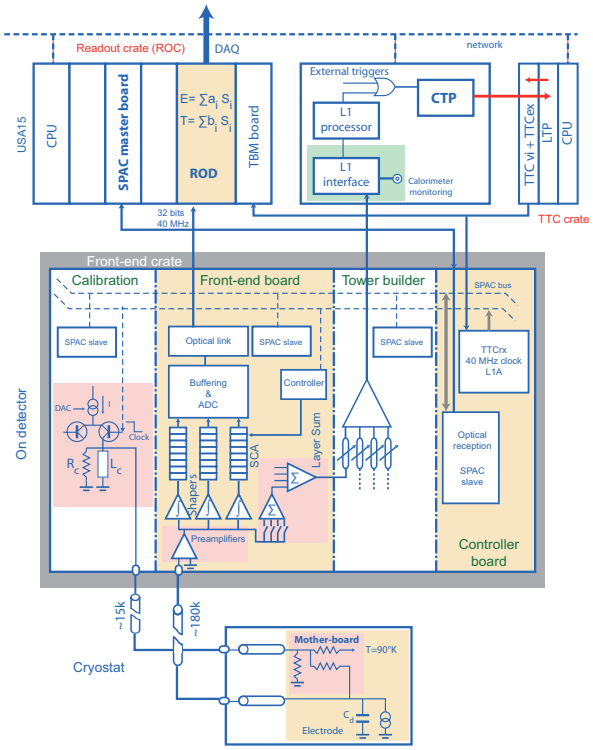

Figure 1: Architecture of the front-end electronics of the current LAr Calorimeter readout.

The main challenge for the design of the front-end system is the radiation in the ATLAS cavern. At nominal LHC operation, with a design luminosity of 10^{34} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and after 10 years of operation, a Total Ionising Dose (TID) of 5 krad(Si), a Non-Ionizing Energy Loss (NIEL) equivalent to 1.6×10^{12} $\mathrm{n/cm}^2$(1 MeV neutrons) and Single-Event Effects (SEE) from 7.7×10^{11} hadrons/$\mathrm{cm}^2(>$ 20 MeV) are expected [5]. In the FEB, 11 types of ASICs with different kind of radiation tolerant technologies, like DMILL and deep-submicron (0.25 μm), are used. They are qualified to function with sufficient performance after these radiation levels, including safety factors of 10-30.

The super-LHC (sLHC) upgrade foresees an increase of instantaneous luminosities up to 10^{35} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$ in the years beyond 2019/2020 and a prolonged operation of the accelerator and the detectors. The current FEB electronics is therefore expected to fail or to be seriously degraded during the sLHC phase [5]. Since only about 6% of spare boards and compo-

nents are available, a continuous replacement of FEB boards or components is not feasible during sLHC running. It is therefore required to design new front-end electronics for the ATLAS LAr Calorimeters and to develop ASICs in more radition-hard technology. Along with the radation requirements some of the design aspects of the current FEB are planned to be improved. The number of ASICs should be reduced, as well as the number of different voltage levels, currently supplied by 19 voltage regulators on board. The voltage distribution system with 58 Low-Voltage Power Supplies (LVPS) is also foreseen to be replaced. The total power consumption per FEB should however not be increased.

The new design gives the opportunity to implement a globally better performing readout system. The Level-1 trigger system should be able to cope with a more challenging scenario: with a higher trigger accept rate, and a longer trigger latency. The latter may be necessary if trigger signals from the Inner Detectors of ATLAS, with a possibly longer readout time, will be included in the trigger decision. Furthermore, it is foreseen to digitize all incoming data at 40 MS/s while keeping the current effective dynamic range of 16 bits. The data shall be transfered by fast optical links to the backend system. Since each FEB produces about 100 Gb/s of data, multi-fibre links are envisaged. Still, each individual optical link must be able to operate at about 10 Gb/s and be radiation tolerant.

The large data rates are also a challenge for the back-end system. The ROD boards of the sLHC generation are planned to treat input from one front-end crate housing 14 FEBs, which corresponds to an input rate of 1.4 Tb/s. Signal processing must proceed within a short latency in the order of 1 μs, since the digital output is foreseen to be fed via the RODs into the Level-1 trigger system. Thus, the hardware trigger will receive digital data with higher granularity which introduces a larger flexibility in the implementation of trigger algorithms. These usually sum up the energy of a given number of calorimeter cells but may also perform more complicated operations. Since the algorithms will be programmable and adjustable to sLHC running conditions, a better optimisation of the suppression of pile-up signals is possible, whose rate is expected to increase by up to a factor of 20 at the sLHC compared to nominal LHC rates. The data pipelines will be implemented in fast digital memory on the ROD board until the Level-1 trigger decision arrives and in dedicated Readout Buffers (ROB) for the higher level triggers and DAQ.

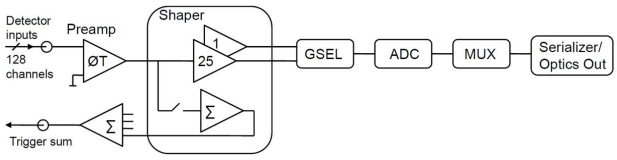

Figure 2: Layout of the front-end prototype with pre-amplifier, dual-gain shaper, gain selector (GSEL), analog-to-digital converter (ADC), multiplexer (MUX) and serializer. The analog trigger sums provide a possible interface to the current trigger electronics.

II. Development of Radiation Tolerant Front-End Electronics

The main components of the future FEB boards are an analog front-end for signal pre-amplification and shaping, an Analog-to-Digital Converter (ADC) with serial output, and a fast optical link. At the sLHC, they have to stand a TID of 300 krad(Si) and a NIEL equivalent to 10^{13} n/cm^2(1 MeV neutrons). The current baseline design is shown in Figure 2. Results from prototypes are presented in the following sections.

A. Pre-amplifier and Shaping

The Silicon-Germanium (SiGe) BiCMOS technology is known for low noise and fast shaping times even after irradiation with high dose levels. The 8WL 0.13 μm process of IBM is chosen to implement prototypes for the LAr pre-amplifier and shaping stages. It is a relatively economic option with $f_T = 100$ GHz for fast ASIC solutions. The pre-amplifier is based on a "super common base" architecture like the one installed in the present FEBs. It achieves an overall equivalent series noise of 25 nV/$\sqrt{\text{Hz}}$ and dissipates only 42 mW [6]. The fully differential shaping stage is split into two gain stages ($\times 1$ and $\times 10$), each consuming 100 mW. A bipolar $CR-(RC)^2$ shaping is chosen, like in the current FEB. Including second stage noise, the front-end has an input-referred noise of ENI=72 nA (RMS), about 28% lower than the pre-amplifier currently used. With the prototype a linearity of better than 0.2% is achieved over the full dynamic range [7]. The peaking time of the shaper is measured to be about 37 ns when a triangular pulse with 20 ns rise and 400 ns fall time is injected, as expected for a typical physics pulse. This value could be further optimized to find the best compromise between electronic and pile-up noise suppression, which, respectively, decrease and increase with longer shaping times. The layout of the front-end ASIC is shown in Figure 3.

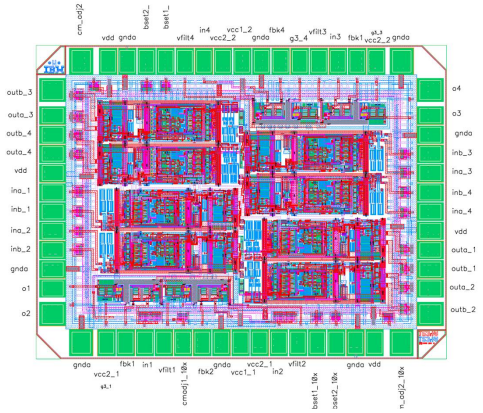

Figure 3: Layout of the LAr analog front-end ASIC design.

The analog front-end was also tested after intake of radiation. First, a SiGe test chip was irradiated with gamma rays up to 50 Mrad(Si) and to 1 MeV neutron equivalent fluences of up to 2×10^{15} n/cm^2. The very high doses were chosen because the

SiGe structures were tested with both high-performance transistors used in the ATLAS silicon tracker read-out and with high-breakdown transistors for LAr applications. The reciprocal gain difference before and after radiation increases linearly with increasing neutron-equivalent dose as expected, with an indication of saturation at highest doses. The same quantity shows a typical power-law dependence for gamma irradiation. The post-radation gains were measured to stay above 40-50 over the dose ranges tested [6], as shown in Figure 4. SiGe BiCMOS is thus well suited for the LAr front-end electronics. Radiation tests with a full prototype of the LAr pre-amplifier and shaper were performed very recently and are reported elsewhere in these proceedings [7].

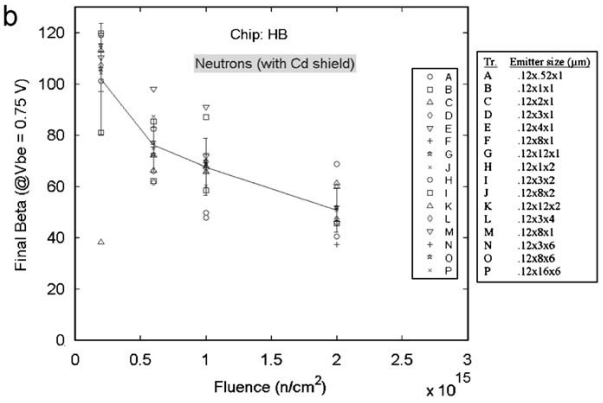

Figure 4: Gain of 8WL transistors after neutron irradiation. A cadmium shielding has been in order to avoid excess damage from thermal neutrons.

B. *Mixed signal front-end ADC*

The output signals of the pre-amplification stage need to be converted into digital signals at a sampling rate of 40 MS/s. This rate is originally fixed by the LHC bunch crossing rate but will be kept also for the sLHC stage even if the upgraded accelerator will operate with longer crossing intervals of 50 ns [8]. The ADC must provide 12 bit resolution in order to cover the full range of interesting energy deposits in the calorimeters from 20 MeV to 3 TeV with 15/16 bit dynamic range. Radiation tolerance and immunity to single event effects (SEE) are another requirement. Furthermore, the ADC output needs to be serialized to match the interface to the subsequent optical link component. Previously developed ADCs with similar performance of 12 bit at 40 MS/s [9] do thus not fit all requirements.

The R&D activities follow two strategies: evaluation of commercial off-the-shelf components advertised as being radation tolerant, like AD9259 , ST-RHF1201 , TI-ADS5281 , and development of a custom ADC chip based on CMOS technology. The IBM 8RF 0.13 μm CMOS technology was shown to be sufficiently radiation hard and available at lower costs than an implementation in SiGe. The 12-bit pipeline ADC is composed of 8 stages of 1.5 bit resolution with digital error correction, which requires calibration constants to be stored in radiation hard memory. The main building block of the ADC is an operational trans-impedance amplifier (OTA) which is at the core for the sample-and-hold (S/H) and multiplying DAC subsystems of each digitisation stage. A sampling capacitance of 1 pF is chosen in the fast S/H stage to reduce the electronic noise, which should stay below 150 μV in total. A test chiplet was submitted via CERN to the MOSIS foundry with an OTA structure and a cascade of two track-and-hold stages. The chiplet is currently in production and expected back for tests by late autumn 2009.

Digital tests of the ADC output stage were performed using commercial non-radiation hard components. Figure 5 shows the test setup. Test signals were fed into a 4×14-bit ADC block. The digitized signals were input to 8×64-bit DRAM, where they were combined with an 8-bit bunch counter. The signals were timed with a 40 MHz clock, similar to the TTC system of ATLAS. The subsequent multiplexer received 4×16 bit at 40 MHz converting the data to a 16 bit data stream at 160 MHz. The final serializer applied an 8b/10b encoding and was driving an 3.2 GHz optical link, at whose end a data receiver board measured the consistency of the data. For the high-speed components a 160 MHz crystal derived clock was used. The control logic of the system was based on Gray codes to be less sensitive to SEE. The DAQ chain was tested successfully and can be used to develop further concepts to reduce sensitivity to radition damage.

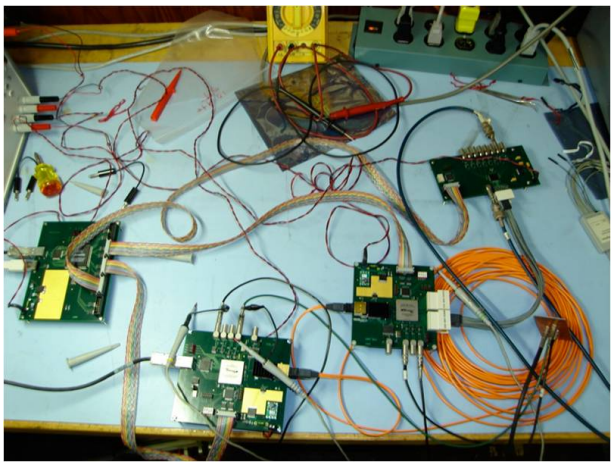

Figure 5: Test setup for the digital ADC logic.

C. *Radiation tolerant optical links*

A challenging project is the development of the very fast optical link which needs to perform at 10 Gb/s and be at the same time insensitive to radiation. To achieve these requirements, Silicon-on-Sapphire (SoS) technology was selected. The 0.25 μm UltraCMOS process provided by Peregrine Semiconductors promises low power consumption and low cross-talk needed for the mixed-signal ASIC design. It is relatively economical or small and medium scale chip development. In 2007, first TID and SEE radiation tests were performed [10]. After irradiation with gamma rays from a ^{60}Co source up to 4 Mrad,

only small leadkage currents of about 250 nA and small threshold voltage increase of about 0.1 V and below were measured for both NMOS and PMOS transistors. When exposing the chiplet to a proton beam with an energy 230 GeV, no SEE was observed in the shift registers at a flux of 7.7×10^8 protons/cm^2/s and they were still correcly functioning after total fluences of 1.9×10^{15} protons/cm^2, which corresponds to 106 Mrad(Si).

A first prototype of the so-called Link-on-Chip (LOC) suffered from high jitter, which is expected to be overcome in the most recent design. The main building blocks of the new LOC2 transceiver are a 16:1 serializer with a CML driver running at 5 Gb/s. Eventually, the conversion to optical signal is planned to be performed by XFP/SFP+ or Versatile link [11] modules. The user data and clock are interfaced to an I/O buffer with 64b/66b encoding, scrambling and possibly data compression. For the prototype, the I/O buffer will be implemented into a standard FPGA with a 16-bit LDVS signal bus at the output to the serializer stage. The serializer is composed of three stages of 2:1 multiplexers running at 312.5 MHz, 625 MHz and 1.25 GHz, respectively. The last and most critical serialization step is implemented in form of two fast transmission gate D-flip-flops, operating at 2.5 GHz. The post-layout simulation of the corresponding 2.5 GHz PLL and of all other components show that the LOC2 requirements are met. In particular, a bit error rate lower than 10^{-12} is achieved, and the total jitter is in the order of 35 ps using an ideal power source. The power consumption is below 500 mW or less than 100 mW per Gb/s. The LOC2 chip is submitted to the foundry and measurement results are expected soon. The layout is shown in Figure 6. In an effort towards an even higher data rate, a 5 GHz LC-tank based PLL is also being designed. In preliminary simulations random jitter below 1 ps (RMS) are observed. This component would be needed to reach the ulitmate goal of a transceiver operating at 10 Gb/s.

Figure 6: Layout of the LOC2 test structure.

D. Power Distribution System

The power supply scheme of the current LAr front-end electronics converts 380 V AC into 280 V DC which is distributed to the LVPS close to the on-detector front-end crates. Each water-cooled LVPS consists of eight isolated switching DC-DC convertors, which need to run in radiation environment and a significant residual magnetic field of up to 100 mT. In the new powering concept the number of different voltages should be reduced and total power consumption is limited to the current level. Furthermore, single points-of-failure should be avoided. In the upgrade design, point-of-load (POL) regulators are foreseen to perform DC-DC conversion in close distance to the FEBs. In the Distributed Power Architecture a main converter generates a single voltage on a distribution bus where the POL are connected. In an Intermediate Bus Architecture, a second set of bus voltages is provided from the main bus, then lower voltages are given by the POL converters. Two commercial POL (LTM4602 and IR3841) were tested for EMI sensitivity in different positions inside and outside the front-end crate. The outcome was that shielding is necessary if the POL are placed inside the crate, on the backside of the FEBs. Radiation tests will be performed. Results on other commercial DC-DC converters are reported elsewhere [12].

III. High Bandwidth Back-End Electronics

In the R&D baseline layout, 14 FEBs are to be connected to one ROD, so that in total about 218 ROD boards will be needed. This assumes a continuous data stream at 100 Gb/s per FEB link, or 150 Tb/s in total for the whole back-end system. The possible architecture of the upgraded LAr back-end is shown in Figure 7. Modern fiber connectors in MPO/MTP style already combine 12 fibers, so that the transmission rate per link is feasable provided that the radiation hard front-end link performs at 10 Gb/s. A reduction of the number of links are being evaluated, like lossless data compression/decompression algorithms with ultra-short latency or the reduction of bits per ADC. The latter is only an option if the effect on physics results are negligible.

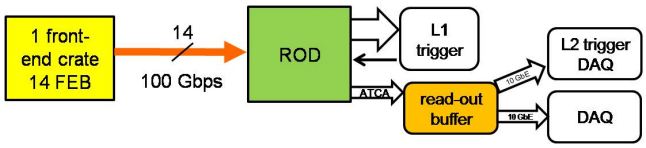

Figure 7: Possible back-end architecture of the upgraded LAr read-out.

In the ROD, FPGA based SERDES are applied to receive the data. Digital signal processing with modern FPGA are provided by a large number of DSP slices per module. The ROD implements a digital FIR filter, to determine the pulse height and signal timing from a given number of sampling points. It should furthermore be capable to align the signals in time and identify the bunch-crossing for the subsequent trigger algorithms. It must eventually perform a summing of signals from neighbouring cells to reduce the data size before transfer to the Level-1 trigger system. The incoming data will also have to be digitally buffered in fast digital memory on the ROD board until the Level-1 trigger decision arrives. A Readout Buffer (ROB), which is accessed by the higher-level triggers, must be implemented either on the ROD or on a separate board inside the ROD shelf system.

Prototype ROD boards are built based on the Xilinx Virtex-5 FPGA (XC5VFX70T) and 75 Gb/s fiber-optic tranceivers of Reflex Photons with SNAP12 connectors. A ROD injector board exploring the Altera Stratix GX II FPGA provided the pseudo-random data source. Both are shown in Figure 8. With this test setup, a rate of 6.5 Gb/s per fibre were found to be feasible. The FIR-filter and energy sums were successfully implemented. Timing alignment still needs to be studied. A total data processing latency of below 1 μs was found to be achievable using parallel DSP slices on the FGPA, and taking the fiber-length of about 70 m between front-end and back-end into account. This is a first step towards a fully digital Level-1 trigger. More R&D is however needed to properly design the interface to the trigger system and to evaluate the implementation of possibly new algorithms which can profit from the higher granularity of the physics signals.

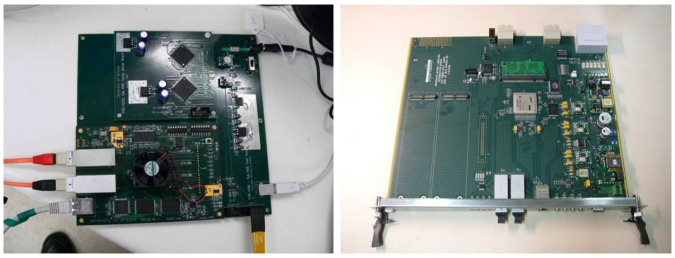

Figure 8: ROD injector board (left) and ROD prototype in ATCA format (right).

For integrating the ROD into a shelf system, the Advanced Telecommunication Computing Architecture (ATCA) is evaluated as a framework that provides shelf management protocols, power management, fast fabrics, and supports module redundancy, if needed. Developments are ongoing for fast data transfer in 10Gb Ethernet between ROD boards and from RODs to an external ROB card inside the ATCA shelf. In a recent concept, the ROB is reduced to a single PC server with fast RAM, to which the PCs of the higher level trigger farm can directly access. For the data transfer into the RAM, Remote DMA is being tested. A custom made buffer module as currently implemented in ATLAS [13] could therefore become obsolete. The data buffer may even be integrated into the ROD board, which is also being studied.

IV. Summary and Outlook

The R&D activities for an upgraded read-out of the ATLAS LAr Calorimeter at the sLHC concentrate on the development of radiation tolerant ASICs for the analog and digitial front-end and on high-performance back-end electronics. Prototypes for the pre-amplifier and shaping system, for the ADC and the optical link-on-chip are being produced and their functionality tested with promising results. Radiation tests of the SiGe, CMOS and SoS technologies showed sufficient immunity to radiation damage. These tests are currently being repeated with the protoypes built recently. Development and tests of the new POL powering scheme are starting, first evaluating commercial components. On the back-end side, the time critical steps of the digital signal processing are studied. Also here, prototypes of the ROD board and ATCA test setups are successfully installed. They are used to evaluate the performance and to develop new algorithms for data treatment, data volume reduction, and fast data transfer on fabrics. The requirement to replace the LAr Calorimeter readout and the opportunity to implement a fully digitial calorimeter trigger, lead to a series of R&D challenges, for which promising first results were obtained and which will be further persued in the near future.

V. Acknowledgements

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