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Development of new readout electronics for the ATLAS LAr calorimeter at the sLHC

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The ATLAS Liquid Argon (LAr) calorimeter consists of 182,486 detector cells whose signals need to be read out, digitized and processed, in order to provide signal timing and the energy deposited in each detector element. The current readout electronics is not designed to sustain the ten times higher radiation levels expected at sLHC in the years ≥2017, and will be replaced by new electronics with a completely different readout scheme. The future on-detector electronics is planned to send out all data continuously at each bunch crossing, as opposed to the current system which only transfers data at a trigger-accept signal. Multiple high-speed and radiation-resistant optical links will transmit 100 Gbps per front-end board, each covering 128 readout channels. The off-detector processing units will not only process the data in real-time and provide digital data buffering, but will also implement trigger algorithms.
An overview about the various components necessary to develop such a complex system will be given. The current R&D activities and architectural studies of the LAr Calorimeter group will be presented, in particular the on-going design of the mixed-signal and radiation hard front-end ASICs, the Silicon-on-Saphire (SOS) based optical-link, the high-speed off-detector FPGA based processing units and the power supply distribution scheme.

Summary

The ATLAS experiment is one of the two general purpose detectors designed to study the proton-proton collisions at the Large Hardron Collider (LHC) with a center-of-mass energy of 14 TeV and to explore the full physics potential of the LHC at CERN. A vital part of the ATLAS detector is the Liquid Argon (LAr) calorimeter which is used to measure the energy of electromagnetic and hadronic particles, and to trigger on interesting physics events. The LAr calorimeter consists of 182,486 detector cells in total. Their signals need to be read out, digitized and processed, in order to provide accurate signal timing and the energy deposited in each detector element. The current readout electronics is not designed to sustain the ten times higher radiation levels expected at sLHC in the years ≥2017, and will be replaced by new electronics with a completely different readout scheme. The different components and general architecture of the upgraded system will be presented.

The challenges for the on-detector electronics are two-fold: it must be radiation tolerant and able to transmit large amount of data at high rates. The future electronics is planned to send out all data continuously at each bunch crossing, as opposed to the current system which only transfers data at a trigger-accept signal.
For the front-end electronics, two R&D efforts are going on which are focused on the analog and mixed-signal ASIC design, respectively. For the analog part, a test structure chiplet based on 0.13 µm SiGe BiCMOS technology will be used to test radiation performance of different transistor configurations. A prototype with a low-noise pre-amplifier, CR–(RC)2 signal shaping and two gain settings is currently being designed and tested. For the mixed-signal part, a custom pipeline ADC in IBM 8RF CMOS technology is chosen and many critical techniques, such as S/H capacitor, amplifier and digital correction etc. have been studied. In summer 2009, a MOSIS test structure proposal is planned to be submitted. For the high speed digital components jitter control is being investigated. An issue is also to provide power to the front-end modules, and radiation and magnetic field tolerant devices are developed, where experience from the current LAr system is used.

The digitized data is sent to the off-detector readout via multiple high-speed and radiation-resistant optical links. The transmission of presumably 16 bit signals from 128 channels per front-end board at 40 MHz requires a total data rate of ˜100 Gbps per board. Currently, radiation tolerant multi-fibre ribbons are tested. The optical transceiver is planned to be in 0.25 µm UltraCMOS Silicon on Sapphire (SOS) technology due to its inherent resistance to radiation. Results from a test chip as well as from a Link-on-Chip prototype will be presented.

The off-detector processing units, the readout drivers (ROD), will not only process the data in real-time and provide digital data buffering, but will also implement trigger algorithms. The data will be received by high-speed commercial optical links and FPGA based SERDES components. Data processing and digital filtering will also be realized in modern FPGAs. A challenging task is the implementation of trigger algorithms which need an interconnect between the ROD boards. The ATCA technology is chosen to provide the framework for fast serial links between the RODs. First ROD prototypes equipped with a Xilinx Virtex-5 FPGA together

with an optical signal injector board currently run successfully at about 40% of the target data rate. A second ROD prototype in ATCA format is expected to be available for further tests in summer 2009.

In the presentation, an overview about the various components necessary to develop this new and complex readout system will be given. The current R&D activities and architectural studies of the LAr Calorimeter group will be presented, in particular the on-going design of the mixed-signal front-end ASICs, the SOS based optical-link, the high-speed off-detector FPGA based processing units and the power supply distribution scheme.

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