A Prototype Front-End Readout Chip for Silicon Microstrip Detectors Using an Advanced SiGe Technology

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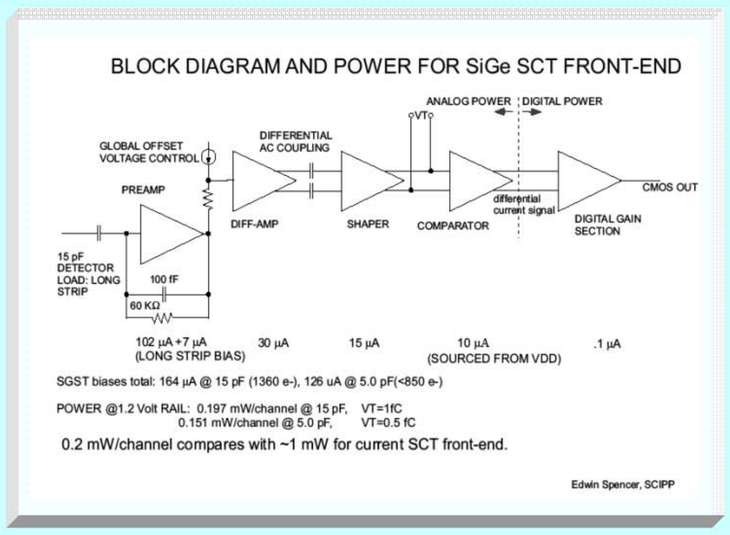
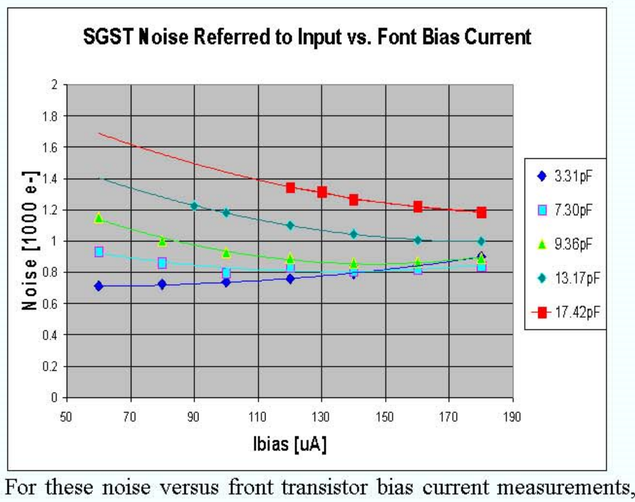
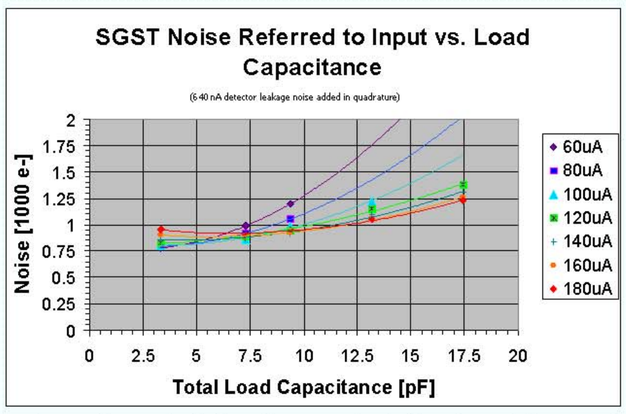
We have been evaluating silicon germanium (SiGe) BiCMOS technologies as a possible choice for the required silicon microstrip and calorimeter front-end readout chips for the ATLAS Upgrade, given that they show promise to provide necessary low noise at low power. Evaluation of the radiation hardness of these technologies has been under study and is reported elsewhere, including a poster here. To validate the expected performance of these technologies, we designed and fabricated an 8-channel front-end readout chip for a silicon microstrip detector using the IBM 8WL technology, a possible choice for the ATLAS Upgrade. Preliminary electrical characteristics of this chip are presented.

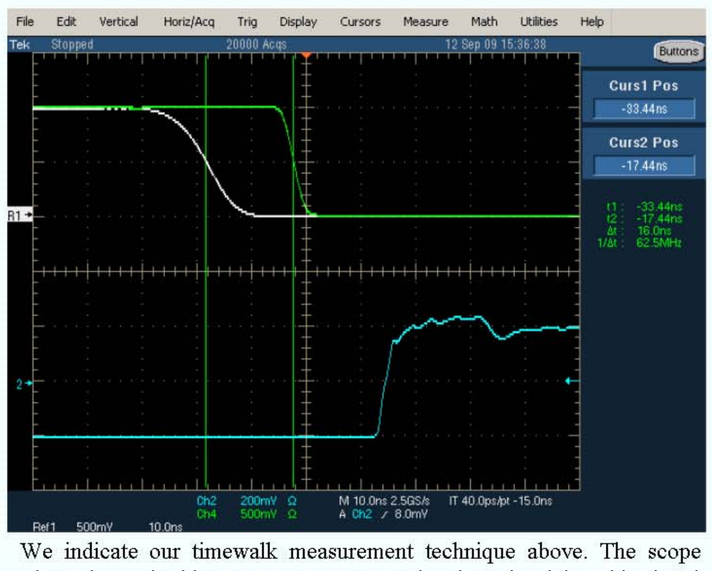




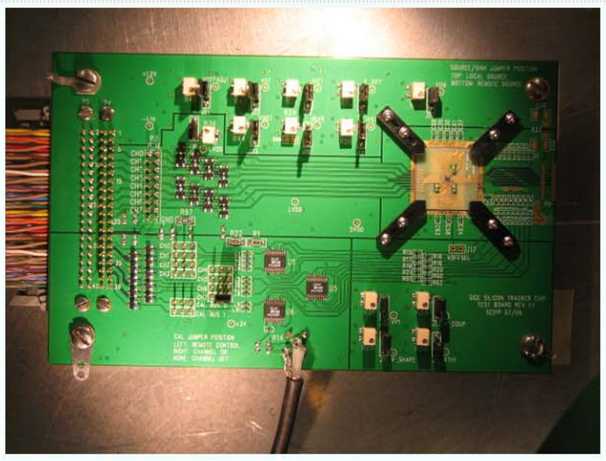
For these noise versus front transistor bias current measurements, the shape was adjusted to 16 ns time walk with a 1 fC threshold for signals between 1.25 fC and 10 fC. The 17.4 pF curve has no data points below 120 µA since the VSHAPE control is out of range for lower front currents.



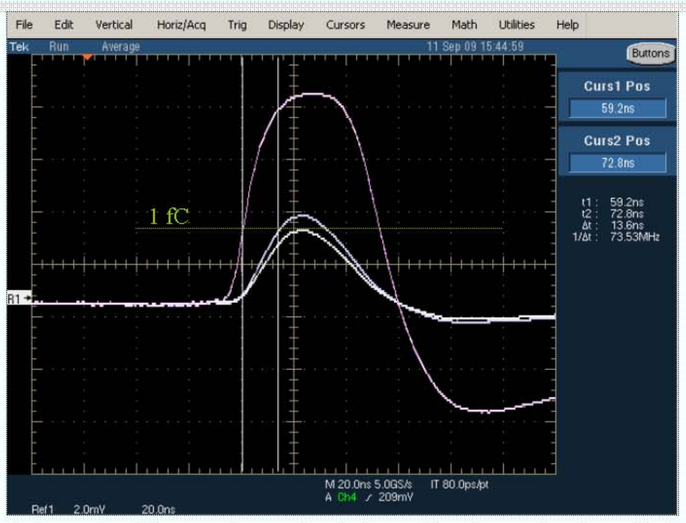
Load capacitance includes all strays, including the miniboard, the bond pads, and an estimate of the chip circuit and protection diodes.



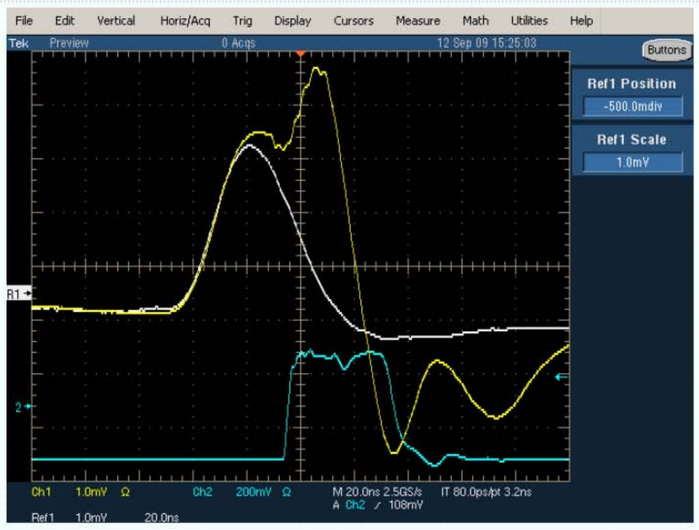
We indicate our timewalk measurement technique above. The scope trigger is on the blue LVDS comparator signal on the right. This signal varies in width with noise in the shaper analog signal. The calibration step signal on the left is averaged ~200 times. Since it has constant width, the average shows as a signal with lower rise time for the white 1.25 fC signal on the left. The green 10 fC signal has apparent faster slew, indicating much less jitter in the LVDS signal width. The cursor indicates a timewalk of 16 ns for this amplifier setting. Note that the earlier green 10 fC signal appears to the right of the later 1 fC signal, since we are post-triggering.



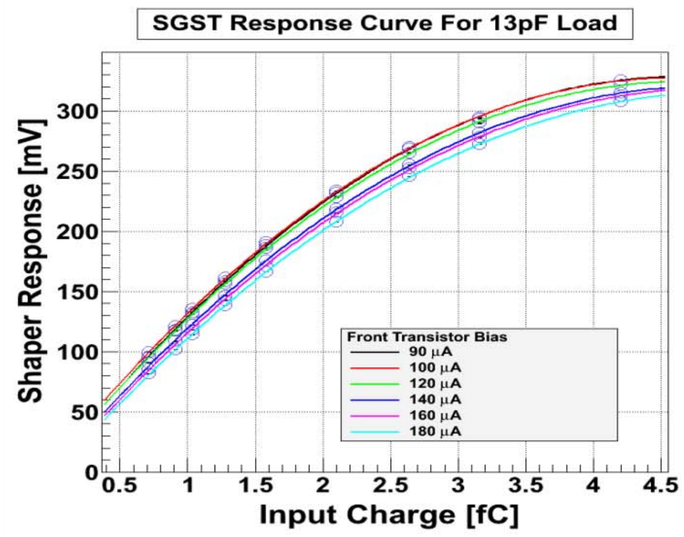
The SGST chip on the test motherboard. Readout of eight amplifier/comparators is by LVDS connector at the left. The 15 x 15 mm miniboard mounting the SGST is held by four Delrin finger clamps.



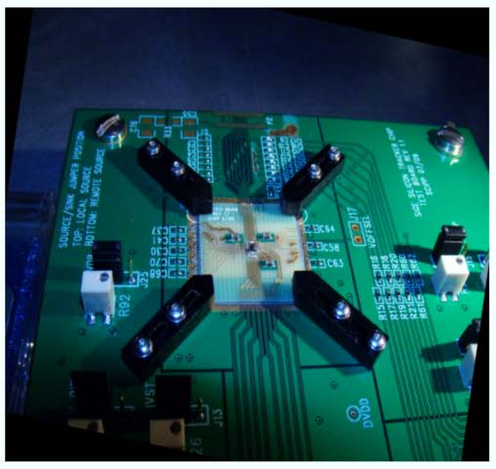
A picoprobe is used to illustrate shaper signal timewalk. Shaper signals are buffered by source follows for the Picoprobe. Traces are 1 fC, 1.25 fC, and 10 fC. Vertical cursors intersect 1.25 fC and 10 fC signals at 1 fC threshold.
Timewalk is 13.6 ns. Two amplifiers have varactor capacitors, with the controlling VSHAPE = 1.000 V in this case, so that shape can be tuned.



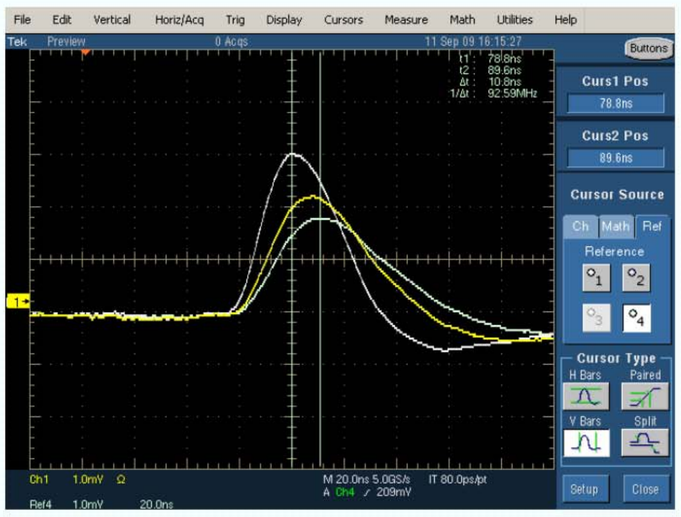
These scope traces indicate the positive shaper side feedback when the comparator trips. There is no emitter follower buffering between the two output shaper nodes and the differential comparator input. For 1 fC input, the feedback from the blue LVDS trigger is evident. White trace is with no comparator trigger, and yellow trace is with comparator trigger.



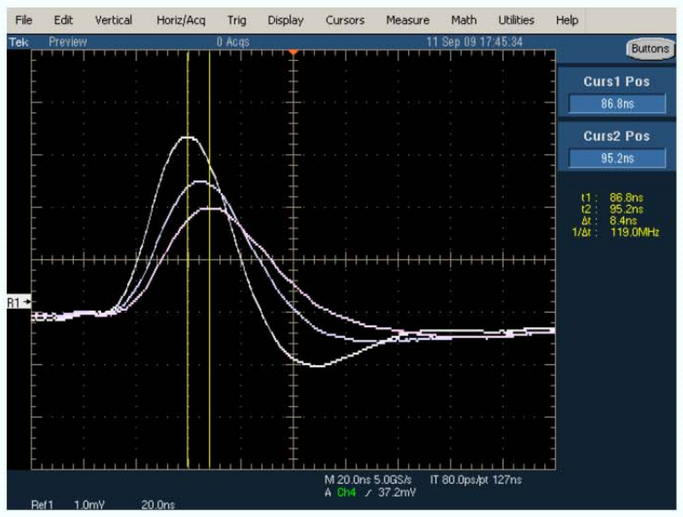
Above is the shaper response curve at 13 pF for a range of front transistor biases. Timewalk was adjusted to 16 ns for each setting. The channel uses two differential amplifiers in addition to the preamp stage giving the nonlinear transfer function.



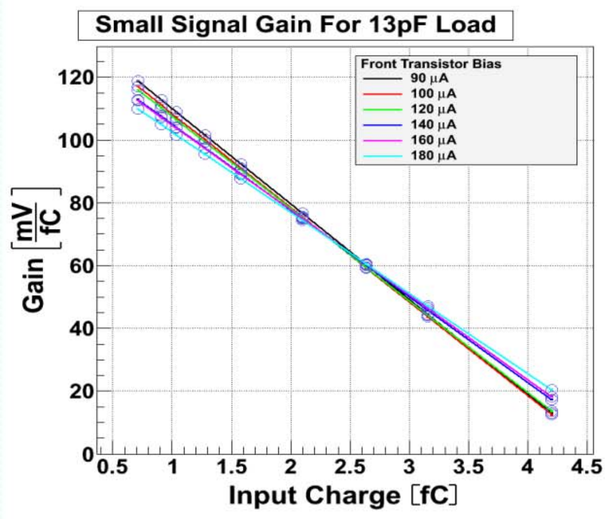
Closeup of the miniboard with Delrin clamp. The miniboard wire bonds to the motherboard are easy to redo. This scheme allows radiation testing of the SGST with minimal material experiencing neutron activation. During radiation testing, the miniboard will clamp onto a conductive silicone elastomeric pad that will short appropriate chip pad nodes together.



Above is one side of the differential Shaper signals with a 1 fC input, 3.31 pF load cap, and Ibias = 120 µA. VSHAPE is the voltage control for varactors on two gain stages. VSHAPE = 1.500V, 0.750V, 0.000V (highest signal to lowest).
Signal peak shifts 10.8 ns over the VSHAPE range. This allows timewalk to be controlled for each front chip.



The range of Shaper signal adjustment is illustrated above. The input is 1 fC with an 18 pF load. The control varactor has three settings: VSHAPE = 1.5 V, 0.75 V, 0 V for largest signal to smallest. The peak shifts 8.4 ns over the VSHAPE range.



Small signal gain is the derivative of the transfer function curve. Small signal gain is used in calculating the noise referred to preamp input.

This 8-channel chip demonstrates that acceptable noise values can be achieved for the silicon microstrip detectors currently envisaged for the ATLAS Upgrade Detector, especially the long strip (~10 cm) sensor version, at exceptionally low power. Additional optimization of the front transistor and feedback could further reduce noise and power for the short strip sensor version. The design and technology easily meet the required 16 ns time-walk requirement and faster performance could be easily achieved. The design allows for variable control of the front transistor bias current and the shaping time, thus allowing noise vs. power optimization for a range of sensor characteristics, in particular to accommodate changes in sensor characteristics due to ongoing radiation damage.