Contribution ID: **131** Type: **Poster**

A Prototype Front-End Readout Chip for Silicon Microstrip Detectors Using an Advanced SiGe Technology

Thursday, 24 September 2009 16:55 (20 minutes)

The upgrade of the ATLAS detector for the high luminosity upgrade of the LHC will require a rebuild of the Inner Detector as well as replacement of the readout electronics of the Liquid Argon Calorimeter and other detector components. We proposed some time ago to study silicon germanium (SiGe) BiCMOS technologies as a possible choice for the required silicon microstrip and calorimeter front-end chips given that they showed promise to provide necessary low noise at low power. Evaluation of the radiation hardness of these technologies has been under study. To validate the expected performance of these technologies, we designed and fabricated an 8-channel front-end readout chip for a silicon microstrip detector using the IBM 8WL technology, a likely choice for the ATLAS upgrade. Preliminary electrical characteristics of this chip will be presented.

Summary

The expected upgrade of the Large Hadron Collider (LHC) to increase luminosity by as much as an order of magnitude will require a major upgrade of the ATLAS detector. Included in the upgrade will be a rebuild of the entire inner detector, replacement of the readout electronics of the Liquid Argon Calorimeter (LAr) as well as many other detector components. The proposed new Inner Detector will include silicon microstrip detectors. The silicon microstrip detectors, especially those proposed to be 10 cm long, and the LAr will present relatively large capacitive loads to the front-end readout chip. These electrical characteristics along with the necessary shaping times less than 20 ns, are well suited to bipolar circuitry as proven in several past experiments including the present ATLAS SCT. The advanced germanium doped bipolar technologies are especially suited to this since they yield extremely small base resistances (of order tens of Ohms), which allow very low noise operation without excessive bias currents.

In order to validate these technologies for use in the upgraded ATLAS Detector, our group has performed radiation studies on several commercial technologies [1,2,3,4]. We have also built one prototype chip using the IHP SG25H1 25 μm technology. The IBM 8WL technology looks very promising for ATLAS upgrade work, given our radiation results and the fact that its CMOS component is compatible with the IBM 8RF technology now being used for several other prototype chips for the upgrade.

In order to confirm the electrical performance of this 8WL technology, we have designed and fabricated an 8-channel front-end readout chip. It consists of pre-amp, shaper and comparator circuits for each channel along with LVDS output drivers such that the comparator outputs can be fed into an FPGA for testing. Any final readout chip would likely contain additional digital circuitry such as pipeline, output buffer and command decoder, which can be implemented with CMOS structures available in the 8WL technology and compatible with 8RF designs already in development.

Along with a description of the circuit and simulation results, we will present preliminary electrical characterization results showing the performance that can be achieved with this technology.

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Session Classification: POSTERS SESSION

Track Classification: ASIC's