

Upgrade of the BOC for the ATLAS Pixel Insertable B-Layer

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Abstract

The phase 1 upgrade of the ATLAS [1] pixel detector will be done by inserting a fourth pixel layer together with a new beampipe into the recent three layer detector. This new detector, the Insertable B-Layer (IBL) should be integrated into the recent pixel system with as few changes in services as possible, but deliver some advantages over the recent system.

One of those advantages will be a new data transmission link from the detector modules to the off-detector electronics, requiring a re-design of the electro-optical converters on the off-detector side. First ideas of how to implement those, together with some ideas to reduce cost by increasing the systems throughput are discussed.

I. REQUIREMENTS OF THE UPGRADE

Readout wise the IBL will be run as part of the recent pixel detector subsystem. Hence the IBL subsystem will have to be compatible to the pixel subsystem in terms of software integration and connectivity with other ATLAS systems.

A. Integration into the recent ATLAS pixel readout structure

The off-detector side of the ATLAS pixel detector readout is a VME based system. It delivers a maximum data rate of 160 MB/s (per building block) to the higher level readout systems. 16 building blocks can be integrated into one readout crate and controlled by a Single Board Computer (SBC), using the VME bus interface.

A building block of the readout system is composed of a pixel ReadOut Driver (ROD) and a pixel Back Of Crate card (BOC). The ROD can send commands to and receive data from a maximum of 32 modules via the BOC. It is given four floating point Digital Signal Processors (DSP) to shrink and evaluate calibration data. Data received from the modules is, during data taking, put out through a high-speed interface on the BOC, the SLink. The VME bus is only used for configuration and calibration communication (e.g. histogram download).

The BOC is an I/O board to the ROD, carrying electro-optical converters (cf. [2]). It adds delays to sent signals to adjust the detectors phase against the LHC bunch crossing and to the returned data, aligning it with the off-detector clocks. The SLink interface is attached to the BOC as a mezzanine card and controlled by the ROD only. A special feature of the Pixel¹ BOC

is decoding of 80 MBit/s streams into two 40 MBit/s streams, which is an input requirement of the ROD.

Software interfaces have been written for the recent system, to run calibration scans, generate histograms and start data-taking. Part of this software package is the firmware running inside the ROD DSPs. It can control all readout hardware, generate configurations for the system automatically and was checked for consistent results during a long calibration phase. Most of this software should be kept as is for the IBL system. Particular importance goes to the firmware of the DSPs on the readout drivers, doing most of the calibration scan control, data analysis and histogramming. Hence the pixel RODs should not undergo changes that are not desperately needed or can be done without changing the DSP code. They should be re-used for the IBL system, concerning the software point of view.

B. Upgrades needed for the IBL

The Insertable B-Layer will suffer higher occupancy due to its lower distance from the interaction point, hence a higher read out rate per detector area will be needed. As single frontends (two per IBL module) are read out a single transmission line only has to transfer a quarter of the former area. Estimates for the IBL frontend data rate assume more than 80 MBit/s. This will be served with 160 MBit/s readout via a single fibre, as opposed to two 80 MBit/s links in the existing B-Layer.

Balanced encoding is foreseen for the coming system to allow for automated threshold adjustments and clock reconstruction in the off-detector electronics. 8B10B encoding will therefore be integrated into the next on-detector readout chip. It allows to use market solutions for clock-data recovery (CDR) and implementing simple failure checks via parity control. The receiver can automatically sense the average light level per transmission line and a per channel monitoring can give direct status information.

The BOC *must* be upgraded to handle the new data rate and, in the process of keeping things simple, rescale it for the RODs input. A decoder will be integrated into the BOC as it has to do the CDR for changing the data rate. This implies a change in data rate down to 144 MBit/s: 10 Bit data transferred at 160 MBit/s are decoded into 8 data bits and a single status bit, offering special k-words of the code. This either needs an adaptation on the ROD side to read data from the BOC asynchronously or a conceptual change moving the first registration of data into the BOC (Therefore removing the redundancy of the status bit) and reading it from the ROD side as an input FIFO.

¹ATLAS pixel uses the same readout system structure and hardware as the SemiConductor Tracker (SCT) with small modifications.

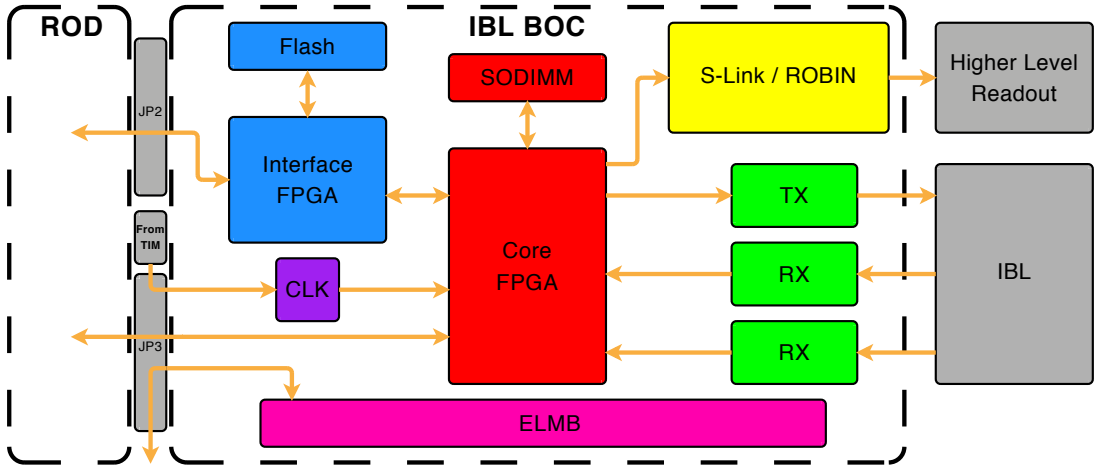


Figure 1: Schematic view of the proposed IBL BOC Layout

The Timing, Trigger and Control (TTC) path will use the same encoding standard as is used in the recent ATLAS pixel detector, BiPhase Mark (BPM) encoding. It can either be encoded by the recently used transmission IC, the BPM-12, or implemented into programmable logic. In the IBL system, two frontends (one module) will share a common TTC link.

II. CONCEPTUAL LAYOUT

Following the requirements, a first schema (cf. Figure 1) for the IBL BOC has been decided on, which allows for maximum flexibility in implementation of other components. Additional features that seemed missing in the previous system have also been included into the new schema.

A. Fulfilling the needs

The core of the IBL BOC is a large programmable device, which connects to any data-path element of the BOC, optical receivers (RX), optical transmitters (TX) and Higher Level Trigger (HLT) connections. Additionally most of the backplane connections will be fed into it. Final layout decisions can thereby be implemented in firmware, when the IBL system goes into production stage.

An interface FPGA is to serve firmware to the core, deliver a bus interface to the ROD and give JTAG access. This FPGA should only be programmable with manual intervention (programming cable), whilst giving easy upgrade-ability for the core of the BOC.

An ATLAS Embedded Local Monitoring Board (ELMB) will be mounted to read monitoring values from the BOC and serve as a native Detector Control System (DCS) interface. Reading and archiving of PiN currents, voltages and interlock values will thus be possible without interaction with the DAQ software system. Also the DCS side will be of much bigger value in debugging the IBL readout chain, which took a lot of DAQ expertise with the recent system.

Optical converter boards will be served with the same 40-pin sockets as before to serve either the same or new plug-ins. The

latter is guaranteed by wiring all I/O pins of the connector up with the central programmable device.

The connection to the higher level readout will be prepared as a mezzanine slot. Opposing to the recent BOC, this will be served with a reprogrammable interface and is planned to host a single ReadOut Buffer Input (ROBIN, see [3]) card. This will remove a transmission line from the readout chain giving a faster and simpler interface between the readout building block and the HLT.

B. Minding the upgrade

In preparation are multiple layouts for the IBL readout based on the recently used VME crate architecture and TTC Infrastructure:

The simplest one is to keep the ROD as is and have the BOC be the I/O card as it is now. The BOC will have to split Data here, such that the per-line data rate goes down below 40 MBit/s. As mentioned above, the ROD-BOC Interface would have to change to an asynchronous one, as raw data rate will not be a multiple of 40 MBit/s anymore.

The opposite approach is to also re-design the ROD, allowing faster operation, in particular concerning data-taking throughput and VME bus performance. This comes with the complication of either rewriting software or hard boundaries on the design, such as usage of the same family of DSPs that is used in the recent ROD.

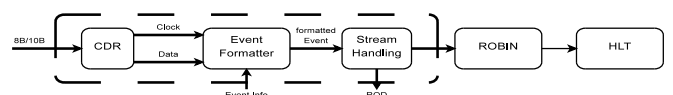


Figure 2: Data path implementation using the BOC

Our favoured design goes with a reproduction of the previous ROD with some simple modifications: The data-path (c.f. Figure 2, dashed container) is removed from the ROD and placed into the BOC. Calibration data that needs to reach the

DSPs would be passed over by the BOC via a reversed SLink Interface.

Advantages are significant:

1. The ROD production will be very close to that of the previous ROD, implying fewer complications.
 - (a) Either full reproduction of the previous ROD with pin compatible replacement of some components
 - (b) Minor re-designs, speeding up VME bandwidth, maybe running a JTAG interface for the BOC into the Program Reset Manager (PRM) on the ROD for in-system reprogramming ability.
2. The former formatting and event building section of the ROD could be removed from the layout or just not equipped. Therefore a total of 9 FPGAs and multiple obsolete memories will not be needed in this ROD design, making it a lot cheaper.
3. The new BOC would deliver a data path during data-taking that can handle a higher throughput than the recent ROD. Data rate could be increased by at least a factor of two, assuming there is a, yet to be defined, faster interface to the embedded ROBIN card. Hence the total system size could be reduced by the same factor decreasing cost again.

To circumvent changing the DSP code, FPGAs on the ROD would be reprogrammed to map the previous ROD data-path functionality into the BOCs data path, hence blinding the DSP code to most of the changes. Programming of the new BOC data path will include re-use of the ROD sourcecode, as a lot of components will only need minor modifications.

C. Programmable encoding

A first successful approach has been made to move the recent encoding chip (BPM-12, cf. [2]) functionality into

an FPGA. Implementing the encoding standard as a reprogrammable block would allow for later changes of the standard and re-use of hardware for other systems. In the present system there is no way of bypassing the encoding process or implementing another encoding standard (8B10B), which would help for loop-back testing of the optical transmission lines, now or in the future system. This would definitely be overcome by using a reprogrammable encoder with a standard optical transmitter.

III. CONCLUSIONS

The new data path of the IBL implies a change in off-detector readout electronics, which will be served with a new BOC card. Servicing and DCS interface will be simplified compared to the recent ATLAS pixel BOC. It will be kept as flexible as possible to allow later implementation of final configurations or protocols, while serving an early prototype for system testing [4]. The BOC will fit into the recent system base, while allowing to speed up the total bandwidth per building block, shrink the IBL system and hence reduce production cost.

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