An Insertable B-Layer Readout Upgrade: The IBL-Back of Crate Card

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The first upgrade of the ATLAS Pixel detector will be done by inserting a fourth pixel layer together with a new beampipe into the recent three layer detector. This new detector should be integrated with as few changes in services as possible, but deliver some advantages over the recent system. One of those advantages will be a new data transmission link from the detector modules to the off-detector electronics, requiring a re-design of the electro-optical converters on the off-detector side. First ideas of implementing those, together with some ideas to save money/increase efficiency are shown here.

Requirement 1: Integrating the IBL into the recent ATLAS Pixel Readout Structure

The off-detector side of the ATLAS Pixel detector readout is a VME based system. It delivers a maximum data rate of 160 MByte (per second and building block) to the higher level readout systems. 16 building blocks can be integrated into one readout crate and controlled by a Single Board Computer (SBC), using the VME bus. Data taking does not need the VME bus interface, other than for configuration, whilst the detector calibration makes heavy use of the VME Bandwidth.

A building block of the readout system is composed of a pixel ReadOut Driver (ROD) and a Pixel Back Of Crate card (BOC). The ROD can send commands to and receive data from a maximum of 32 modules via the BOC. It is given four floating point DSPs to evaluate and shrink calibration data.

The BOC itself is an I/O board to the ROD carrying electro-optical converters. It adds delays to sent signals to adjust the detectors phase against the LHC bunch crossing and to the returned data to align it versus the off-detector clocks. An additional feature of the Pixel BOC is decoding of 80 MBit/s streams into two 40 MBit/s Streams, which is an input requirement for the ROD.

Software interfaces have been written for the recent system to run calibration scans, readout histograms and start datataking. It can control all readout hardware, generate configurations for the system automatically and was checked for consistent results during a long calibration phase. Most of this software should be kept as is for the IBL system, particularly important the firmware of the digital signal processors (DSPs) on the Readout drivers, doing most of the data analysis and histogramming. Hence the Pixel readout drivers should not be changed any further than can be done without changes the DSP code significantly.

Requirement 2: Upgrading the System for a new detector Interface

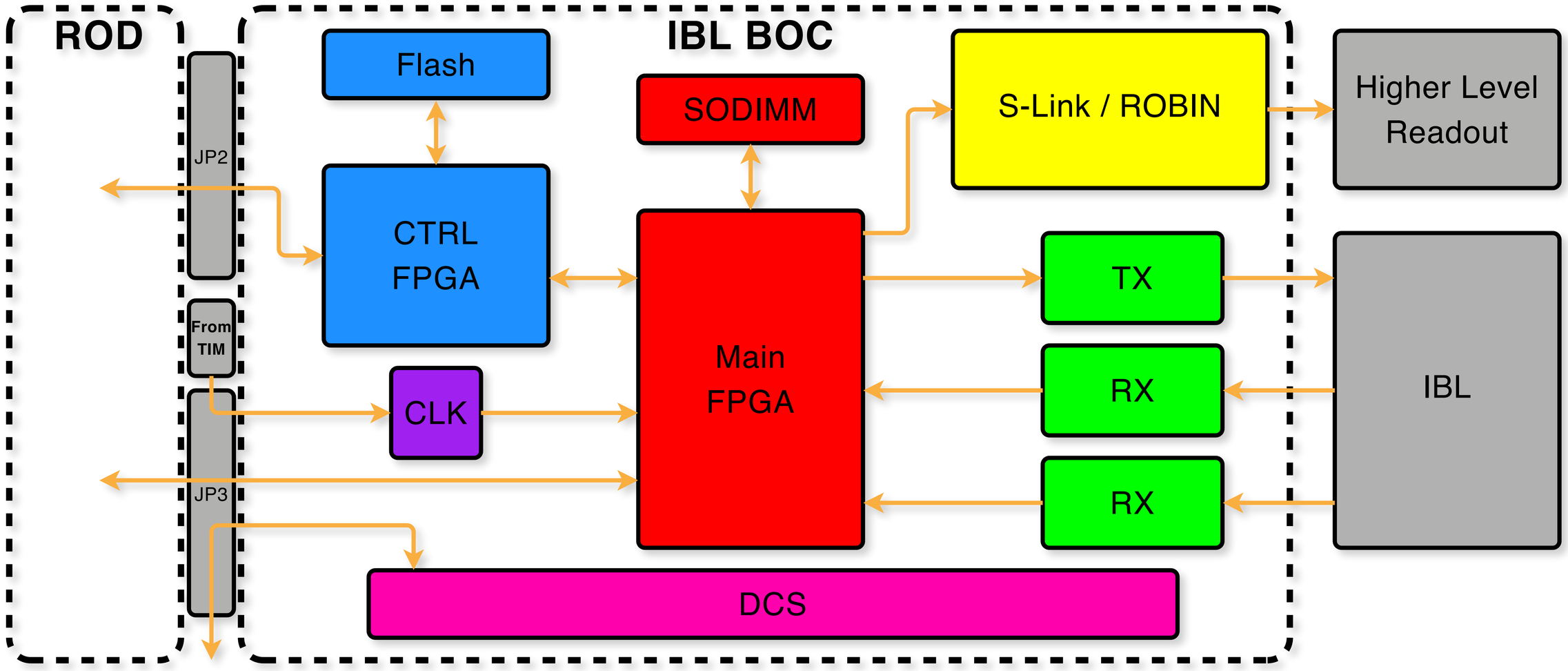
The Insertable B-Layer will suffer higher occupancy due to it's lower distance from the interaction point. As single frontends (two per module) are read out and pixels become smaller for the IBL, the data rate per readout link is lower than that of the recent B-Layer. Estimates still assume more than 80 MBit/s. This will be served with 160 MBit/s readout via a single link, as opposed to two 80 MBit/s links in the existing B-Layer.

Balanced coding is forseen for the coming system, to allow for automated threshold adjustments and clock reconstruction in the off-detector electronics. 8B10B encoding will therefore be integrated into the next on-detector readout chip. It allows to use market solutions for CDR (clock-data-recovery) and implementing simple failure checks via parity control. The receiver can automatically sense the average light level per transmission line and a per channel monitoring gives direct status information.

The BOC **must** be upgraded to handle the new data rate and, in the process of keeping things simple, adjust it for the RODs input. A decoder will be integrated into the BOC, which implies a change in data rate, down to 128 MBit/s. As the data protocol forsees to use special transmission codes for event headers and trailers, the easiest solution here is to implement the first reception buffer into the BOC and give buffer status flags to the ROD, which then reads from the BOC asynchroneously.

The Timing, Trigger and Control (TTC) path will use the same encoding standard as is used in the recent ATLAS Pixel detector, BiPhase Mark encoding, given by the recently used transmission IC, the BPM-12. To reduce the number of transmission channels needed here, two frontends (a module) will have a common TTC line.

Insertable B-Layer Back of Crate Card Schema



IBL BOC Concept: Reprogrammable Logic at it's heart...

Following the requirements, a first schema for the IBL BOC has been decided on, which allows for maximum flexibility in implementation of other components. Additional features that seemed missing in the previous system have also been included into the new schema.

The central core of the IBL BOC is a large programmable device, which connects to any data-path element of the BOC, Receivers (RX), Transmitters (TX) and Higher Level Readout Connections. Additionally most of the backplane should be directly fed into it. Thereby a decision about the final mode of operation can be made at a later point of time, when the IBL system gets into a production stage.

An interface FPGA is to serve firmware to the core and deliver a bus interface to the ROD, thereby serving a stable interface to the BOC and giving in-system upgrade capability. This FPGA will only be programmable by manual intervention.

An ATLAS ELMB will be mounted to read monitoring values from the BOC and serve as a natural DCS interface.

Optical converter boards will be served with the same sockets as before, leaving a chance to attach different plugins to the same position after reprogramming the core FPGA.

The connection to the higher level readout will be prepared as a mezzanine slot. Opposing to the recent BOC, this will be served with a reprogrammable Interface and is planned to host a single ROBIN card. This will remove a transmission line from the system, giving a faster and simpler interface between the ROD/BOC and the level 2 trigger.

Upgrading the BOC: A new IBL Readout Concept

In preparation are multiple layouts for the IBL readout architecture:

The simplest one is, to keep the ROD as is and let the BOC be the I/O card as it used to be, decreasing data rate per signal line on the inputs.

A much more complicated solution includes redesigning the ROD, allowing it to operate faster - in particular concerning total throughput in data taking and VME performance.

Our favoured approach goes with a reproduction of the previous RODs with simple modifications: The data path is removed from the ROD and placed inside the BOC. Calibration data is handed to the RODs DSPs via a reversed SLink interface. Advantages are:

1) The ROD could be reproduced from the same Layouts, but exchanging some buffer ICs.

2) Lots of components would not be needed on the ROD, in particular 9 FPGAs and obsolete memories. Production would be significantly cheaper.

3) In Data taking, the BOC would deliver the data path with the maximum rate defined by the output device. Assuming data taking is completely independent of the ROD, the total data rate per building block could be increased by a factor of two, given a direct interface to a ROBIN daughterboard. Hence the number of racks needed to read out the IBL will go from two down to one.

To circumvent changing the DSP code, FPGAs on the ROD would be reprogrammed in this approach, to map the previous ROD addresses to the BOC.