

Novel charge sensitive amplifier design methodology suitable for large detector capacitance applications

Thursday, 24 September 2009 16:55 (20 minutes)

Alternative current mode charge sensitive amplifier (CSA) topology and related methodology for use as pre-amplification block in radiation detection read out front end IC systems is proposed. It is based on the use of a current conveyor architecture providing advantageous noise performance characteristics in comparison to the typically used CSA folded cascode structure. In the proposed architecture the CSA output noise is independent of the detector capacitance value, allowing the use of large area detectors without affecting the system noise performance. Theoretical analysis and simulation based results are confirmed by measurements on a prototype demonstrating the advantageous performance in relation to the traditional voltage mode structures mainly in terms of the noise performance dependency on the detector capacitance value.

Summary

In charge sensitive amplifiers, the minimum charge that can be detected by the detector-preamplifier system is limited by the noise level reducing the system resolution. It is therefore greatly important to reduce the noise sources contribution. In radiation detection systems the noise is dependent on the detector capacitance value, its associated leakage current and the noise produced mainly by the preamplification block. Using the folded cascode preamplifier typical amplification scheme, the total output noise, for a large detector capacitance applications, is proportional to the detector capacitance value. While large area detectors can offer increased sensitivity, they also should be divided in pixels in order to minimise the total noise and each pixel needs its own readout circuit.

In this work we propose a current mode amplification scheme which can be used with large area detectors without affecting the noise level. This configuration is based on the use of second generation current conveyor (CCII) providing output noise independent to the detector capacitance value, allowing the use of large area detectors without affecting the system noise performance. Theoretical analysis and simulation results are confirm the operation –performance of the proposed topology. Measurement results on a current mode CSA prototype fabricated in a 0.35 μm CMOS process by AMS are provided supporting the theoretical and simulation analysis and confirming the advantageous performance in relation to the traditional voltage mode structures mainly in terms of the noise performance dependency on the detector capacitance value.

Primary authors: Dr SARRABAYROUSE, Gerard (CNRS; LAAS; 7 avenue du colonel Roche, F-31077 Toulouse, France and Université de Toulouse; UPS, INSA, INP, ISAE; LAAS; F-31077 Toulouse, France); Mr BARY, Laurent (CNRS; LAAS); Prof. SISKOS, Stylianos (Electronics Lab. , Physics Dept., Aristotle Univ. of Thessaloniki, 54124 Thessaloniki Greece); Dr NOULIS, Thomas (Electronics Lab. , Physics Dept., Aristotle Univ. of Thessaloniki, 54124 Thessaloniki Greece)

Presenter: Dr NOULIS, Thomas (Electronics Lab. , Physics Dept., Aristotle Univ. of Thessaloniki, 54124 Thessaloniki Greece)

Session Classification: POSTERS SESSION

Track Classification: ASIC's