Readout and Data Processing Electronics for the Belle-II Silicon Vertex Detector

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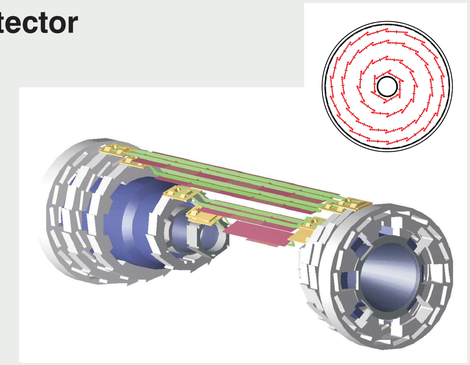
ABSTRACT

A prototype readout system has been developed for the future Belle-II Silicon Vertex Detector at the Super-KEK-B factory in Tsukuba, Japan.
It will receive raw data from double-sided sensors with a total of approximately 240,000 strips read out by APV25 chips at a trigger rate of up to 30kHz and perform strip reordering, pedestal subtraction, a two-pass common mode correction and zero suppression in FPGA firmware.
Moreover, the APV25 will be operated in multi-peak mode, where (typically) six samples along the shaped waveform are used for precise hit-time reconstruction which will also be implemented in FPGAs using look-up tables.

BELLE SVD

Silicon Vertex Detector
SVD2.0

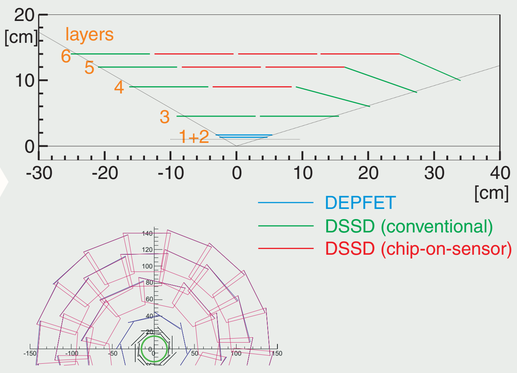
Layers: 4
Sensors: 246 (4") double-sided silicon strip detectors (DSSD)
Radii: 2.0...8.8 cm
Active area: 0.5 m^2
Readout channels: 111 k
Front-end chip: VA1TA (0.8 μs shaping time)



Upgrade until 2013

Target luminosity: 8 x 10^{35} $cm^{-2}s^{-1}$
About 40 times the present value
Accordingly increase of background
Limits: occupancy, trigger rate (deadtime)

Solution: new vertex detector and readout electronics using APV25

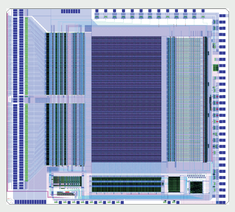


Belle-II Silicon Vertex Detector
SuperSVD

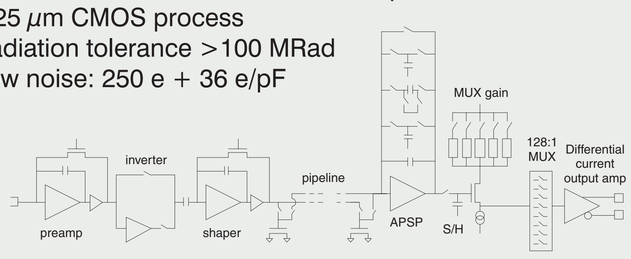
Layers: 2 DEPFET (pixels) + 4 DSSD
Sensors: 182 (6") DSSDs
Radii: 1.8 / 2.2 / 3.8 / 8 / 11.5 / 14 cm
Active area: ~1.2 m^2
Readout channels: 11 MPx, 240 k strips
Front-end chip: APV25 (strips) (50 ns shaping time)
DEPFET (pixels)

APV25

APV25 Front-End Chip Features



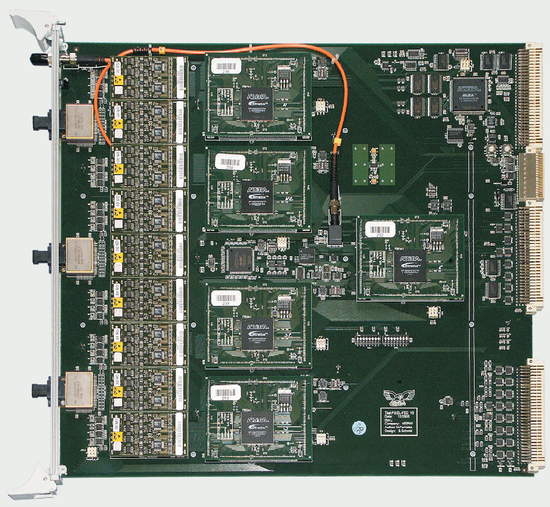
40 MHz operation
128 channels
192 cell deep analog pipeline
50 ns shaping time (adjustable)
Modes: Peak / Deconvolution / Multi-peak
0.25 μm CMOS process
Radiation tolerance >100 MRad
Low noise: 250 e + 36 e/pF

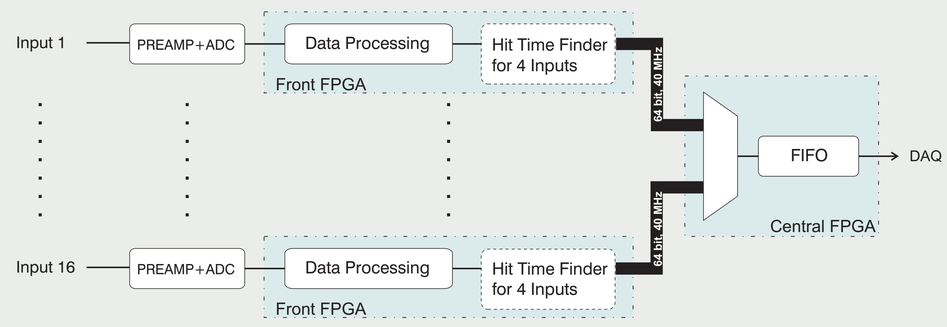


FADC + PROCESSOR

FADC + PROCESSOR Features

16 input channels
12 bit ADC
Data processing & zero suppression
Hit time reconstruction
64 bit, 40 MHz local bus
Transparent mode (pedestal determination)
Processed mode (optional w/o time finding)

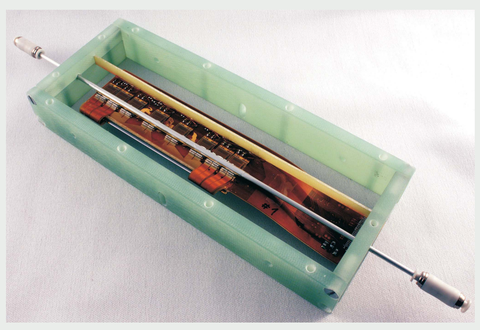




Block diagramm of the data processing chain.

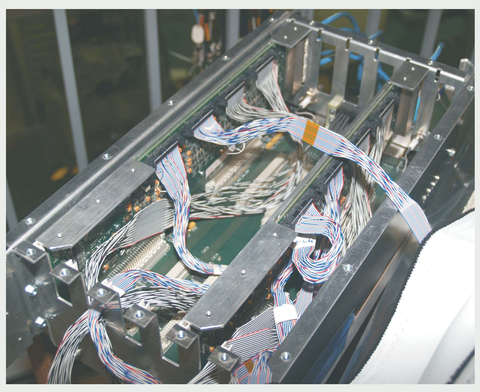
The FADC+PROCESSOR is a 9U VME board with 16 input channels used to digitize and process the data of the APV25 chips. The core functions are implemented in FPGAs and thus can easily be adapted by modifying the firmware.
A dedicated data processing chain is forseen for each input, performing APV25 header detection, strip reordering, a two-pass common mode correction, zero suppression and hit time reconstruction (see below). Finally position, pulse height and timing information of a hit are encoded in a single 32 bit wide word.
Thanks to the pipelined design with several FIFOs and a 64 bit wide local bus, data can be processed continously as long as they are fetched by the downstream DAQ system without congestion. Thus the acceptable trigger rate is about 50 kHz, limited by the time needed to read out the samples from the APV25 chips.

READOUT CHAIN



Front-end:

Flexible Circuit with thinned APV25 chips using the Origami Chip-on-Sensor concept for low material budget (see presentation by Christian Irmler on Thursday morning for details).



Dock-box:

Motherboard (Mambo) with up to 6 Repeater boards (Rebo) for signal level translation, signal buffering, power monitoring and overvoltage protection.

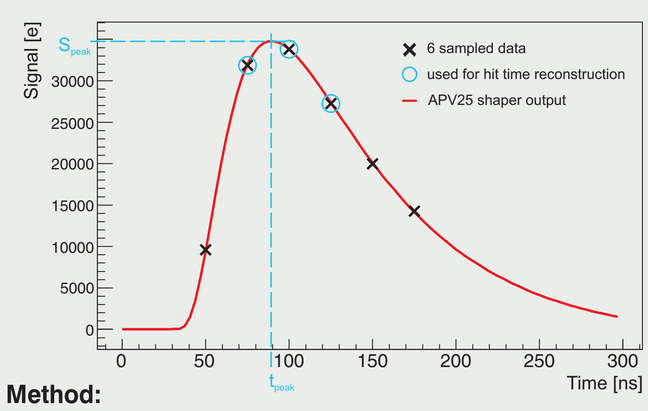
Back-end:

VME controller board (Neco) for trigger and control signals.

FADC boards with online data processing using FPGAs.

Data acqusition (DAQ)

HIT TIME RECONSTRUCTION

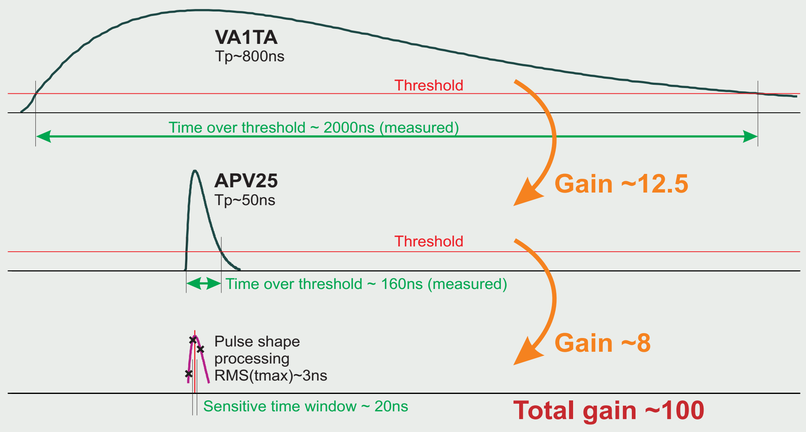


Method:

The multi-peak mode of the APV25 allows to take 3, 6, 9, ... consecutive samples of the shaper output signal. Three points around the maximum of the curve can be used to determine timing and amplitude of the peak with lookup tables, which are generated from the calibration pulse of the APV25.
Thanks to using only three out of six samples, a trigger jitter of up to +/- 2 clocks can be tolerated.
A time resolution of 2 ... 3 ns RMS can be achieved with this method, depending on the signal-to-noise ratio (SNR).

Advantage:

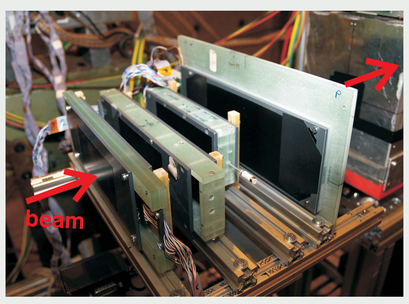
The sensitive time window and thus the occupancy depends on the shaping time (T_p) of the front-end chip. Hence, a gain of ~12.5 can be achieved by using the APV25 instead of the VA1TA.
However, knowing the timing information of the hits, an additional reduction of the sensive time window by a factor of ~8 is possible.
The knowledge of the correct timing further allows to match hits across layers and reject off-time background in the offline analysis.

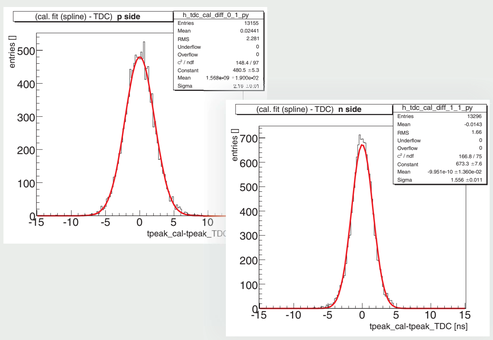


BEAM TEST RESULTS

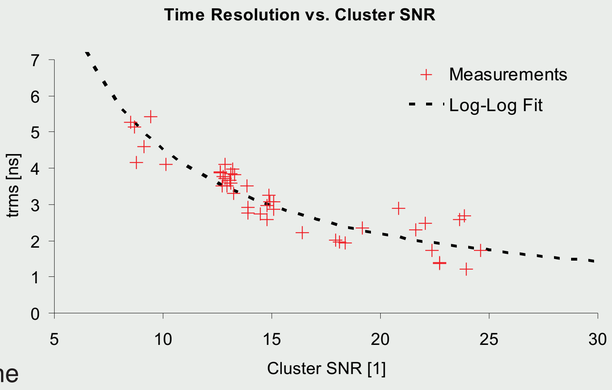
Beam test setup:

The readout system was tested in several beam tests at KEK and CERN together with four DSSD modules, which are all prototypes for the SuperSVD equipped with APV25 chips.





Residual distributions of the fitted peak time against a TDC reference measurement: ~2 ns RMS.
At the time of the beam test the hit time finder was not yet implemented in the FPGA firmware, a numerical offline fit was used instead.



Achieved time resolution of all modules and beam tests as a function of the SNR. The results can be fit by a straight line in a log-log mode.

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