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Readout and Data Processing Electronics for the Super-Belle Silicon Vertex Detector

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A prototype readout system has been developed for the future Super-Belle Silicon Vertex Detector at the Super-KEK-B factory in Tsukuba, Japan. It will receive raw data from double-sided sensors with a total of approximately 250,000 strips read out by APV25 chips at a trigger rate of up to 30kHz and perform strip reordering, pedestal subtraction, a two-pass common mode correction and zero suppression in FPGA firmware. Moreover, the APV25 will be operated in multi-peak mode, where (typically) six samples along the shaped waveform are used for precise hit-time reconstruction which will also be implemented in FPGAs using look-up tables.

Summary

The Belle experiment at KEK will finish in early 2010, followed by a major upgrade of both the KEK-B machine as well as the detector. The ultimate luminosity target is up to 8 x 10^35 cm^-2s^-1, or a factor of 50 higher than now. The present Belle detector and its Silicon Vertex Detector (SVD2) in particular must be completely replaced for this challenging endeavor, as its innermost layer is already at the limit in terms of occupancy and dead time. Both are related to the readout chip, which is currently a slow-shaping VA1TA with moderate readout speed and no pipeline.

The future Super-Belle SVD will be equipped with APV25 readout chips (originally developed for CMS), which feature fast shaping (50ns), a 192-cell deep pipeline and a readout speed of 40MHz. As the occupancy observed in the detector scales with the peaking time of the shaping amplifier, we get a reduction factor of ~12.5 compared to the present system. In CMS, the APV25 chips are used in so-called deconvolution mode, where a switched capacitor filter narrows the pulse down to a single clock for unambiguous association with a certain bunch crossing. This feature requires a clock-synchronous beam and thus cannot be used with the quasi-continuous beam of (Super-)KEK-B. Nonetheless, a similar feature can be implemented outside of the APV25 chip by using its multi-peak mode where it samples several points along the shaped waveform of a single hit. These data can be processed in order to find the hit time with a precision of a few nanoseconds, depending on signal-to-noise. This method yields another gain of up to 8 in terms of occupancy, or up to 100 in total compared to the current system.

We have developed a prototype readout system consisting of repeater boxes in the front-end and VME-based Controller and FADC+Processor modules in the back-end. The connections are made by 30m of CAT7 cables and equalizers are used to compensate the cable loss for the multiplexed analog strip data being transmitted at a rate of 40 million samples per second.

The repeaters do not only buffer analog and control signals, but also perform the level translation between the front-end, which sits at the bias voltage of the detector, and the back-end which is grounded. This is achieved by capacitive coupling for fast signals (analog, clock, trigger) and optocouplers for slow controls.

The FADC+Processor VME boards perform digitization at an individually

adjustable clock phase for each input and digital data conditioning in Altera Stratix FPGAs. Each channel has its own pipelined processing chain which runs at the same speed as data are received. After re-ordering, the silicon strip data are treated with the typical steps of pedestal subtraction, common-mode correction and zero suppression. Moreover, the APV25 will deliver 6 samples along the shaping curve, such that we can use three samples around the maximum together with pre-loaded look-up tables to quickly find the peak time for each hit. Together with a precise time reference from the trigger system, our electronics can reduce the amount of data such that only the hits which belong to the event in question are passed on to the DAQ system.

Primary authors: IRMLER, Christian (HEPHY Vienna); PERNICKA, Manfred (HEPHY Vienna); Dr FRIEDL, Markus (HEPHY Vienna)

Presenter: Dr FRIEDL, Markus (HEPHY Vienna)

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