Contribution ID: **23** Type: **Oral**

BAO radio electronic system

Tuesday, 22 September 2009 11:25 (25 minutes)

The description of the electronic chain for the BArionicOscillation project
The BAO Radio project aims at mapping the H gas distribution in the universe using the 21 cm (1420 MHz) hyperfine transition of atomic hydrogen, up to red-shifts z ˜ 1.5-2. The main goal of the project is to constrain the Dark Energy properties using the BAO (Baryon Acoustic Oscillation) cosmological probe, which can be considered as a "standard ruler". The large frequency range (0.5-1.5 GHz), large sky coverage (1/2 sky) and resolution (˜ 10 arc") are the main observational constraints which have driven the electronics. The electronics chain is installed for test at the second biggest radio-telescope in the word at Nancay (France) and foreseen to be installed at Pittsburgh (USA). Its architecture can be separated in 3 segments: antenna/RF amplifier, digitization/signal processing/transmission, acquisition by PC. The analog signal coming from the dipole is amplified by a warm LNA then sent to the RF board on a 50-ohm copper cable. The latter behaves as amplifier/mixer: analog signal is filtered and thanks to a 1.2GHz local oscillator split in four 250 MHz bands to match the Nyquist condition of the 500 MHz digitization. This way the analog signal can directly enter the ADC, avoiding an anti-aliasing filter at its input. Nevertheless the possibility to work in down-conversion mode is foreseen, taking advantage of the 1500 MHz analog input bandwidth. The card is a 4-channel VME/USB board. It embeds two 500-MHz ADC, two StGX FPGA and 5-Gbits/s optical drivers. The FPGA perform the FTT in streaming mode, pack data, serialize it and encode it in a 8b/10b protocol and then send it on a 5 Gbit optical link. The PC server house a PCIExpress board based on a Actel STRATIXII, a raid controller board wich is able to manage 8 sata2 hard disk of 160GByte. The FPGA integrate: 128kByte of memory, a controller of the data integrity and a PCIExpress 4x interface. With this architecture we reach 500MByte/s of data transfer to the ram of the PCI and 360MByte/s from the ram to the disk.

Primary author: Mr CHARLET, Daniel (Laboratoire de l"Accelerateur Lineaire (LAL) (IN2P3) (LAL))

Presenter: Mr CHARLET, Daniel (Laboratoire de l"Accelerateur Lineaire (LAL) (IN2P3) (LAL))

Session Classification: Parallel session B1 - Systems, Installation and Commissioning

Track Classification: Systems, installation and commissioning